# 4V-28V Vin, 6A Synchronous Step-down DCDC Converter Integrated with a 3.3V and 150mA LDO

## FEATURES

- Wide 4V-28V Input Voltage Range
- 0.6V-5.5V Output Voltage Range
- 6A Continuous Output Current
- Integrated 36mΩ/16mΩ Rdson of HS/LS Power MOSFETs
- A 3.3V, 150mA LDO Integrated
- Fixed 1ms Soft-start Time
- Fixed 400KHz Switching Frequencies
- Selectable PWM, PFM and USM Operation Modes
- Cycle-by-Cycle Current Limiting
- Output Over-Voltage Protection
- Over-Temperature Protection
- Available in a FCUTQFN3*3-12L Package

## APPLICATIONS

- Auto
- DTV, Monitor/LCD Display
- Printer, Charging Station
- Industry PC

## DESCRIPTION

The SCT2361 is a high efficiency synchronous step-down DC-DC converter integrated with a 3.3V, 150mA LDO. With the wide 4V-28V input voltage range and adjustable output voltage down to 0.6V, the SCT2361 supplies continuous 6A output current. The device fully integrates high-side and low-side power MOSFETs with 36mΩ/16mΩ on-resistance to minimize the conduction loss. The Supply of integrated 3.3V output LDO has path management between Vin and DC-DC converter output to achieve the lower power loss and better thermal performance.

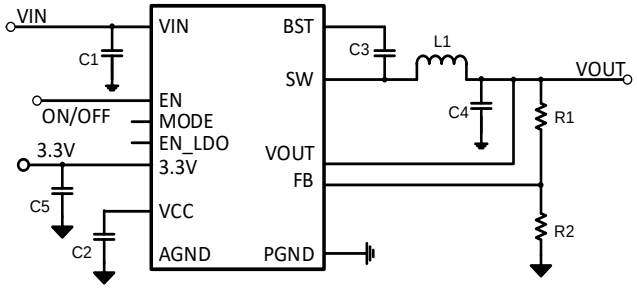
The SCT2361 adopts a Constant On-Time (COT) control to provide fast transient response and easy loop stabilization. The device offers fixed 1ms soft start to prevent inrush current during the startup of output voltage ramping.

The SCT2361 has the MODE pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save, or Ultrasonic Mode (USM) to keep the switching frequency above audible frequency areas during light-load or no-load conditions, or the PWM mode to achieve the small output ripple.

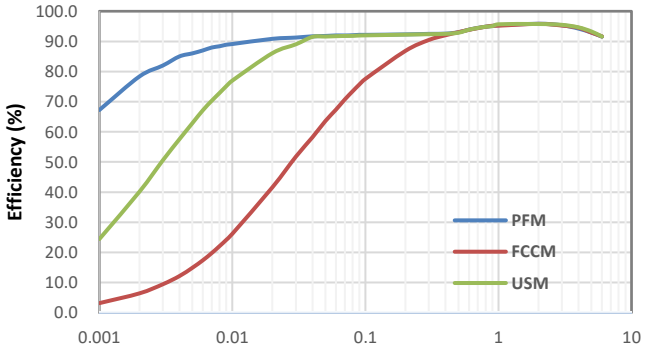
Full protection includes over current protection, under-voltage protection, and thermal shutdown.

The converter requires a minimum number of external components and is available in a FCUTQFN3*3-12L package.

## TYPICAL APPLICATION




**4V-28V, Synchronous Buck Converter**




**VIN=12V, Vout=5V, $F_{SW}$=400kHz**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Production.

Revision 1.1: Update Equation 1, Equation 2 and Figure 9.

Revision 1.2: Update Device Order Information.

Revision 1.3: Update PACKAGE INFORMATION.

Revision 1.4: Update package name and MSL level.

## DEVICE ORDER INFORMATION

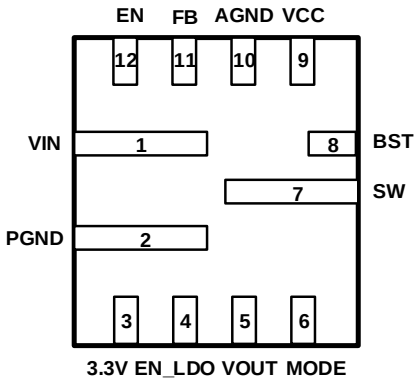
| ORDERABLE DEVICE | PACKAGING TYPE | STANDARD PACK QTY | PACKAGE MARKING | PINS | PACKAGE DESCRIPTION | MSL |
|---|---|---|---|---|---|---|
| SCT2361FPBR | Tape & Reel | 5000 | 2361 | 12 | FCUTQFN 3*3-12L | 1 |

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

| DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|
| VIN, EN | -0.3 | 32 | V |
| SW | -1 | 32 | V |
| BST | -0.3 | 38 | V |
| BST-SW | -0.3 | 6 | V |
| 3.3V, EN_LDO, VOUT, MODE, VCC, FB | -0.3 | 6 | V |
| Operating junction temperature(2) | -40 | 125 | C |
| Storage temperature $T_{STG}$ | -65 | 150 | C |

## PIN CONFIGURATION




Top View: FCUTQFN3*3-12L, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

## PIN FUNCTIONS

| NAME | NO. | PIN FUNCTION |
|---|---|---|
| VIN | 1 | Input voltage. Decouple the input rail with at least a 0.1uF and 10uF input ceramic capacitor. Place the capacitor as close to VIN and PGND pins as possible. Use wide PCB traces and multiple vias to make the connection. |
| PGND | 2 | Power ground. Using wide PCB traces and multiple vias large enough to handle the load current. |
| 3.3V | 3 | The output of the 3.3V, 150mA LDO output, at least a 4.7uF ceramic cap connected between VCC pin and ground. |
| EN_LDO | 4 | Enable logic input. EN_LDO is a digital input that controls the 3.3V LDO on or off. EN_LDO high turns on the LDO and EN_LDO low turns off the device. Floating EN pin automatically starts up the LDO. |
| VOUT | 5 | VOUT is used to sense the output voltage of the buck regulator. Connect VOUT to the output capacitor of the regulator directly. Keep the VOUT sensing trace far away from the SW node. VIAs should also be avoided on the VOUT sensing trace. A trace larger than 25mil is required. |
| MODE | 6 | PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM. |
| SW | 7 | Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized. |
| BST | 8 | Bootstrap. Must connect a 0.1uF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET. |
| VCC | 9 | Internal VCC LDO output. The driver and control circuits are powered by VCC. Decouple with 1μF ceramic capacitor placed as close to VCC as possible. |
| AGND | 10 | Signal logic ground. AGND is the Kelvin connection to PGND. |
| FB | 11 | Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical. |
| EN | 12 | Enable logic input. EN is a digital input that controls the converter on or off. EN high turns on the device and EN low turns off the device. Connecting to VIN with a 100kΩ pull-up resistor can enable the device. Floating EN pin automatically starts up the converter. |

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 4 | 28 | V |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

## ESD RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1) | -2 | +2 | kV |
| | Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1) | -0.5 | +0.5 | kV |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## THERMAL INFORMATION

| PARAMETER | THERMAL METRIC | FCUTQFN3*3-12L | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance(1) | 50 | °C/W |
| $R_{\theta JC}$ | Junction to case thermal resistance(1) | 12 | |

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2361 is mounted. The PCB board is a heat sink that is soldered to the leads of the SCT2361. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN}$=12V, $T_J$=-40°C~125°C, typical value is tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply and Output** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 4 | | 28 | V |
| $V_{IN\_UVLO}$ | Input UVLO<br>Hysteresis | $V_{IN}$ rising | | 3.8<br>300 | | V<br>mV |
| $I_{SD}$ | Shutdown current | EN=0, No load, VIN=12V | | 1 | 5 | uA |
| $I_Q$ | Quiescent current | EN=floating, No load, No switching. VIN=12V. BST-SW=5V | | 135 | | uA |
| $V_{CC}$ | $V_{CC}$ internal LDO regulator voltage | $I_{VCC}$=0mA | 4.75 | 5 | 5.25 | V |
| $V_{CC\_LR}$ | $V_{CC}$ internal LDO load regulation | $I_{VCC}$=5mA | | 1 | | % |
| $I_{VCC\_LIM}$ | $V_{CC}$ internal LDO current limit | VCC short to ground | | 30 | | mA |
| **Buck Reference** | | | | | | |
| $V_{REF}$ | Reference voltage of FB | $T_J$=25°C | 0.594 | 0.6 | 0.606 | V |
| $I_{FB}$ | FB pin leakage current | $V_{FB}$=1.2V | | | 100 | nA |
| **3.3V LDO** | | | | | | |
| $V_{3.3V}$ | 3.3V LDO regulator voltage | $I_{3.3V}$=0mA | | 3.3 | | V |
| $V_{3.3V\_LR}$ | 3.3V LDO load regulation | $I_{3.3V}$=100mA | | 1 | | % |
| $I_{3.3V\_LIM}$ | 3.3V LDO current limit | $V_{3.3V}$=2V | | 180 | | mA |
| | | $V_{3.3V}$=0V | | 50 | | mA |
| **Power MOSFETs** | | | | | | |
| $R_{DSON\_H}$ | High side FET on-resistance | $V_{CC}$=5V | | 36 | | mΩ |
| $R_{DSON\_L}$ | Low side FET on-resistance | $V_{CC}$=5V | | 16 | | mΩ |
| **Enable** | | | | | | |
| $V_{EN\_H}$ | Enable high threshold | | | 1.2 | | V |
| $V_{EN\_L}$ | Enable low threshold | | | 1.09 | | V |
| $I_{EN}$ | Enable pin input current | | | 1.4 | | uA |
| $I_{EN\_HYS}$ | Enable pin hysteresis current | | | 3.6 | | uA |
| $V_{EN\_LDO\_H}$ | Enable high threshold | | | 1.21 | | V |
| $V_{EN\_LDO\_L}$ | Enable low threshold | | | 1 | | V |
| **Operation Mode** | | | | | | |
| $V_{MD\_PWM}$ | PWM mode input logic high threshold | VCC=5V | 4.2 | | | V |
| $V_{MD\_USM}$ | PFM mode with USM logic threshold | | 1.5 | | 3.5 | V |
| $V_{MD\_PFM}$ | PFM mode input logic low threshold | | | | 0.9 | V |
| **Switching Frequency** | | | | | | |
| $F_{SW}$ | Switching frequency | | | 400 | | kHz |
| $T_{ON\_TIME}$ | Minimum On-time | | | 100 | | ns |
| $T_{OFF\_TIME}$ | Minimum Off-time | | | 200 | | ns |
| **Soft Start Time** | | | | | | |
| $t_{SS}$ | Internal soft-start time | | | 1 | | ms |
| **Protection** | | | | | | |

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OVP}$ | Output OVP threshold<br>Hysteresis | $V_{OUT}$ rising | | 120<br>5 | | %<br>% |
| $T_{HIC\_W}$ | OCP hiccup wait time | | | 7 | | Cycles |
| $V_{UVP}$ | Output UVP threshold | $V_{OUT}$ falling | | 75 | | % |
| $I_{LIM\_P}$ | LS MOSFET positive current limit | From source to drain | | 7.5 | | A |
| $I_{LIM\_N}$ | LS MOSFET negative current limit | From drain to source, MODE connects to VCC | | 2.5 | | A |
| $R_{Discharge}$ | SW to ground resistance | | | 100 | | Ω |
| $T_{SD}$ | Thermal shutdown threshold<br>Hysteresis | $T_J$ rising | | 160<br>25 | | °C |

## TYPICAL CHARACTERISTICS

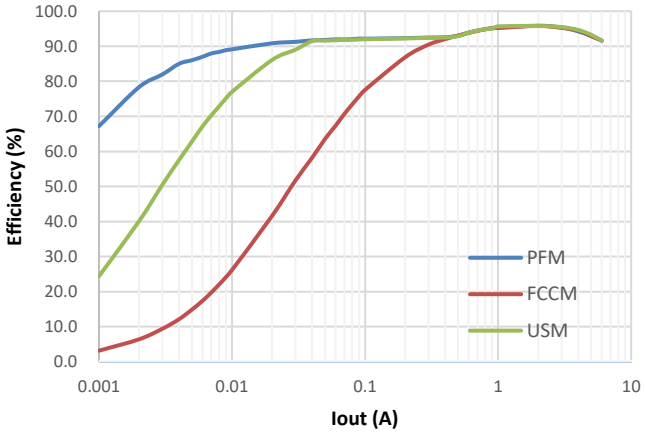



Figure 1. Efficiency, Vin=12V, Vout=5V, Fsw=400kHz

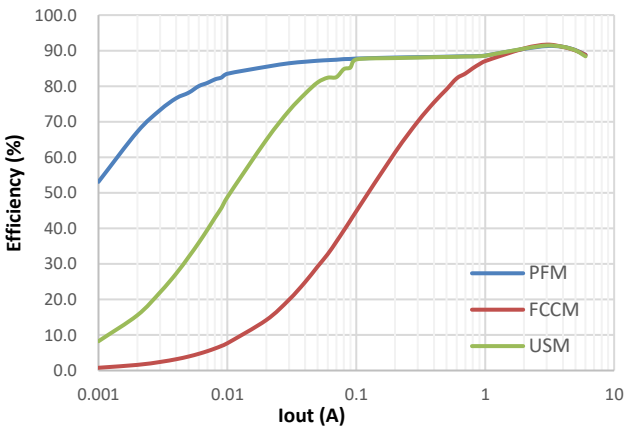



Figure 2. Efficiency, Vin=24V, Vout=5V, Fsw=400kHz

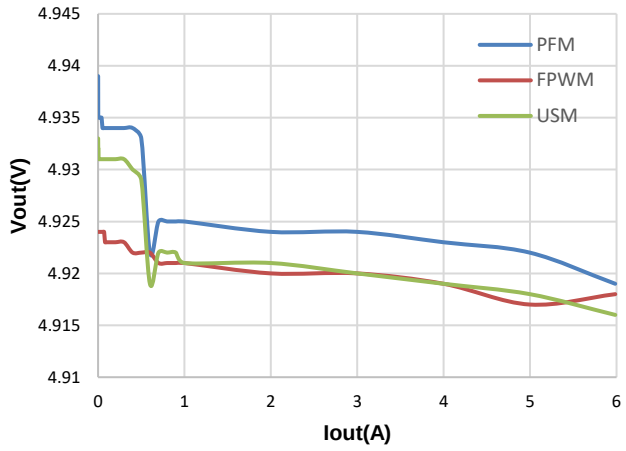



Figure 3. Buck Load Regulation, Vin=12V, Fsw=400kHz

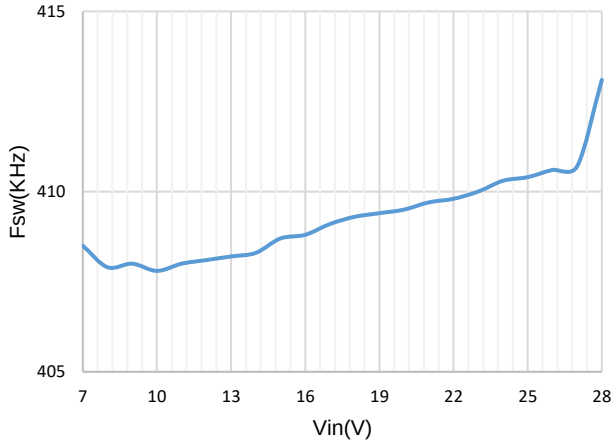



Figure 4. Buck Fsw VS Vin

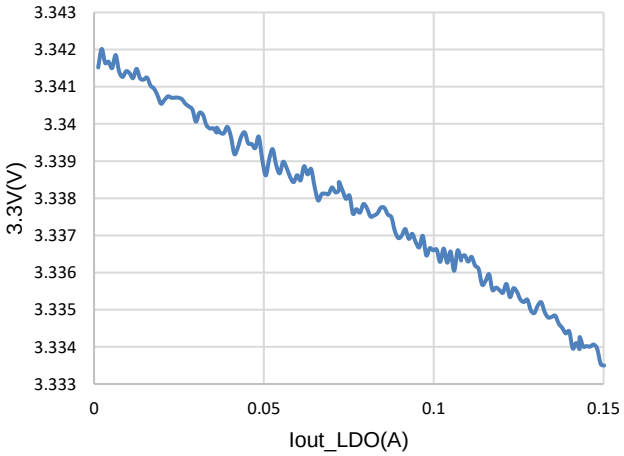



Figure 5. LDO Load Regulation

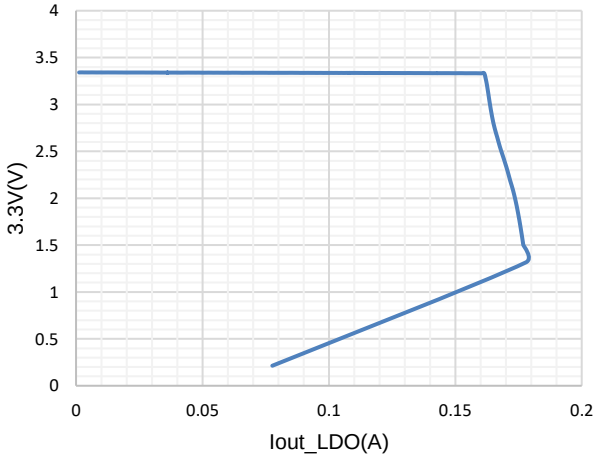



Figure 6. 3.3V LDO, Iout_ldo VS Vout_ldo

## FUNCTIONAL BLOCK DIAGRAM

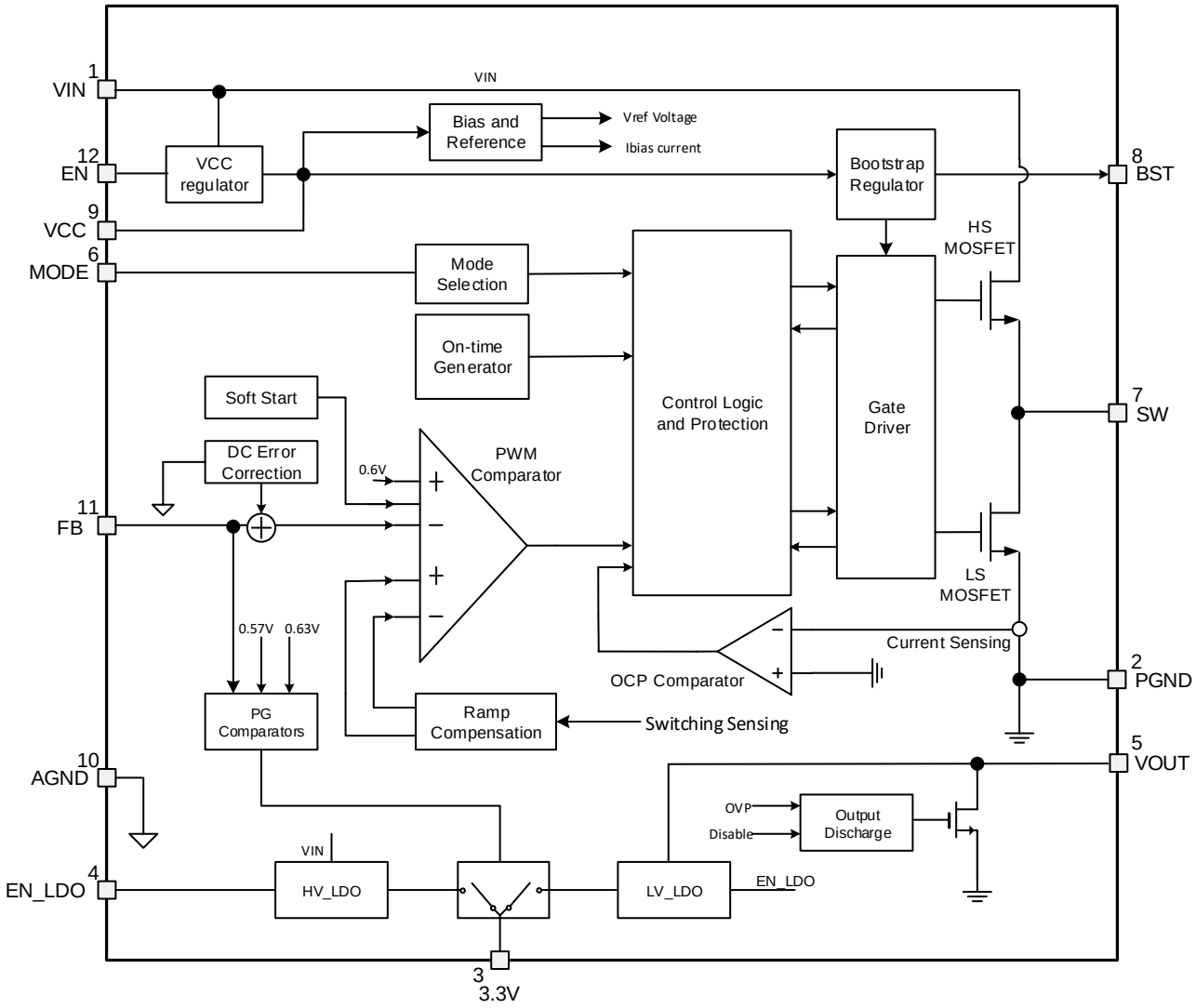



**Figure 7. Functional Block Diagram**

# OPERATION

## Overview

The SCT2361 is a 4V-28V input, 6A continuous output synchronous buck converter with built-in 36mΩ Rdson high-side and 16mΩ Rdson low-side power MOSFETs. It implements the Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is fixed 400kHz to optimizes either the power efficiency or the external components' sizes. The SCT2361 features an internal 1ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device features three different operation modes at light loading: Pulse Frequency Modulation (PFM) mode, and Ultra-Sonic Modulation (USM) mode, and PWM mode. The quiescent current is typically 130uA under no load and sleep mode condition to achieve high efficiency at light load.

The SCT2631 integrates a fixed 3.3V LDO which supplies up to 150mA output current. The LDO output load regulation is less than 1%.

The SCT2361 has a default input start-up voltage of 3.8V with 300mV hysteresis. The EN function features with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin.

The SCT2361 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

## Constant on-time (COT) Mode Control

The SCT2361 employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and output voltage. After the on-time, the Q1 turns off and the low-side MOSFET (Q2) turns on after dead time duration. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreased below the VREF, the Q1 turns during one on-time after another dead time duration. This repeats on cycle-by-cycle based.

The SCT2361 works with an internal compensation for optimizing the loop stability and transient response.

## 3.3V LDO

The SCT2631 integrates a 3.3V LDO which supplies up to 150mA output current. The LDO has an enable pin EN_LDO to realize buck convertor and LDO can work independently.

Meanwhile, SCT2361 has the path management for the LDO, the LDO supply can switch between VIN and the Buck output to save the power loss. If buck is disabled or the output voltage of buck converter drops lower than 4.25V which means the buck not establish well, the LDO input is connected to VIN. When the buck enabled and the output voltage is higher than 4.75V, the LDO input is riding on the Buck output after 500us deglitching time. The recommended output capacitor value is 4.7uF.

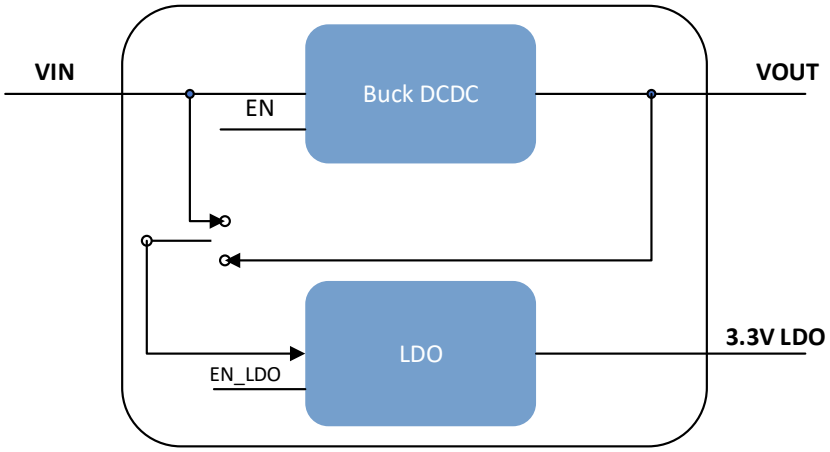



**Figure 8 LDO power path Architecture**

### Pulse Frequency Modulation (PFM) and Ultra-sonic Modulation (USM) Modes

Grounding the MODE pin makes the SCT2361 works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current.

Floating the MODE pin makes the device works at PFM with Ultra-Sonic Modulation (USM) mode to keep the switching frequency out of the acoustic audible frequency. The USM mode block monitors the state of both high-side and low-side MOSFETs. When both high-side and low-side MOSFETs are off for 33us, the low-side MOSFET forces to turn on until the negative current limit is triggered or the feedback voltage (VFB) drops below the internal reference voltage (VREF).

### Forced Pulse Width Modulation (FPWM) mode

Connecting MODE pin to VCC, the SCT2361 forces the device operating at forced Pulse Width Modulation (PWM) mode with pseudo-fixed switching frequency regardless loading current. Operating in PWM mode can achieve smaller output voltage ripple compared with PFM or USM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

### Enable and Under Voltage Lockout Threshold

The SCT2361 is enabled when the VIN pin voltage rises above 3.8V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.5V or when the EN pin voltage is below 1.1V. An internal 1.4uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.2 * \left(1 + \frac{R1}{R2}\right) - 1.4uA * R1 \quad (1)$$

$$V_{fall} = 1.09 * \left(1 + \frac{R1}{R2}\right) - 5uA * R1 \quad (2)$$

where

- $V_{rise}$ is rising threshold of Vin UVLO
- $V_{fall}$ is falling threshold of Vin UVLO

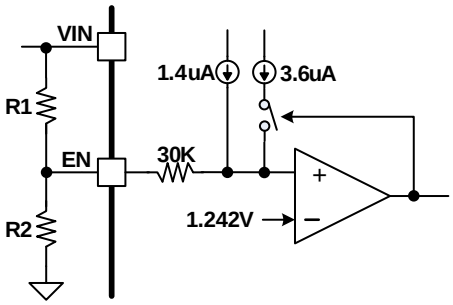



Figure 9. System UVLO by enable divide

### Output Voltage

The SCT2361 regulates the internal reference voltage at 0.6V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- $R_{FB\_TOP}$ is the resistor connecting the output to the FB pin.
- $R_{FB\_BOT}$ is the resistor connecting the FB pin to the ground.

### Internal Soft-Start

The SCT2361 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 1ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

### Mode Selection

The SCT2361 features three different operation modes at light load by easily programming the MODE pin. The programming information is listed in following table. The mode setting is latched in at each power up and is not be able to be modified during operation. Cycling the input power or the EN pin can reselect the switching frequency.

**Table 1. MODE Pin Set-up for Mode Selection**

| MODE Set-up | Floating | Connect to GND | Connect to VCC |
|---|---|---|---|
| Switching Frequency | PFM with USM | PFM | FCCM |

### Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from 5V VCC power or when high-side power MOSFET is off and low-side power MOSFET is on.

### Over Current Limit and Hiccup Mode

The output over-current limit (OCL) is implemented in SCT2361 by using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state of the high-side FET (Q1) by measuring the low-side FET(Q2) drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-

side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decrease linearly. The average value of the switch current is the load current IOUT.

If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 75% of the target voltage, the UVP comparator detects it and shuts down the device immediately, the device re-starts after a hiccup time of 7ms. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. When the overcurrent condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up then the device enters hiccup-mode immediately without a wait time of 1ms.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

### Under-voltage Protection

The SCT2361 features the Under-voltage Protection (UVP) by monitoring the output voltage to detect the under-voltage voltage. When the feedback voltage falls below 75% of $V_{REF}$, the SCT2361 enters hiccup mode until the under-voltage scenario released.

### Over voltage Protection

The SCT2361 implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When the feedback voltage rises higher than 120% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on until trigger negative current limit or FB below reference voltage. Then HS-FET turns on with normal ON-time and turn off, following with a LS-FET on until negative current limited triggered or FB lower than reference voltage. The device exits this regulation period when the feedback voltage falls below 115% of the reference voltage.

### Thermal Shutdown

The SCT2361 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 160C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 135C, the device restarts with internal soft start phase.

# APPLICATION INFORMATION

## Typical Application

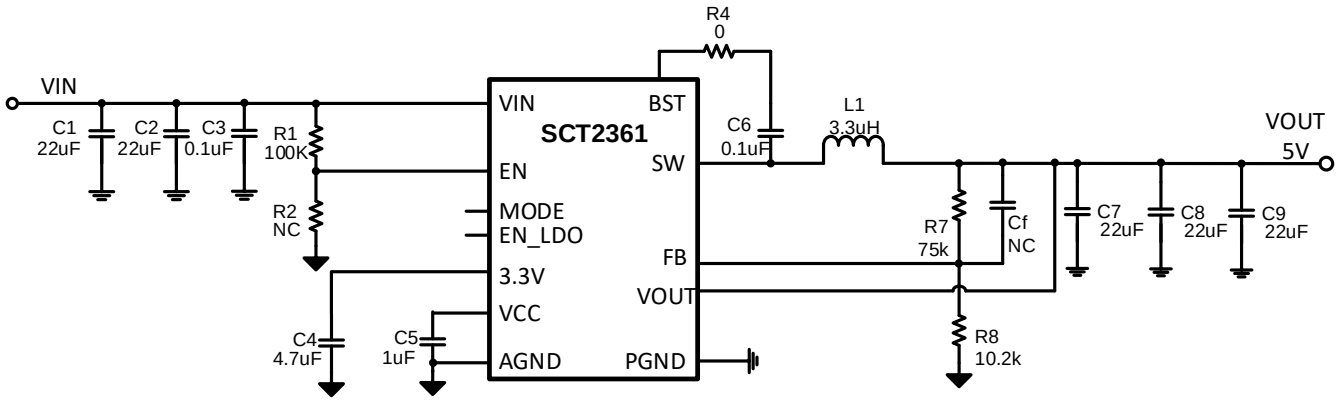



**Figure 10. 12V Input, 5V/6A Output**

**Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 12V |
| Output Voltage | 5V |
| Output Current | 6A |
| Output voltage ripple (peak to peak) | 50mV |
| Switching Frequency | 400kHz |

### Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2361.

Use Equation 4 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where:

- $C_{IN}$ is the input capacitor value
- $f_{sw}$ is the converter switching frequency
- $I_{OUT}$ is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, two 22uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

### Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation 5.

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (5)$$

Where:

- $K_{IND}$ is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, $I_{LPEAK}$, is calculated as in equation 6.

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (6)$$

Set the current limit of the SCT2361 higher than the peak current $I_{LPEAK}$ and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

### Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 7 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (7)$$

Where

- $\Delta V_{OUT}$ is the output voltage ripple
- $f_{SW}$ is the switching frequency
- L is the inductance of inductor
- $C_{OUT}$ is the output capacitance
- $V_{OUT}$ is the output voltage
- $V_{IN}$ is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, three 22μF ceramic output capacitors work for most applications.

### Output Feedback Resistor Divider Selection

The SCT2361 features external programmable output voltage by using a resistor divider network R7 and R8 as shown in the typical application circuit Figure10. Use equation 8 to calculate the resistor divider values.

$$R_7 = \frac{(V_{OUT} - V_{ref}) \times R_8}{V_{ref}} \quad (8)$$

**Table 2. Recommended Component Values for Typical Output Voltage**

| Vin(V) | Fsw (kHz) | Vout (V) | L (uH) | R7 (kΩ) | R8 (kΩ) | Cout(uF) |
|---|---|---|---|---|---|---|
| 12 | 400 | 5.0 | 3.3 | 75.0 | 10.2 | 66uF |
| 24 | 400 | 5.0 | 3.3 | 75.0 | 10.2 | 66uF |

### Application Waveforms(continued)

Vin=12V, Vout=5V, unless otherwise noted

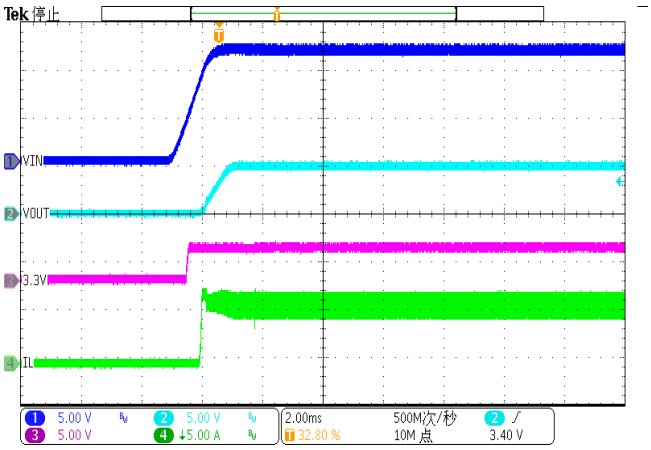



Figure 11. Power up

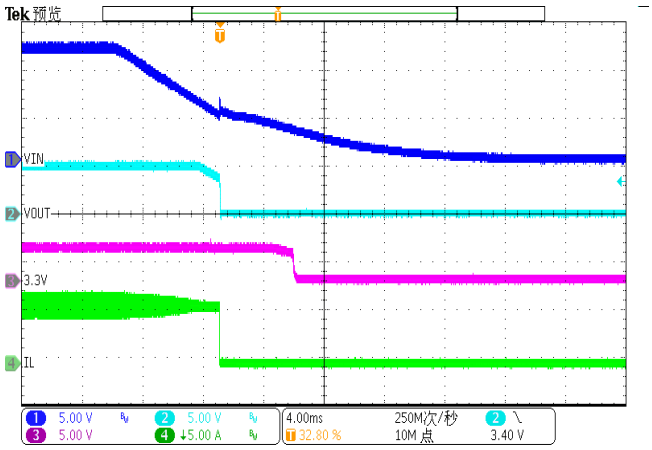



Figure 12. Power down

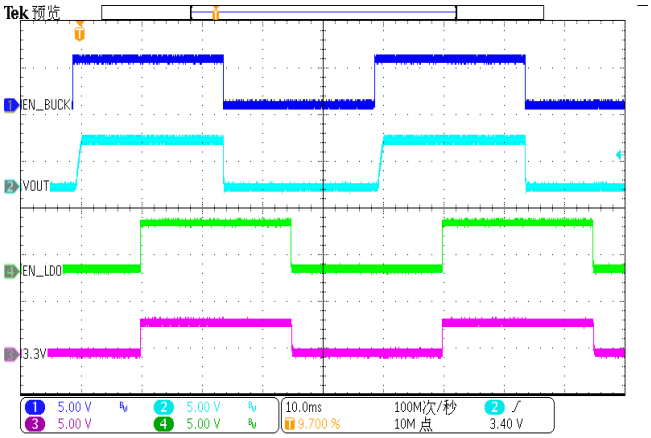



Figure 13. EN toggle(EN_BUCK ahead EN_LDO)

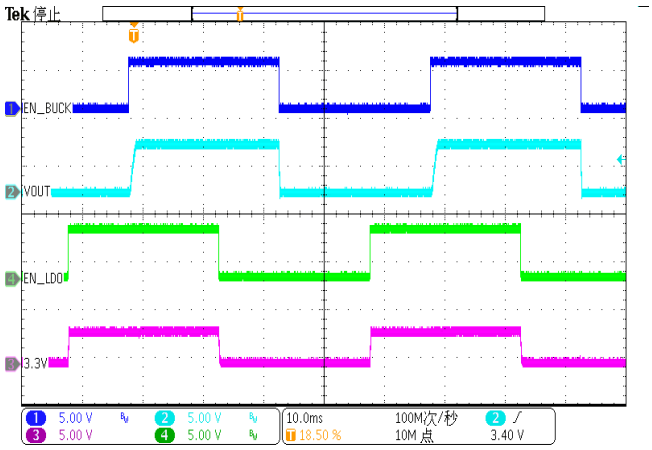



Figure 14. EN toggle(EN_LDO ahead EN_BUCK)

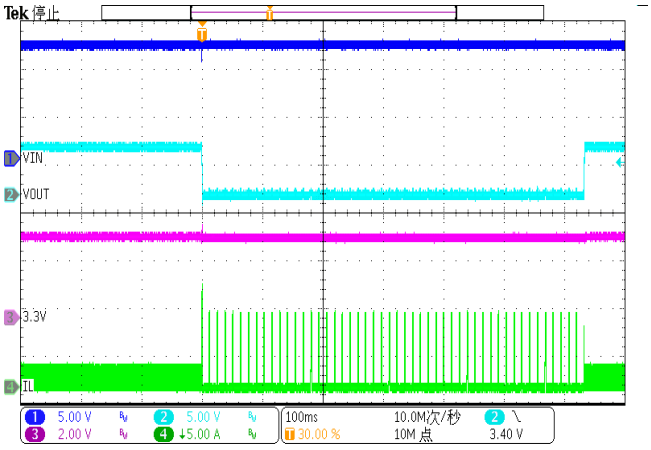



Figure 15. Over Current Protection and Release

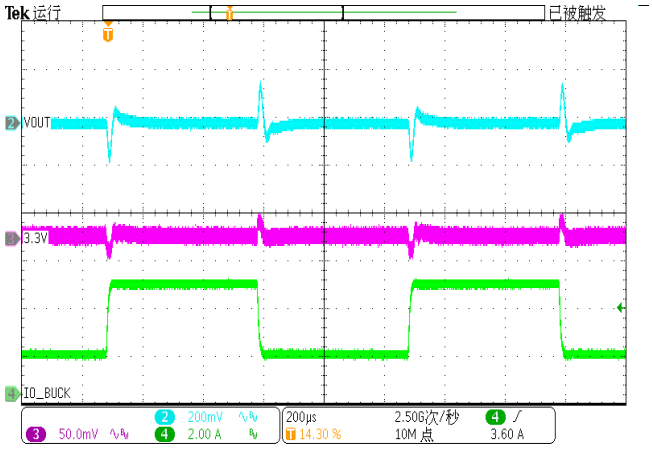



Figure 16. Buck Load Transient (1.5A-4.5A, 1.6A/us)

### Application Waveforms

Vin=12V, Vout=5V, unless otherwise noted

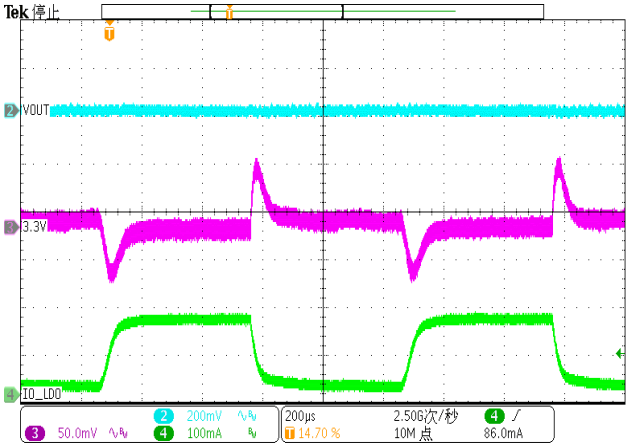



Figure 17. LDO Load Transient (0A-100mA, 1.6A/us)

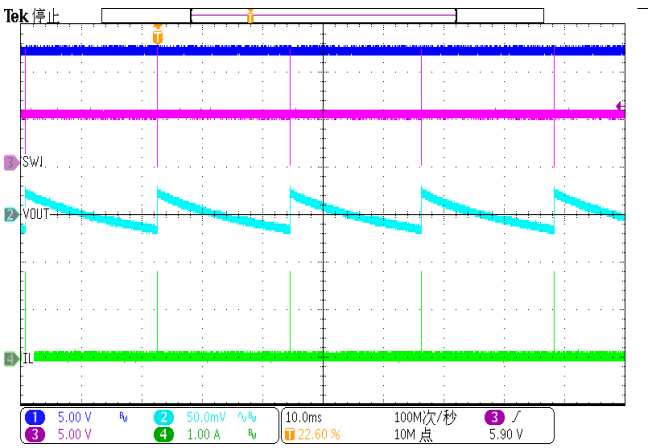



Figure 18. Output Ripple (Iload=0A, PFM)

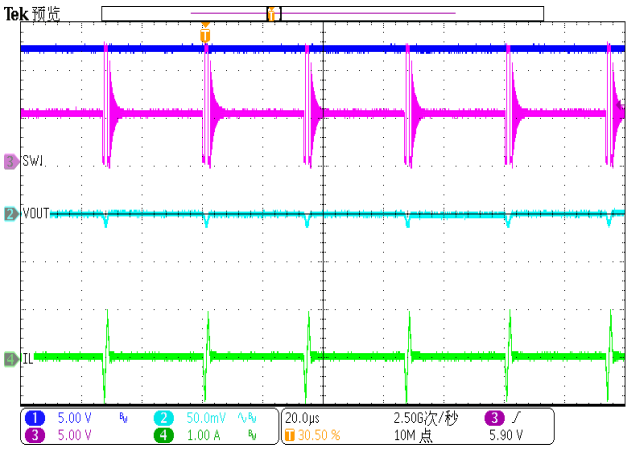



Figure 19. Output Ripple (Iload=0A, USM)

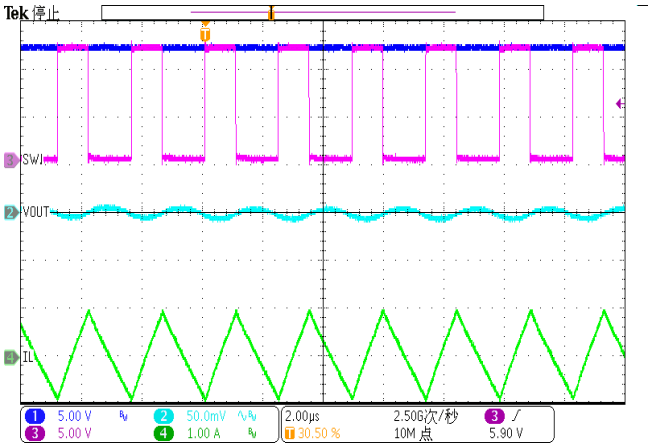



Figure 20. Output Ripple (Iload=0A, FPWM)

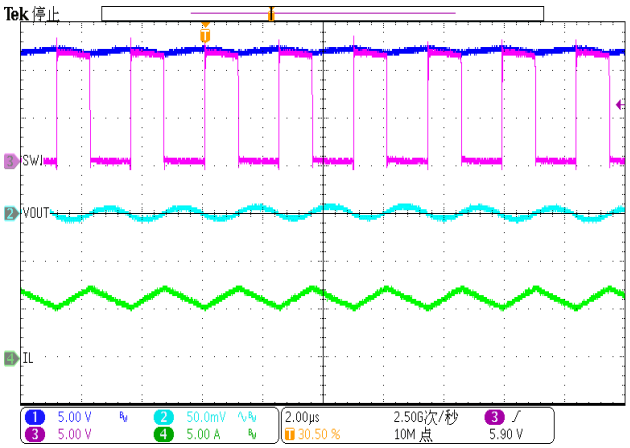



Figure 21. Output Ripple (Iload=6A)

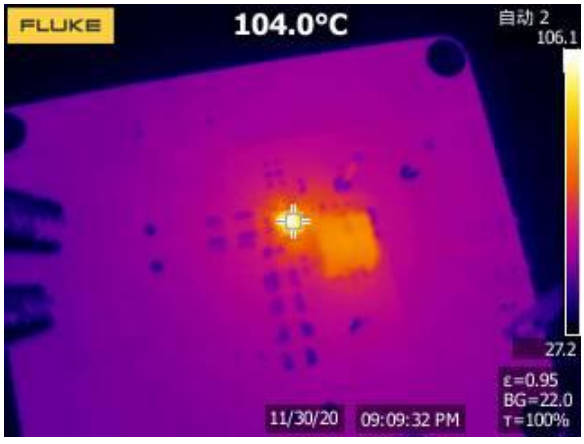



Figure 2. Thermal, 12VIN, Buck Iload=6A, LDO Iload=0.1A

### Layout Guideline

Proper PCB layout is a critical for SCT2361 stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
3. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
4. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
5. UVLO adjust and loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. Route BST resistor and capacitor with a minimized length between the BST PIN and SW PIN.

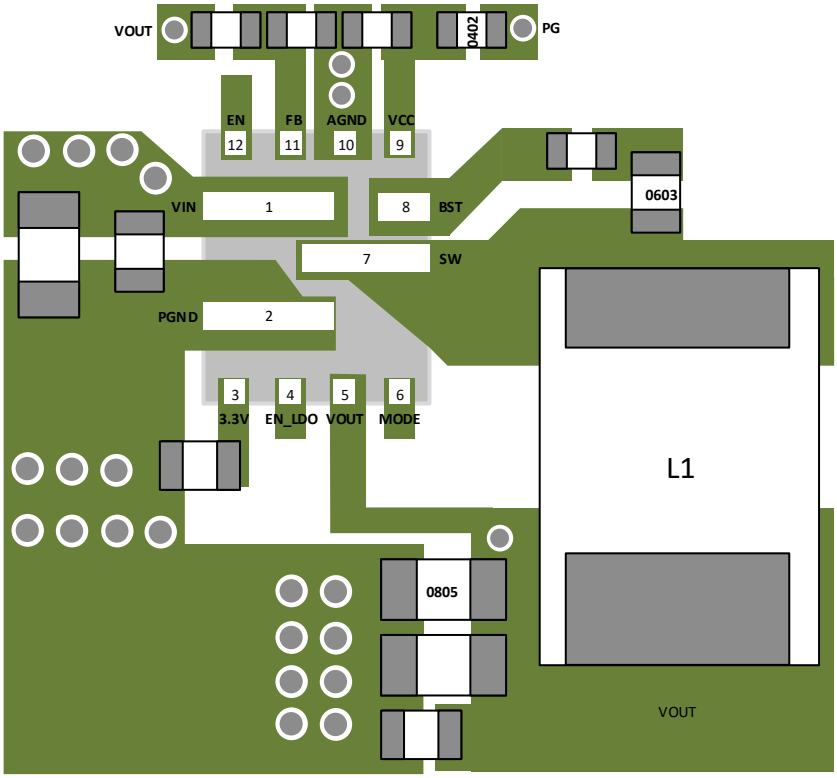
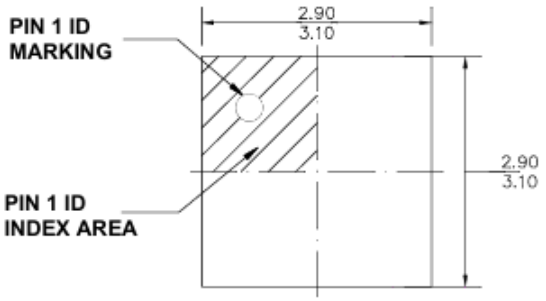


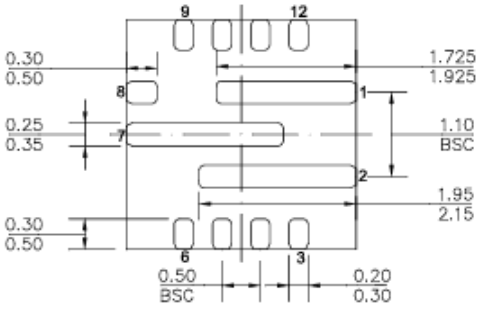

Figure 23. PCB Layout Example

## PACKAGE INFORMATION

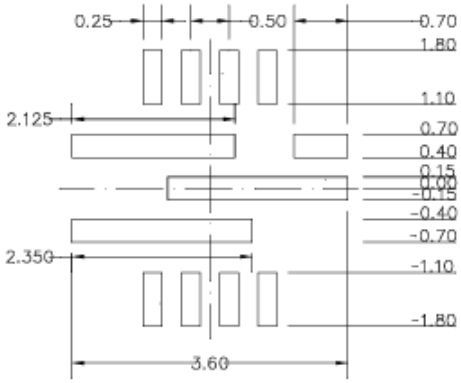



**TOP VIEW**




**BOTTOM VIEW**


**SIDE VIEW**



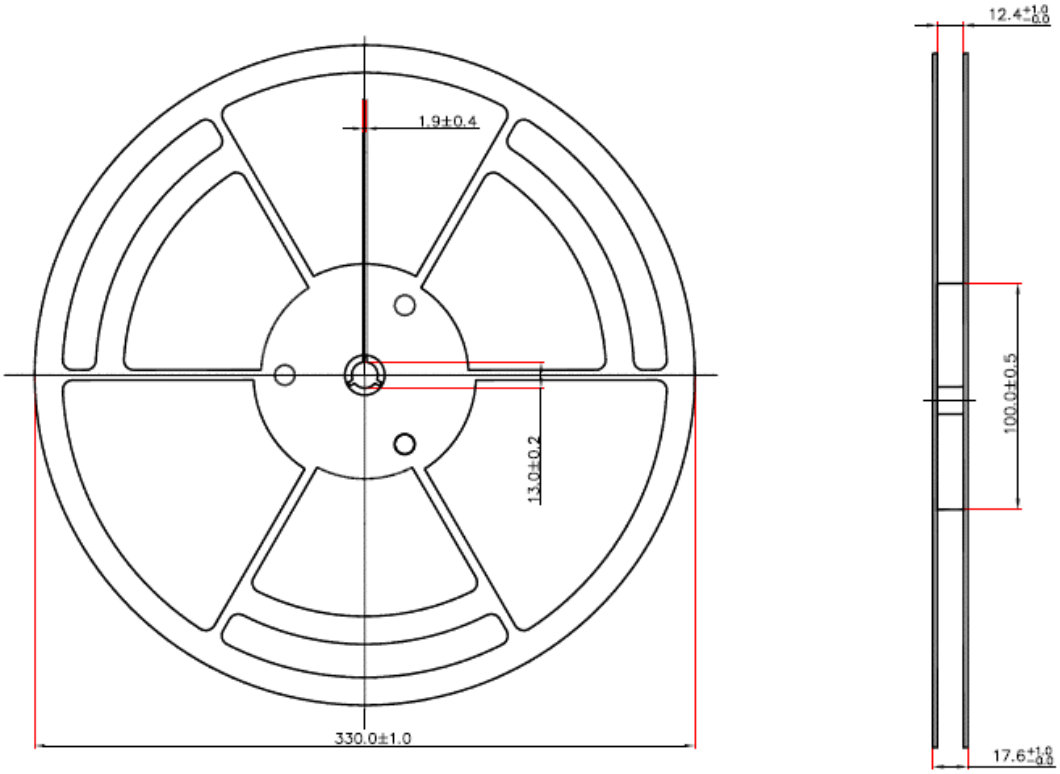

**RECOMMENDED LAND PATTERN**

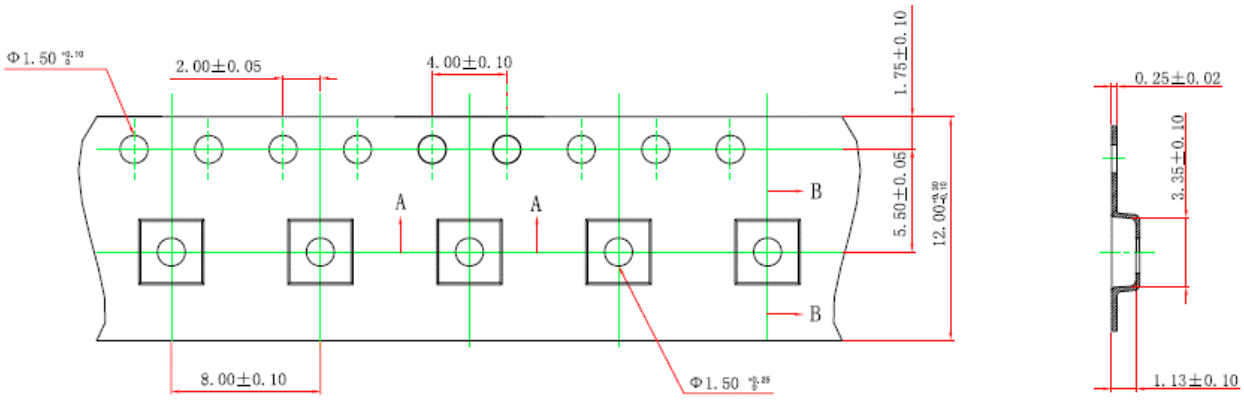
**NOTE:**

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

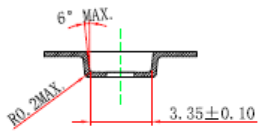
  

## TAPE AND REEL INFORMATION




SECTION B-B




SECTION A-A