3.5V-36V Vin, 10A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Range: 3.5V-36V
- Up to 10A Continuous Output Current
- 1V±1% Feedback Reference Voltage at room temperature
- Integrated 21mΩ High-Side and 13mΩ Low-Side Power MOSFETs
- 0.8uA Quiescent Current with BIAS Connected to an auxiliary power supply to 5V
- 115ns Minimum On-time
- 3.5ms Internal Soft-start Time
- Adjustable Frequency 200kHz to 2.2MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- External BIAS for improved efficiency
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Parallel input path to minimize switch node ringing
- Low Dropout Function and Minimum On Time Function
- Power Good Indicator
- Over-voltage and Over-Temperature Protection
- Available in 4mm*4mm FCQFN-24L Package with wettable flanks

APPLICATIONS

- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies
- Large Cleaning Robot

DESCRIPTION

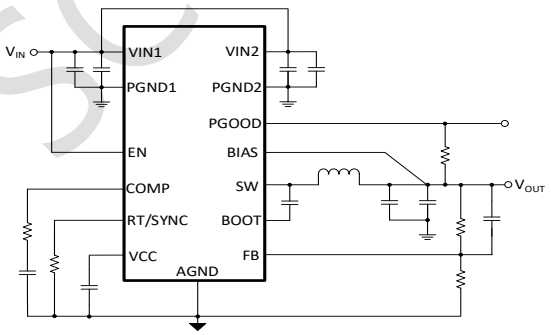
The SCT24A0 is 10A synchronous buck converters with wide input voltage, ranging from 3.5V to 36V, which integrates a 21mΩ high-side MOSFET and a 13mΩ low-side MOSFET. The SCT24A0, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 0.8uA (BIAS=5V) low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT24A0 features adjustable switching frequency from 200kHz to 2.2MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 200kHz to 2.2MHz. The SCT24A0 integrates LDO function and minimum on time function, so it can support normal operation within a wide range of duty cycles.

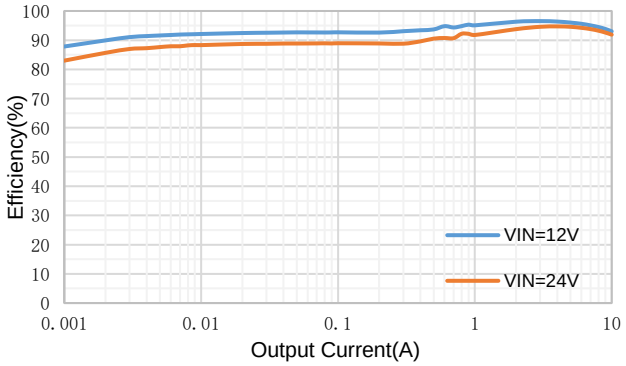
The SCT24A0 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT24A0 features Frequency Spread Spectrum FSS use a pseudorandom frequency hopping with ±4% jittering span of the switching frequency to reduce the conducted EMI.

The SCT24A0 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in 4mm*4mm FCQFN-24L package with wettable flanks.

TYPICAL APPLICATION



3.5V-36V, Synchronous Buck Converter



Efficiency, F_{SW}=400kHz, BIAS=V_{OUT}=5V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer Samples.

Revision 0.81: Update relevant parameters based on the latest batch test data.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT24A0FDAR	Tape & Reel	5000	24A0	24	FCQFN4x4-24L	TBD

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN1, VIN2 (2)	-0.3	42	V
EN	-0.3	42	V
BST	-0.3	47.5	V
SW	-1	42	V
SW(<10ns) (3)	-3	42	V
BST-SW	-0.3	5.5	V
BIAS, PGOOD	-0.3	16	V
VCC, FB, RT, COMP	-0.3	5.5	V
Operating junction temperature TJ (4)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Function Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

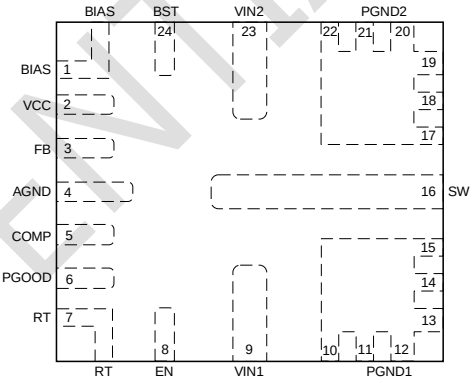


Figure 1. 24-Lead FCQFN 4mm×4mm

(Sketch Map)

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BIAS	1	Input to internal LDO. Connect to output voltage point to improve efficiency. Connect an optional high quality 0.1-μF to 1-μF capacitor from this pin to ground for improved noise immunity.
VCC	2	Internal LDO output. Used as supply to internal control circuits. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
FB	3	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1V typical.
AGND	4	Analog ground.
COMP	5	Error amplifier output. Connect to frequency loop compensation network.
PGOOD	6	Power good open-drain output. PGOOD is high if the output voltage is higher than 90% and lower than 112% of the nominal voltage.

RT	7	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set the switching frequency between 200kHz and 2.2MHz. An external clock can be input directly to this pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the function mode automatically returns to resistor adjusted frequency.
EN	8	Enable pin to the regulator with internal pull-up current source. Pull below 0.93V to disable the converter, pull to 1.26V or above to start the converter. Can be connected to VIN. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN1	9	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
PGND1	10-15	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	16	Regulator switching output. Connect SW to an external power inductor.
PGND2	17-22	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	23	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
BST	24	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT}	Output voltage range	1	16	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	PIN	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM)	SW	-1.5	1.5	kV
		Others	-2	2	
	Charged Device Model (CDM)	All	-1	1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCQFN-24L	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	36.32	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	1.55	
Ψ_{JB} (2)	Junction-to-board characterization parameter	2.47	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	24.27	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	2.59	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	24.67	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	0.9	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT24A0 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT24A0. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual RθJA and RθJC.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(3) Measured on SCT standard EVM: SCT24A0 Demo Board, 1oz copper thickness, 75mm x 65mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.5		36	V
I_{SHDN}	Shutdown current from VIN pin	EN=0, V_{FB}=1.05V		0.6	4	μA
I_{Q_BIAS}	Quiescent current from VIN pin	V_{EN}=12V, V_{FB}=1.05V, V_{BIAS}=5V		0.8	5	μA
I_Q	Quiescent current from VIN pin	V_{EN}=12V, V_{FB}=1.05V		36	50	μA
I_{BIAS}	Quiescent Current into BIAS pin	V_{FB}=1.05V, V_{EN}=12V, V_{BIAS}=5V		36	50	uA
VCC LDO and BIAS						
V_{CC}	V_{CC} voltage at CCM-mode	V_{FB}=0.8V		4.2		V
	V_{CC} voltage at non-switching	V_{FB}=1.05V		4		
V_{CC_UVLO}	V_{CC} UVLO Threshold	V_{CC} rising		3.25	3.48	V
	Hysteresis			400		mV
V_{BIAS_rising}	BIAS voltage rising, V_{CC} power switch to BIAS			4.6		V
$V_{BIAS\_falling}$	BIAS voltage falling, V_{CC} power switch back to V_{IN}			4.2		V
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance			21		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			13		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	0.99	1	1.01	V
		Tj=-40°C~125 °C	0.98		1.02	V
G_{EA}	Error amplifier trans-conductance			36		μS
I_{COMP_SRC}	EA maximum source current	V_{FB}=0V, V_{COMP}=2V		5		μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=2V, V_{COMP}=0.53V		5		μA
V_{COMP_H}	COMP high voltage			2		V
V_{COMP_L}	COMP low voltage			0.53		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit		10.5	16	22.5	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit		9	12	18	A
I_{ROC}	Low-side reverse current limit			6		A
V_{Hiccup}	Hiccup trigger threshold voltage on FB pin			0.4		V
t_{Hiccup_delay}	Delay time of Hiccup trigger			128		cycle
t_{Hiccup}	Hiccup protection time			40		ms
$I_{PEAK\_PSM\_0}$	I_{PEAK} at PSM mode and duty is closing to 0%			1.6		A
$I_{PEAK\_PSM\_100}$	I_{PEAK} at PSM mode and duty is closing to 100%			0.6		A

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Enable and Soft Startup						
V_{EN_WAKE}	EN_wake threshold when VCC-LDO start-up			0.7		V
$V_{EN\_OK\_rising}$	EN-OK threshold rising			1.26	1.4	V
$V_{EN\_OK\_falling}$	EN-OK threshold falling		0.75	0.93		V
$V_{EN\_OK\_HYST}$	EN-OK threshold hysteresis			0.33		V
I_{EN}	EN pin input current	$V_{EN}=V_{IN}=12V$			200	nA
t_{SS}	Internal soft start time			3.5		ms
t_{SS2}	Time from first SW pulse to release of hiccup lockout if output not in regulation			6.8		ms
Switching Frequency and External Clock Synchronization						
F_{RANGE_RT}	Frequency range using RT mode		200		2200	kHz
F_{SW}	Switching frequency	R_{RT}=40.2 kΩ (1%)	380	400	420	kHz
F_{SW}	Switching frequency	R_{RT}=6.8 kΩ (1%)	2	2.2	2.4	MHz
F_{RANGE_CLK}	Frequency range using CLK mode		200		2200	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±4		%
V_{SYNC_H}	RT input voltage of high level				3	V
V_{SYNC_L}	RT input voltage of low level		0.7			V
t_{ON_MIN}	Minimum on-time			115		ns
t_{OFF_MIN}	Minimum off-tion			250		ns
t_{LDO}	Maximum on time in LDO mode			10		us
Power Good						
V_{PG_UV}	PGOOD flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		90		%
		POWER BAD (% of FB voltage)		87		%
V_{PG_OV}	PGOOD flag over voltage tripping threshold	POWER BAD (% of FB voltage)		112		%
		POWER GOOD (% of FB voltage)		109		%
V_{IN_PG}	Input voltage for proper PGOOD function			1.2		V
V_{PG_LOW}	PGOOD low level output voltage	$I_{Pull-Up}$ = 1 mA		0.15		V
$t_{PG\_H\_DLY}$	Delay time to PGOOD high signal			2.2		ms
$t_{PG\_Deglitch}$	PGOOD OV and UV glitch filter time			27		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		112		%
		V_{FB}/V_{REF} falling		109		%
V_{BST_UV}	BST-SW UVLO Threshold	BST-SW voltage		2.5		V
T_{SD}*	Thermal shutdown threshold	T_J rising		168		°C
		Hysteresis		8		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

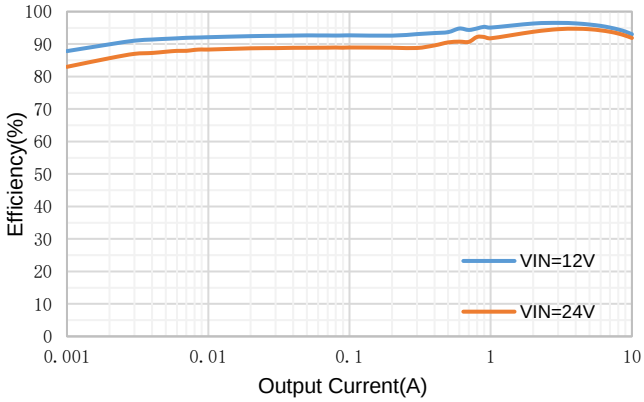


Figure 2. Efficiency, F_{SW}=400kHz, BIAS=V_{OUT}=5V

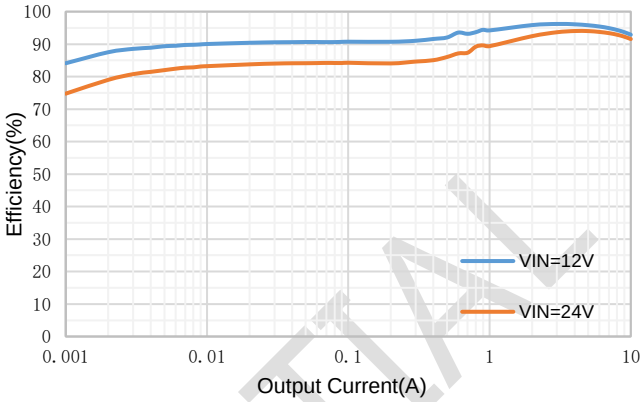


Figure 3. Efficiency, F_{SW}=400kHz, V_{OUT}=5V

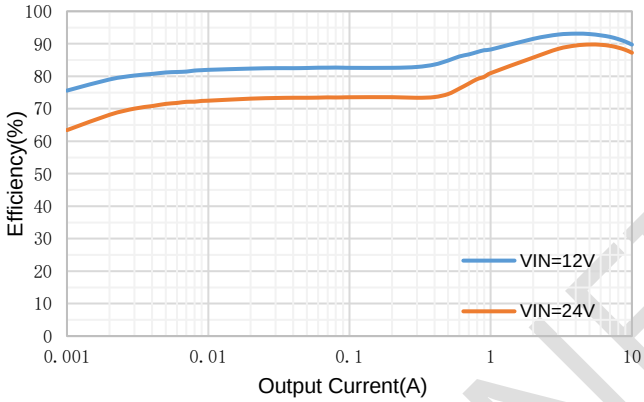


Figure 4. Efficiency, F_{SW}=400kHz, V_{OUT}=3.3V

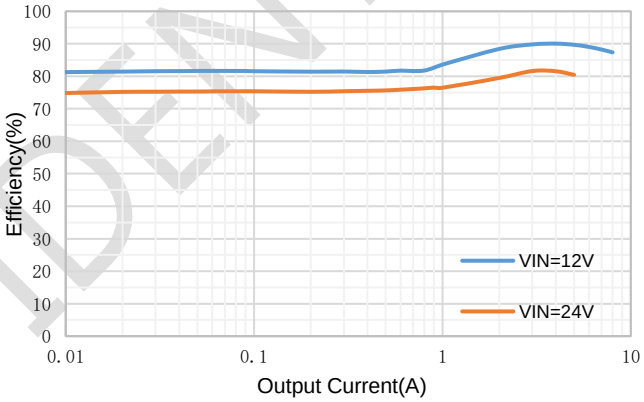


Figure 5. Efficiency, F_{SW}=2.2MHz, BIAS=V_{OUT}=5V

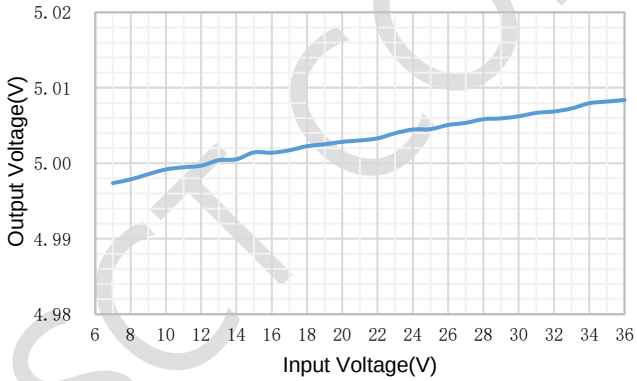


Figure 6. Line Regulation (V_{OUT}=5V, I_{LOAD}=5A)

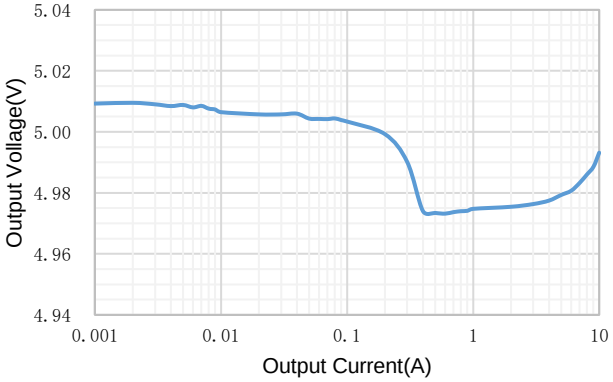


Figure 7. Load Regulation (V_{IN}=12V, V_{OUT}=5V)

TYPICAL CHARACTERISTICS

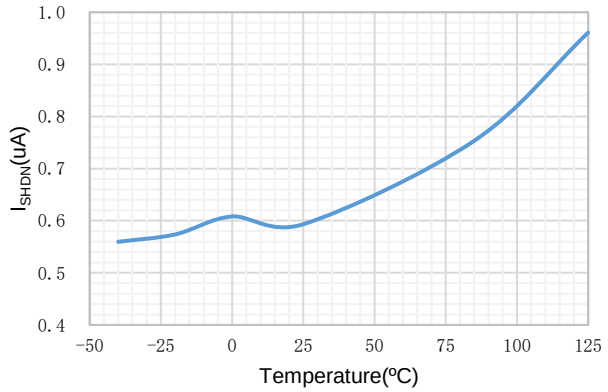


Figure 8. Shutdown Current VS Temperature

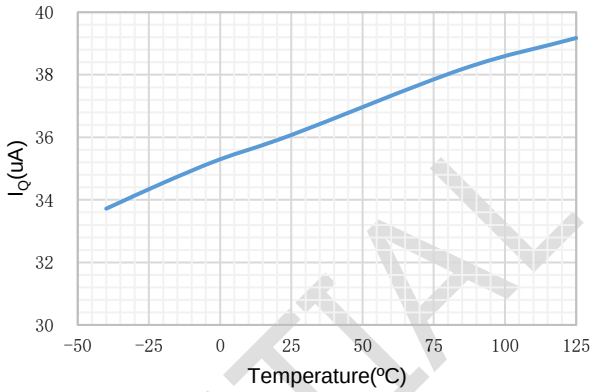


Figure 9. Quiescent Current VS Temperature

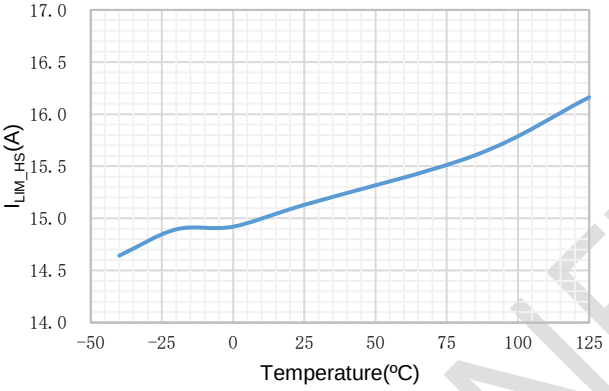


Figure 10. HS Current Limit VS Temperature

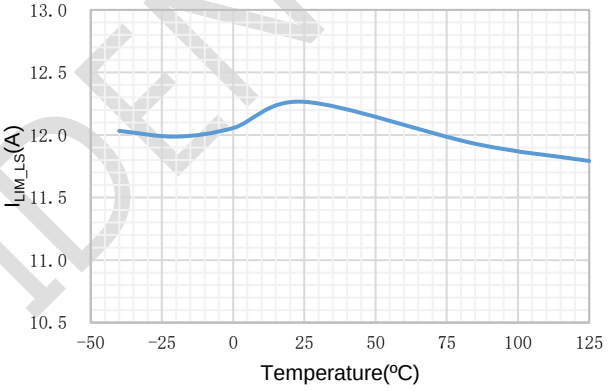


Figure 11. LS Current Limit VS Temperature

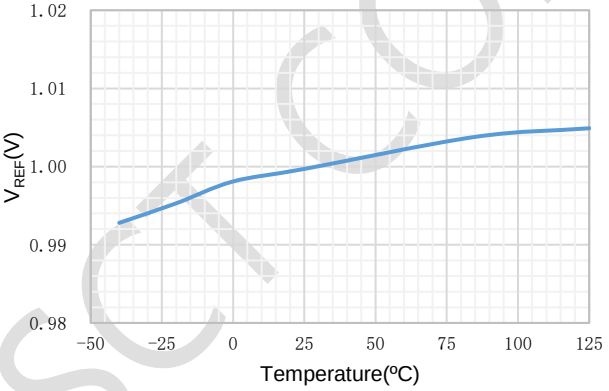


Figure 12. Reference voltage VS Temperature

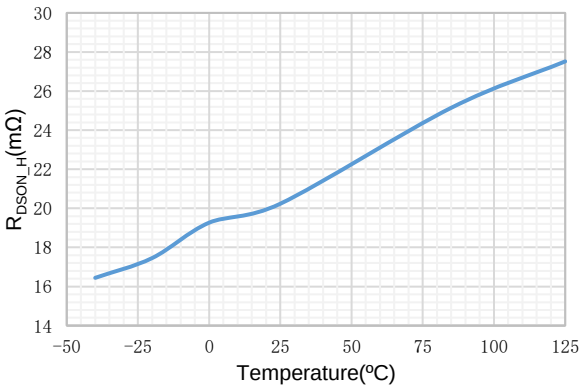


Figure 13. HS R_{DSON} VS Temperature

FUNCTIONAL BLOCK DIAGRAM

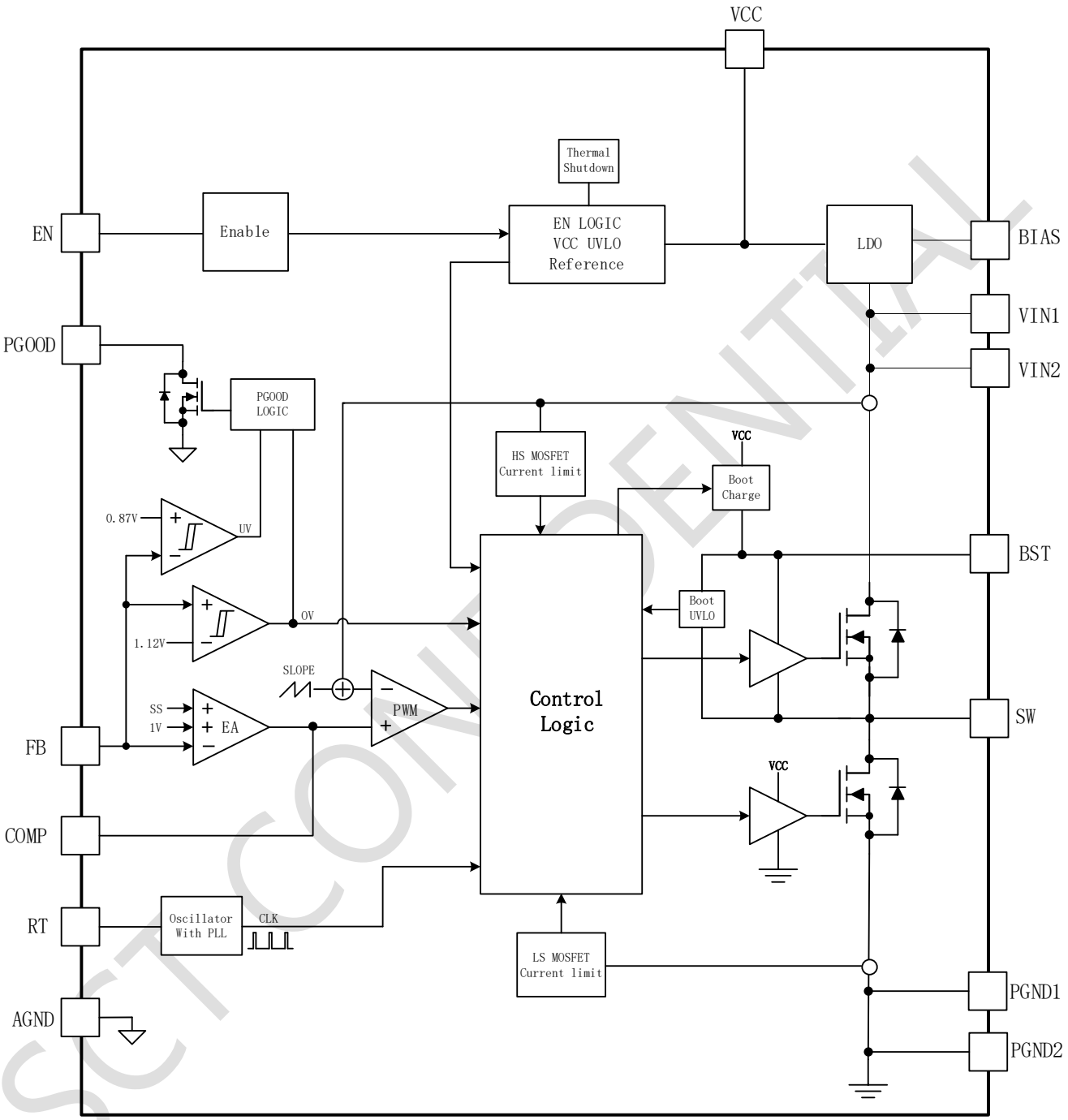


Figure 14. Functional Block Diagram

FUNCTION

Overview

The SCT24A0 is a 3.5V-36V input, 10A output, EMI friendly synchronous buck converter with built-in 21mΩ Rdson high-side and 13mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 2.2MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT24A0 features an internal 3.2ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The mode-transition between PWM mode and PSM mode functions ensure high efficiency over wide load current range. The quiescent current is typically 1uA (V_{BIAS}=5V) under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Connecting EN pin to VIN directly starts up the device automatically.

The SCT24A0 implements the Frequency Spread Spectrum FSS modulation spreading of ±4% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT24A0 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT24A0 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 1.0V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

Pulse Skipping Mode (PSM) Function

The SCT24A0 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (530mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold, then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical I_{peak} inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded. To better reduce power consumption within the full input voltage range, SCT24A0 will correspond to different Ipeak at different input voltages. According to the duty cycle, the minimum value of I_{peak} is 0.6A and the maximum value is 1.6A.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 0.8uA (V_{BIAS}=5V) during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

Start-up and shutdown are controlled by the EN input and VIN UVLO. The SCT24A0 is enabled when the VIN pin voltage rises above 3.5V and the EN pin voltage exceeds the enable threshold of 1.26V. For the device to remain in shutdown mode, apply a voltage below 0.7V to the EN pin. In shutdown mode, the quiescent current drops to 0.6uA (typical). At a voltage above 0.7 and below 1.26V, VCC is active, and the SW node is inactive.

The EN pin cannot be left floating. The EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 15 from VIN to EN. This can be used for sequencing, preventing re-triggering of the device when used with long input cables, or reducing the occurrence of deep discharge of a battery power source. The UVLO threshold can be calculated by Equation 1 respectively.

$$R_1 = \left(\frac{V_{ON}}{V_{EN}} - 1\right) * R_2$$

$$V_{OFF} = V_{ON} * \left(1 - V_{EN\_HYST}\right) \quad (1)$$

Where:

- V_{ON} =V_{IN} turn on voltage
- V_{OFF}=V_{IN} turn off voltage

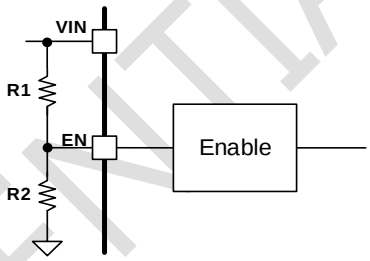


Figure 15. System UVLO by enable divide

Output Voltage

The SCT24A0 regulates the internal reference voltage at 1.0V with ±2% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (2)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft Start and Soft Start Tracking

The SCT24A0 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.0V reference voltage in t_{SS}. Soft start is triggered by any of the following conditions:

• The device is activated through EN or VIN UVLO.

• Recovery from a hiccup waiting period or shutdown due to overtemperature protection.

During soft start, hiccup is disabled. These actions together provide start-up with limited inrush currents and allow the use of larger output capacitors and higher loading conditions that cause current to border on current limit during start-up without triggering hiccup. Hiccup is enabled once output reaches regulation or time exceeds t_{SS2}, whichever happens first.

When the output voltage drops below the set value, the soft start voltage will track the decrease in output voltage in a certain proportion. This situation may occur under the following conditions:

• When the input voltage is too low to maintain the set output voltage.

• When overcurrent occurs causing a decrease in output voltage.

When the above conditions are removed, the output voltage will still increase under soft start. But it should be noted that if the output voltage drops below 40% due to overcurrent, hiccup will be triggered.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT24A0 is set by placing a resistor between RT pin and the ground or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 200kHz to 2.2MHz. RT pin is not allowed to be left floating or shorted to the ground. Use Equation 3 and the plot in Figure 17 to determine the resistance for a switching frequency needed.

$$RT(k\Omega) = \frac{16.4}{f_{SW}(MHz)} - 0.633 \qquad (3)$$

where, f_{SW} is switching clock frequency.

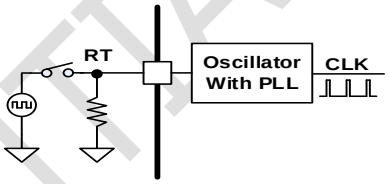


Figure 16. Setting Frequency and Clock Synchronization

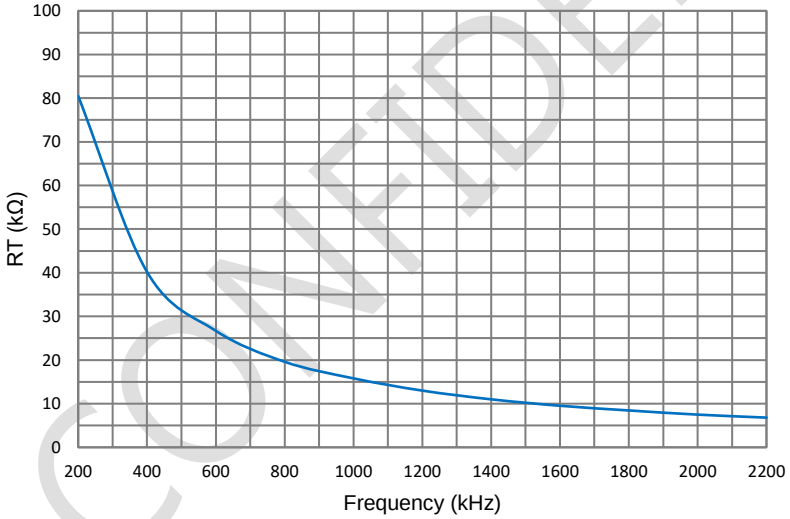


Figure 17. Setting Switching Frequency

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT pin. The synchronization frequency range is from 200kHz to 2.2MHz and the rising edge of the SW synchronizes to the rising edge of the external clock at RT pin with typical 20ns time delay. A square wave clock signal to RT pin must have high level no lower than 3V, low level no higher than 0.7V, and pulse width larger than 100ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 16. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks the internal clock frequency onto the external clock after a delay of no more than 260us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT24A0 implements Frequency Spread Spectrum (FSS). The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than apart with fixed frequency function. In most systems containing the SCT24A0, low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered.

The FSS circuit uses pseudo-random frequency hopping to vary the switching frequency within a specific range. The jittering span is ±4% of the switching frequency. The spread spectrum is only available while the clock of the SCT24A0 devices is free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

• The clock is reduced during LDO function.

• The clock is reduced at light load in PSM.

• The clock is reduced during minimum on time function.

• The clock is synchronized with an external clock.

VCC LDO, VCC UVLO, BIAS

The VCC pin is the output of the internal LDO used to supply the control circuits of the SCT24A0, and its minimum operating voltage is 3.25V. The VCC is powered from VIN or BIAS. The BIAS pin is the input of the internal LDO. This input can be connected to V_{OUT}, or it could be an external voltage source to save the power loss from V_{IN}. If the BIAS voltage is larger than 4.6V, LDO is powered by BIAS pin. If the BIAS voltage is less than 4.2V or the output voltage is not within the POWER GOOD range, VIN1 and VIN2 directly powers the internal LDO. To prevent unsafe function, VCC has a UVLO that prevents switching if the internal voltage is too low.

Bootstrap Voltage Regulator and BST UVLO

An external bootstrap capacitor between BST pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. A boot diode is integrated on the SCT24A0 die to minimize external component count.

The UVLO of high-side MOSFET gate driver has threshold of 2.5V. When the voltage across bootstrap capacitor drops below 2.5V, BST UVLO occurs, the voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's function.

Low Drop-out Function

At a given clock frequency, duty cycle is limited by minimum off time. During the condition of low voltage difference from the input to the output, to maintain the output voltage from falling, the SCT24A0 extends on time past the end of the clock cycle until the required peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a predetermined maximum on time (t_{LDO}) of approximately 10us passes. As a result, to ensure that the output voltage can better follow the changes in input voltage, when SCT24A0 operates in LDO function, the switching frequency begins to decrease, with a minimum decrease to 100kHz. The minimum frequency limit avoids possible audio interference.

During slow power on and power off applications, due to the LDO function, the output voltage can closely track the slope changes of the input voltage. As the input voltage is reduced to near the output voltage, i.e., during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO function mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT24A0 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Minimum On Time Function

Even if the duty cycle at the set frequency is limited by the minimum on time, SCT24A0 can still maintain stable adjustment of the output voltage during the transition from high input voltage to low output voltage.

If the input-output voltage ratio is too high, even if the current exceeds the compensation specified peak, the high side MOSFET cannot shut down quickly enough to adjust the output voltage. This will cause the output voltage to continuously increase until overvoltage protection is triggered. To avoid this situation, when the conduction time of the high side MOSFET touches the minimum on time due to the increase in input and output voltage difference, SCT24A0 will switch to valley current control mode. After the high side MOSFET is turned off, the low side MOSFET will remain open until the inductor current drops below the required valley current. During this period, the next clock cycle will be blocked from starting, so the switching frequency will decrease. Since on time of high side MOSFET is fixed at its minimum value, this type of function resembles that of a device using a Constant On-Time (COT) control scheme.

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT24A0 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the inductor current is clamped at over current limitation, the converter cannot provide output current to satisfy loading requirement. Thus, the output capacitor is discharged, and the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP voltage ramps up to high clamp voltage 2V typical. When FB voltage is below 40% of the reference voltage and after 128 cycles of low side current limit, the converter stops switching. After remaining OFF for 40ms，the device restarts from soft start phase. If overload or hard short condition still exists during t_{SS2} and make COMP voltage clamped at high, after t_{SS2} and FB voltage keep below 40% of the reference voltage for 128 cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating function.

If the FB voltage drops below 40% of the reference voltage due to LDO function, hiccup mode will be disabled.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT24A0 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 112% of internal 1.0V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 109% of the 1.0V reference voltage, the high-side MOSFET can turn on again.

Power Good

The PGOOD pin is an open-drain output. Connect the pin to V_{OUT} or other voltage source through a pull-up resistor between 10kΩ and 100kΩ. Please ensure that the voltage connected to the PGOOD pin does not exceed 16V.

Once the FB pin is between 90% and 109% of the internal voltage reference the PGOOD pin is de-asserted and the pin floats with 2.2ms delay. The PGOOD pin is pulled low when the FB is lower than 87% or greater than 112% of the nominal internal reference voltage with 27us deglitching time. Also, the PGOOD is pulled low if Vin UVLO or thermal shutdown are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 27us deglitching time do not trip the PGOOD flag.

Thermal Shutdown

The SCT24A0 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 168°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

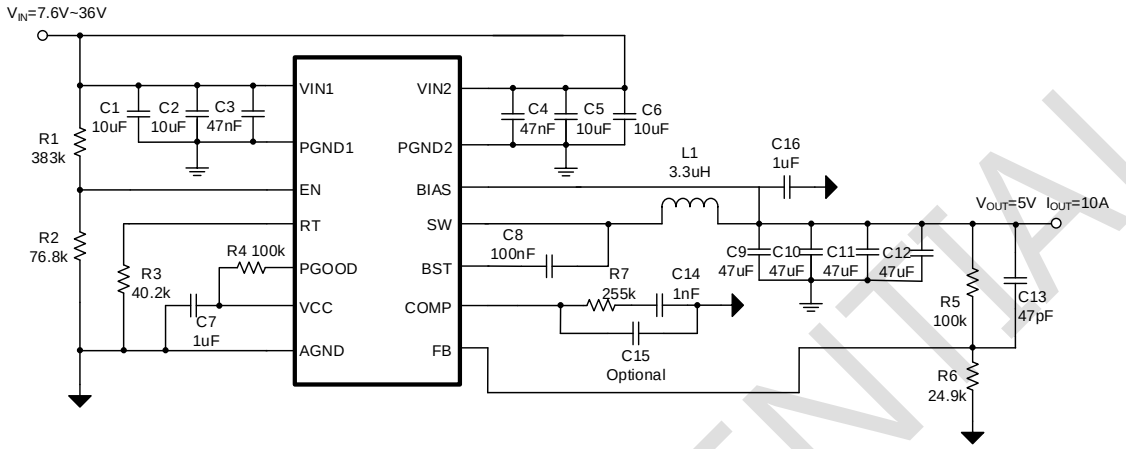


Figure 18. SCT24A0 Design Example, 5V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 7.6V to 36V
Output Voltage	5V
Maximum Output Current	10A
Switching Frequency	400kHz
Output voltage ripple (peak to peak)	5.8mV
Transient Response 2.5A to 8.5A load step	ΔVout = 436mV
Start Input Voltage (rising VIN)	7.6V
Stop Input Voltage (falling VIN)	5.5V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 24.9kΩ. Use Equation 4 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 1V.

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
1.8 V	19.6 kΩ	24.9 kΩ
2.5 V	37.4 kΩ	24.9 kΩ
3.3 V	57.6 kΩ	24.9 kΩ
5 V	100 kΩ	24.9 kΩ
12 V	221 kΩ	20 kΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. In this design, a moderate switching frequency of 400 kHz is selected to achieve both small solution size and high efficiency function.

The resistor connected from RT to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using Equation 5 or determined from Figure 17.

$$R_3(\text{k}\Omega) = \frac{16.4}{f_{SW}(MHz)} - 0.633 \quad (5)$$

where:

- f_{SW} is the desired switching frequency

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_3 (R_{FSW})
200 kHz	80.5 kΩ
400 kHz	40.2 kΩ
800 kHz	19.6 kΩ
1200 kHz	13 kΩ
1700 kHz	9.09 kΩ
2200 kHz	6.81 kΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 7.6V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 5.5V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 383kΩ and 76.8kΩ of R1 and R2 resistors.

$$R_1 = \left(\frac{V_{ON}}{V_{EN}} - 1\right) * R_2 \quad (6)$$

$$V_{OFF} = V_{ON} * \left(1 - V_{EN\_HYST}\right) \quad (7)$$

where:

- V_{ON} is rising threshold of Vin UVLO
- V_{OFF} is falling threshold of Vin UVLO

- V_{EN}=1.26V, V_{EN_HYST}=0.33V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

$$I_{LPP} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*f_{SW}} \quad (8)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW}*LIR*I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (9)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN\ (max)}$ is the maximum input voltage.
- $I_{OUT\ (max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak function current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 10 and Equation 11.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (10)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (11)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 16A. The most conservative approach is to choose an inductor with a saturation current rating greater than 16A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the

SCT24A0 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 12.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (12)$$

The worst-case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (13)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 14 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

For this example, four 10μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper function. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 15 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (15)$$

Where:

- ΔV_{OUT} is the output voltage ripple.

- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- $V_{IN}$is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 47μF ceramic output capacitors work for most applications. If you want to achieve better dynamic response performance, you need to add electrolytic capacitors with larger capacitance values.

Compensation Components

The SCT24A0 employs peak current mode control for easy compensation and fast transient response. An external network comprising resister R7, ceramic capacitors C14 and optional C15 connected to the COMP pin is used for the loop compensation. The Equation16 shows the close-loop small signal transfer function.

$$H(S)=\left[A_{EA}*\frac{1+\frac{S}{2\pi*f_{Z1}}}{\left(1+\frac{S}{2\pi*f_{P1}}\right)*\left(1+\frac{S}{2\pi*f_{P3}}\right)}\right]*\left[G_{ISNS}*\frac{V_{OUT}}{I_{OUT}}*\frac{1+\frac{S}{2\pi*f_{Z2}}}{1+\frac{S}{2\pi*f_{P2}}}\right]*\frac{V_{FB}}{V_{OUT}} \quad (16)$$

Where:

- A_{EA} is error amplifier voltage gain.
- G_{ISNS} is COMP to SW current trans-conductance, 15.6A/V typically.

The DC voltage gain of the loop is given by Equation 17.

$$A_{VDC}=A_{EA}*G_{ISNS}*\frac{V_{FB}}{I_{OUT}} \quad (17)$$

The system has two noteworthy poles: one is due to the compensation capacitor C14 and the error amplifier output resistor. The other is caused by the output capacitor and the load resistor. These poles as located at:

$$f_{P1}=\frac{1}{2\pi*R_{OEA}*C_{14}}=\frac{G_{EA}}{2\pi*A_{EA}*C_{14}} \quad (18)$$

$$f_{P2}=\frac{1}{2\pi*R_{LOAD}*C_{OUT}}=\frac{I_{OUT}}{2\pi*V_{OUT}*C_{OUT}} \quad (19)$$

Where:

- R_{OEA} is error amplifier output resistor.
- G_{EA} is Error amplifier trans-conductance, 36uS typically.
- R_{LOAD} is equivalent load resistor.

The system has one zero of importance from R7 and C14. fz1 is used to counteract the fp2, and fz1 located at:

$$f_{Z1}=\frac{1}{2\pi*C_{14}*R_7} \quad (20)$$

The system may have another important zero if the output capacitor has a large capacitance or a high ESR value. The zero, due to the ESR and the capacitance of the output capacitor is calculated by Equation 21.

$$f_{Z2}=\frac{1}{2\pi*C_{OUT}*ESR} \quad (21)$$

In this case, a third pole set by the optional compensation capacitor C15 and the compensation resistor R7 is used to compensates the effect of the ESR zero. This pole is calculated by Equation 22.

$$f_{P3} = \frac{1}{2\pi * C_{15} * R_7} \quad (22)$$

The crossover frequency of converter is shown in Equation 23.

$$f_C = \frac{V_{FB}}{V_{OUT}} * \frac{G_{EA} * G_{ISNS} * R_7}{2\pi * C_{OUT}} \quad (23)$$

The system crossover frequency, where the feedback loop has unity gain, is important. A lower crossover frequency results in slower line and load transient response. A higher crossover frequency could cause the system unstable. A recommended rule of thumb is to set the crossover frequency to be approximately 1/10 of switching frequency.

The following steps can be followed to calculate the external compensation components. Calculate the compensation resistor R7 with Equation 24 once crossover frequency is selected.

$$R_7 = \frac{V_{OUT}}{V_{FB}} * \frac{2\pi * C_{OUT} * f_C}{G_{EA} * G_{ISNS}} \quad (24)$$

Then calculate C14 by placing a compensation zero at or before the output stage pole.

$$C_{14} = \frac{R_{LOAD} * C_{OUT}}{R_7} \quad (25)$$

Determine if the optional compensation capacitor C15 is required. Generally, it is required if the ESR zero fz2 is located less than half of the switching frequency. Then fp3 can be used to cancel fz2. C15 can be calculated with Equation 26.

$$C_{15} = \frac{C_{OUT} \times ESR}{R_7} \quad (26)$$

Table 3 lists typical values of compensation components for some standard output voltages with various output ceramic capacitors and inductors. The values of the compensation components have been optimized for fast transient responses and good stability. For the conditions do not list in Table 3, customers can use Equation 24-Equation 26 to optimize the compensation components.

Table 3: Typical External Component Values

VOUT	FREQUENCY	R5	R6	R3	L1	R7	C14	C15	C13
3.3V	400kHz	57.6 kΩ	24.9 kΩ	40.2 kΩ	2.2uH	255 kΩ	1 nF	/	47 pF
3.3V	2200kHz	57.6 kΩ	24.9 kΩ	6.81 kΩ	0.56uH	499 kΩ	470 pF	/	68 pF
5V	400kHz	100 kΩ	24.9 kΩ	40.2 kΩ	3.3uH	255 kΩ	1 nF	/	47 pF
5V	2200kHz	100 kΩ	24.9 kΩ	6.81 kΩ	0.68uH	499 kΩ	470 pF	/	68 pF
12V	400kHz	274 kΩ	24.9 kΩ	40.2 kΩ	5.6uH	400 kΩ	500 pF	/	10 pF

Application Waveforms

V_{IN}=12V, V_{OUT}=5V, F_{SW}=400k, unless otherwise noted

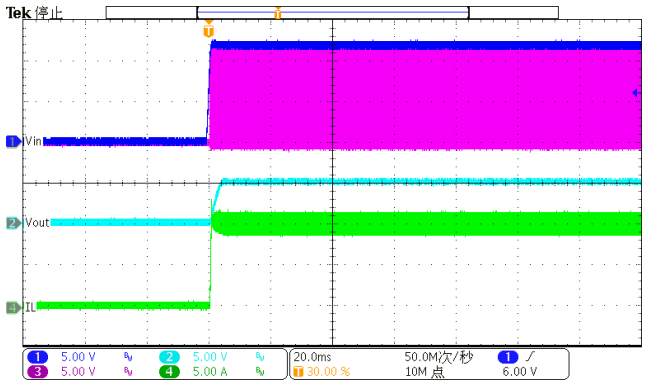


Figure 19. Power up (I_{LOAD}=10A)

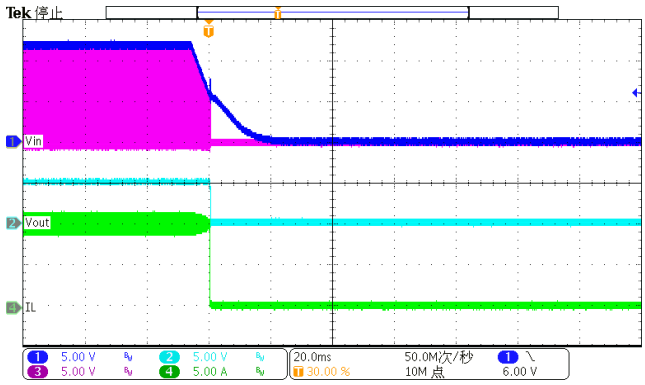


Figure 20. Power down (I_{LOAD}=10A)

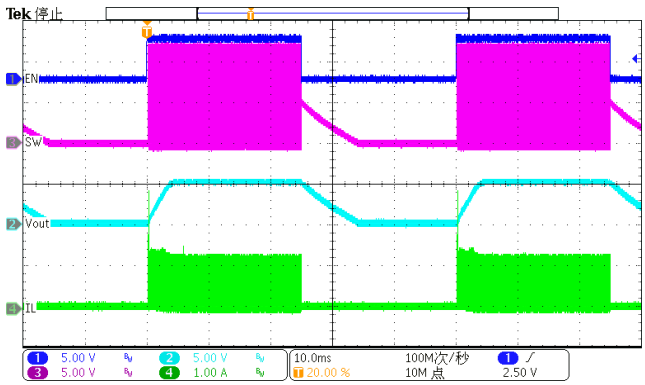


Figure 21. EN toggle (I_{LOAD}=0.1A)

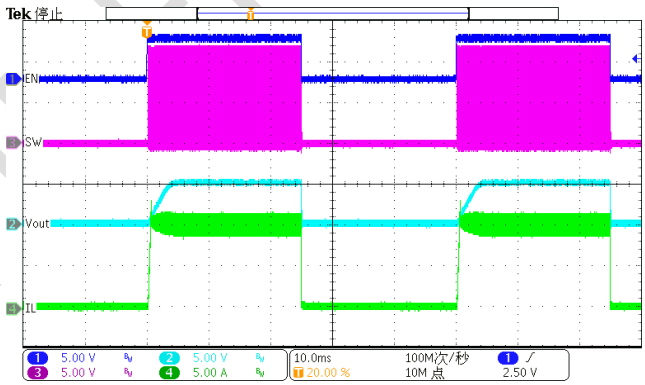


Figure 22. EN toggle (I_{LOAD}=10A)

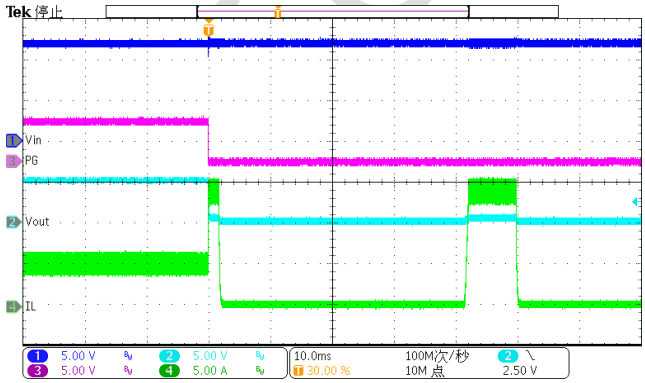


Figure 23. Over Current Protection (5A to hard short)

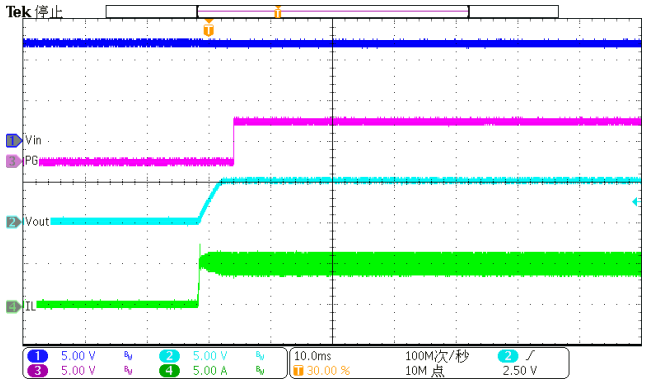


Figure 24. Over Current Release (hard short to 5A)

Application Waveforms

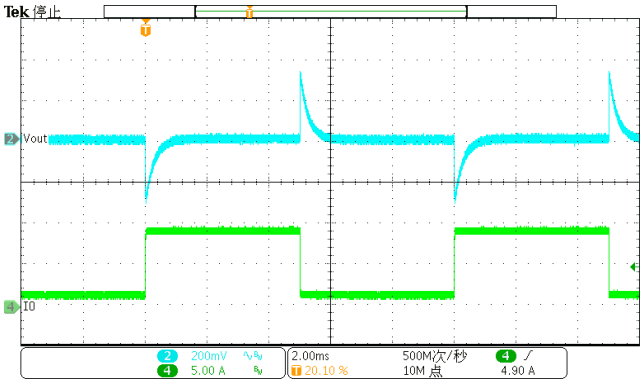


Figure 25. Load Transient (1A~9A, 1.6A/us)

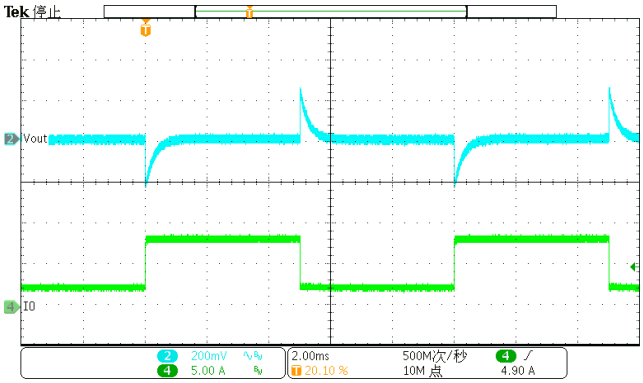


Figure 26. Load Transient (2A~8A, 1.6A/us)

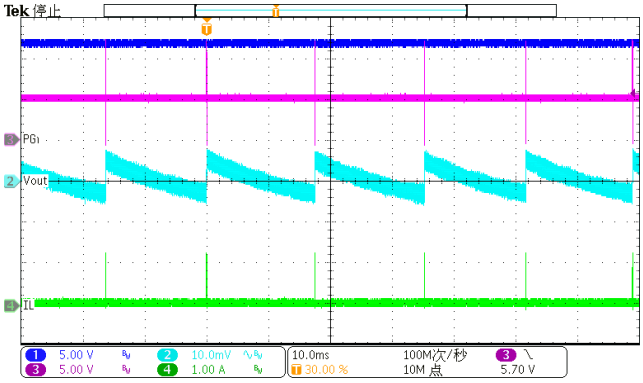


Figure 27. Output Ripple (I_{LOAD}=0A)

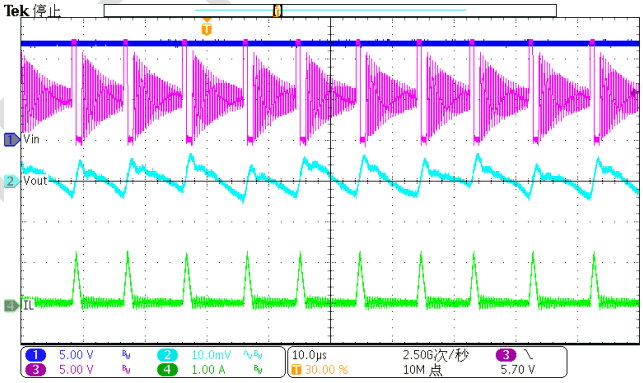


Figure 28. Output Ripple (I_{LOAD}=0.1A)

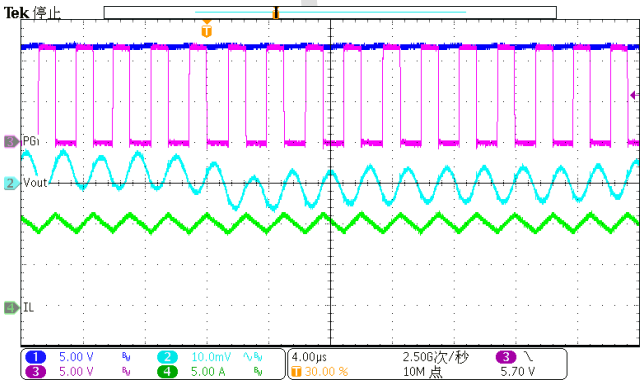


Figure 29. Output Ripple (I_{LOAD}=10A)

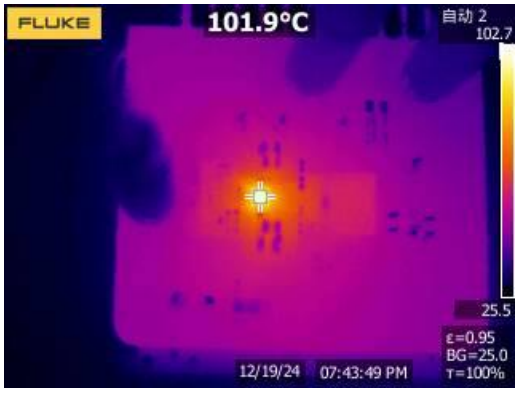


Figure 30. Thermal, 12V_{IN}, 5V_{OUT}, 10A

Layout Guideline

Proper PCB layout is a critical for SCT24A0's stable and efficient function. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The RT terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
5. UVLO adjust and RT resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. For achieving better thermal performance, a four-layer layout is strongly recommended.

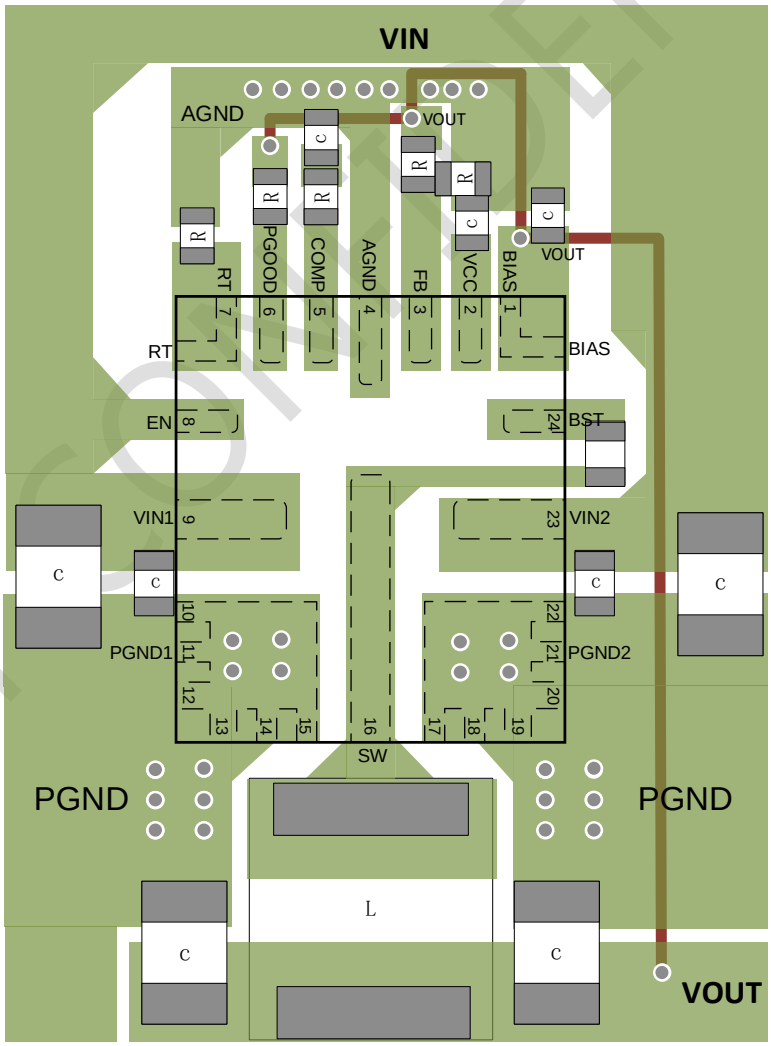
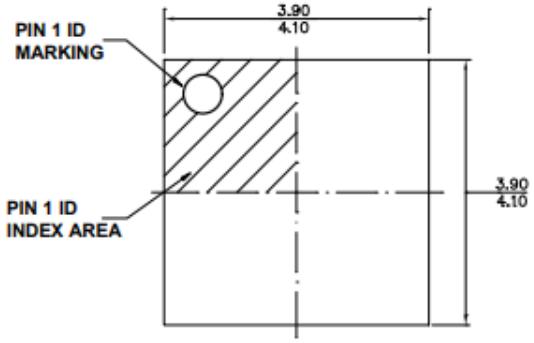
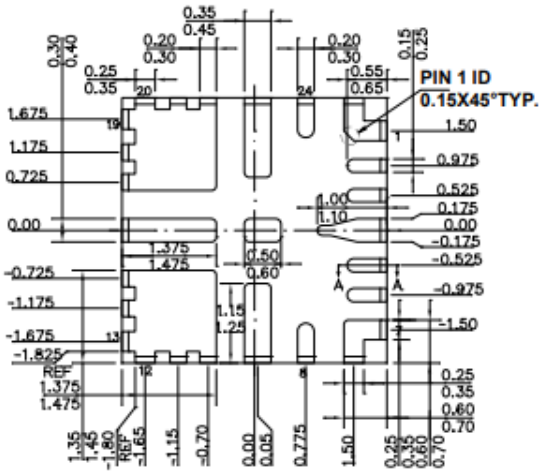


Figure 31. PCB Layout Example (Sketch Map)

PACKAGE INFORMATION

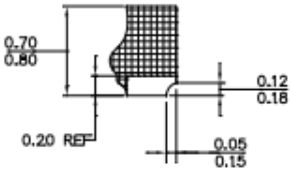


TOP VIEW

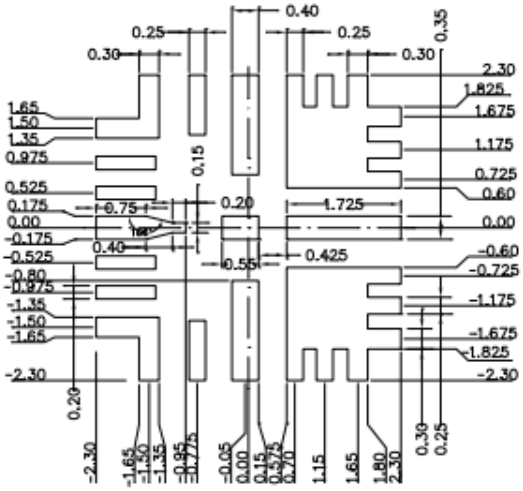


BOTTOM VIEW

SIDE VIEW



SECTION A-A

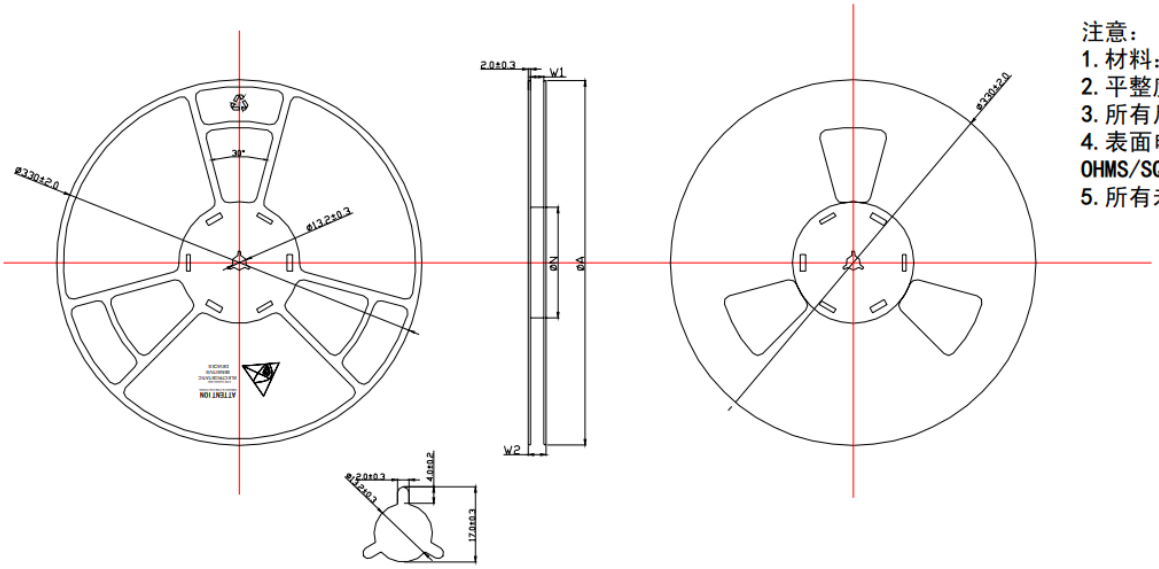


RECOMMENDED LAND PATTERN

NOTE:

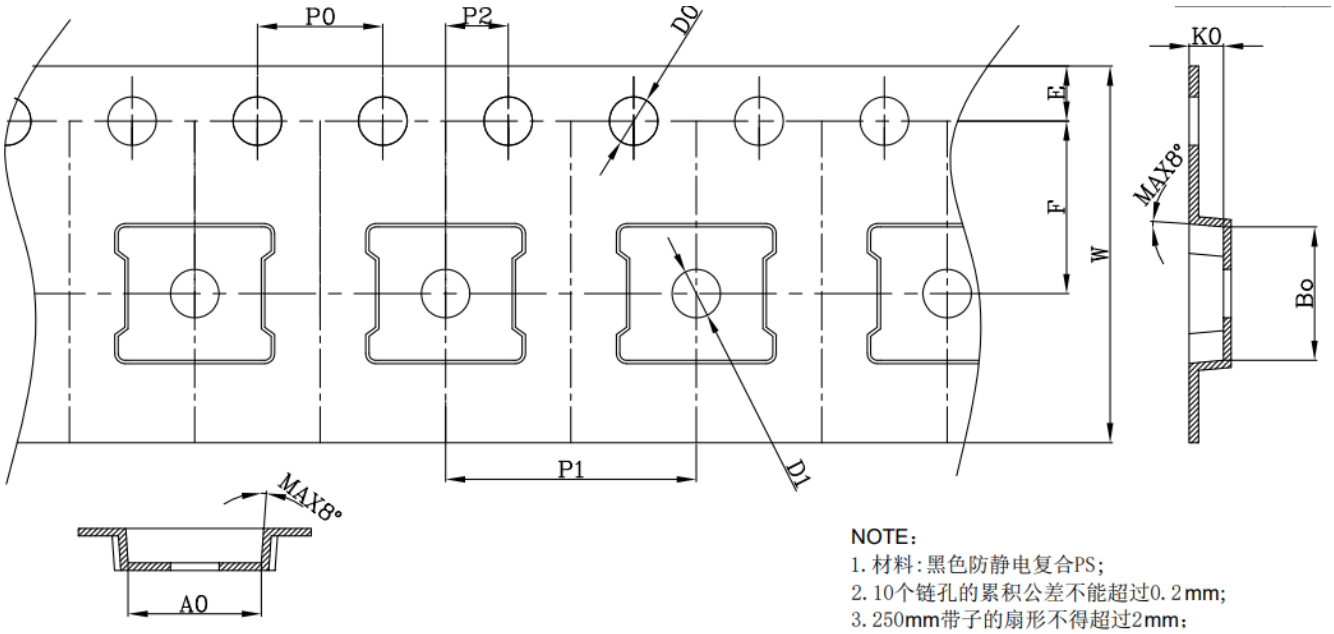
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



注意：
1. 材料：聚苯乙烯；
2. 平整度：最大允许3毫米；
3. 所有尺寸为毫米；
4. 表面电阻：10E5~10E11 OHMS/SQ以下
5. 所有未标注公差：±0.5

PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4



NOTE：
1. 材料：黑色防静电复合PS；
2. 10个链孔的累积公差不能超过0.2mm;
3. 250mm带子的扇形不得超过2mm；
4. 所有尺寸符合EIA-481-E的要求。

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	4.30±0.10	4.30±0.10	1.10±0.10	4.00±0.10	8.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.30±0.05	1.75±0.10	5.50±0.05	1.55±0.05	1.55±0.10	12.00±0.30