4.4V-80V Vin, 2A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Voltage Range: 4.4V-80V
- Continuous Output Current: 2A
- 1V±1% Feedback Reference Voltage at 25°C
- Integrated MOSFETs 270mΩ / 120mΩ Rdson
- Low shutdown current: 0.6uA
- Low Quiescent Current: 36uA
- Pulse Skipping Mode (PSM) in Light-Load
- Adjustable Frequency 200kHz to 1.5MHz
- External Clock Synchronization
- 3.5ms Internal Soft-start Time
- Power Good Indicator
- Random Spread Spectrum option for reduced EMI
- Low Dropout and Minimum On Time Function
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Support start-up with pre-biased output
- Over-voltage and Over-Temperature Protection
- FCTQFN2.5*3-11L Package

APPLICATIONS

- Industrial transportation
- Wireless infrastructure and networking
- Factory automation and control
- Electric bicycles and Electric scooters

DESCRIPTION

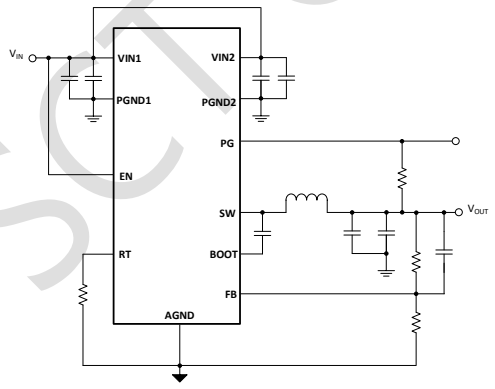
The SCT2821 is 2A synchronous buck converters with wide input voltage, ranging from 4.4V to 80V, which integrates a 270mΩ high-side MOSFET and a 120mΩ low-side MOSFET. The SCT2821, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 36uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2821 features an internal 3.5ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency can be adjusted from 200kHz to 1.5MHz. The SCT2821 integrates LDO function and minimum on time function, so it can support normal operation within a wide range of duty cycles.

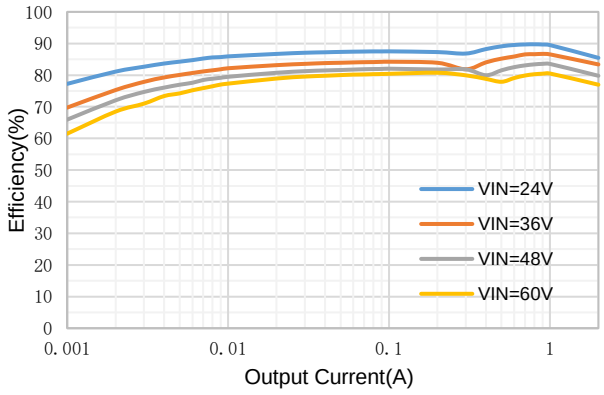
The SCT2821 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2821 features Frequency Spread Spectrum FSS uses a pseudorandom frequency hopping with ±8% jittering span of the switching frequency to reduce the conducted EMI.

The SCT2821 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in FCTQFN2.5*3-11L package.

TYPICAL APPLICATION



4.4V-80V, Synchronous Buck Converter



Efficiency, F_{SW}=400kHz, V_{OUT}=5V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer Samples.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2821FQCR	Tape & Reel	5000	2821	11	FCTQFN 2.5*3-11L	TBD

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN (2)	-0.3	85	V
BOOT	-0.3	91	V
SW	-0.3	85	V
SW (<10ns) (3)	-3	85	V
BOOT-SW	-0.3	6	V
FB, RT	-0.3	6	V
PG	-0.3	20	V
Operating junction temperature TJ (4)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

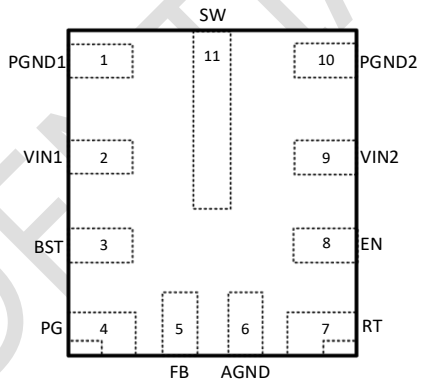


Figure 1. 11-Lead FCTQFN 2.5mm*3mm

(Sketch Map)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PGND1	1	Internal power ground. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
VIN1	2	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
BST	3	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
PG	4	Open-drain power-good flag output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. The flag pulls low when EN = low. It can be left open when not used.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1V typical.
AGND	6	Analog ground. Single point connection to PGND or system ground.

RT	7	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stop, the operation mode automatically returns to resistor programmed frequency.
EN	8	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold. Do not float.
VIN2	9	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
PGND2	10	Internal power ground. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
SW	11	Regulator switching output. Connect SW to an external power inductor.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.4	80	V
V_{OUT}	Output voltage range	1	40	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-3	3	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (2)	-1	1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCTQFN2.5*3-11L	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	TBD	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	TBD	
Ψ_{JB} (2)	Junction-to-board characterization parameter	TBD	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	TBD	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	TBD	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	TBD	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	TBD	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2821 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT2821. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(3) Measured on SCT standard EVM: SCT2821 Demo Board, Outer layer 1oz and inner layer 0.5oz copper thickness, 75mm x 65mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.4		80	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		3.55	4.4	V
	Hysteresis			300		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V		0.6	2	μA
I_Q	Quiescent current from VIN pin	EN=3.3V, non-switching, BOOT-SW=5V		36	60	μA
I_{Active_EVM}*	Active current from VIN pin	V_{IN}=48V, EN=5V, V_{OUT}=5V, no-load		45		uA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=4.2V		270		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			120		mΩ
Reference						
V_{REF}	Reference voltage of FB	T_J=25°C	0.99	1	1.01	V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		2.8	3.2	3.5	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold	T_J=25°C	2	2.3	2.6	A
		T_J=-40°C~125°C	1.8		2.8	A
I_{ZC}	Zero cross detector threshold			20		mA
V_{Hiccup}	Hiccup trigger threshold voltage on FB pin			0.375		V
t_{Hiccup_delay}	Delay time of Hiccup trigger			256		cycle
t_{Hiccup_wait}	Hiccup protection turn-off time			68		ms
I_{PEAK_MIN}	Minimum inductor peak current at PSM mode			0.5		A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.25	1.5	V
V_{EN_L}	Enable low threshold		0.85	1.1		V
$V_{EN\_WAKE\_H}$	Internal logic wake-up voltage			0.79	1.1	V
$V_{EN\_WAKE\_L}$	Internal logic shutdown voltage		0.32	0.66		V
t_{SS}	Internal soft start time			3.5		ms
t_{SS2}	Time from first SW pulse to release of hiccup lockout if output not in regulation			11.5		ms
Switching Frequency and External Clock Synchronization						
F_{SW}	Switching frequency	T_J=25°C	200		1500	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±8		%
V_{SYNC_H}	RT input voltage of high level				2.75	V
V_{SYNC_L}	RT input voltage of low level		0.45			V
t_{ON_MIN}*	Minimum on-time			160		ns

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
t_{OFF_MIN}*	Minimum off-time			250		ns
t_{LDO}*	Maximum on time in LDO mode			12		us
Power Good						
V_{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		89		%
		POWER BAD (% of FB voltage)		87		%
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		112		%
		POWER GOOD (% of FB voltage)		110		%
V_{PG_LOW}	Power-good low level output voltage	IPull-Up = 1 mA		85		mV
t_{PG_delay}	Delay time of Power-good signal			50		us
R_{PG}	Power-Good on-resistance			85		Ω
Protection						
V_{BOOTUV}		BOOT-SW falling		2.5		V
T_{SD}*	Thermal shutdown threshold	T_J rising		168		°C
		Hysteresis		15		°C

*Derived from bench characterization.

TYPICAL CHARACTERISTICS

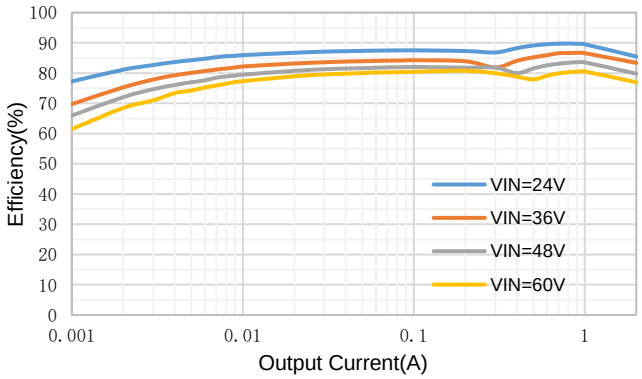


Figure 2. Efficiency, F_{SW}=400kHz, V_{OUT}=5V

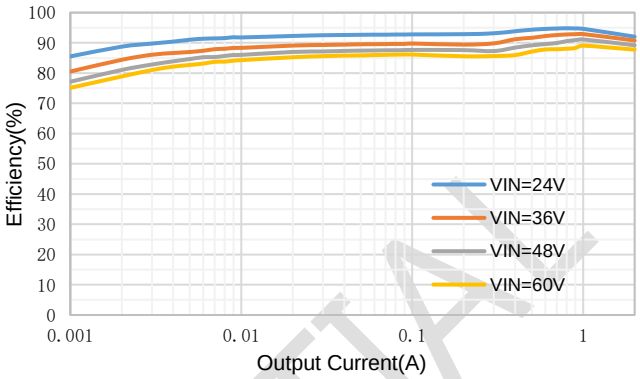


Figure 3. Efficiency, F_{SW}=400kHz, V_{OUT}=12V

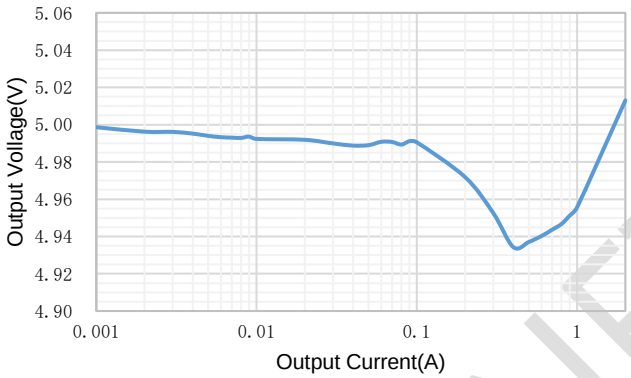


Figure 4. Load Regulation (V_{IN}=48V, V_{OUT}=5V)

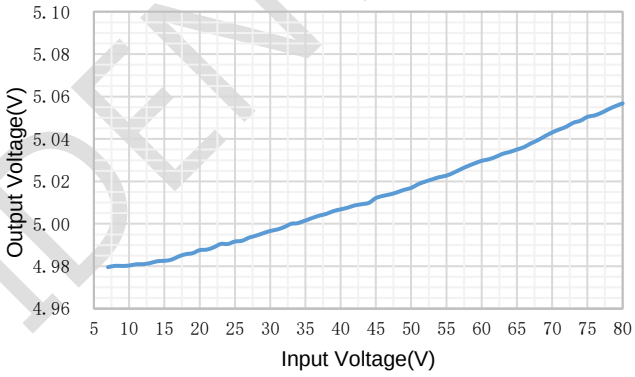


Figure 5. Line Regulation (V_{OUT}=5V, I_{LOAD}=2A)

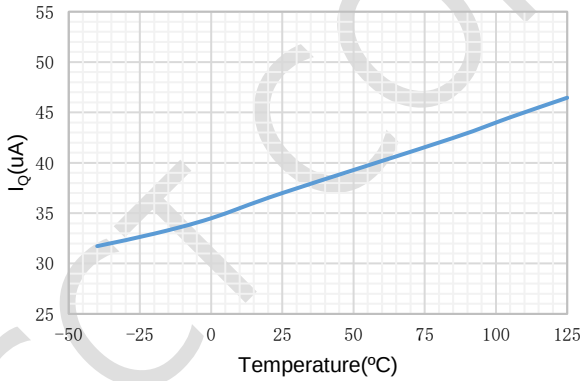


Figure 6. Quiescent current VS Temperature

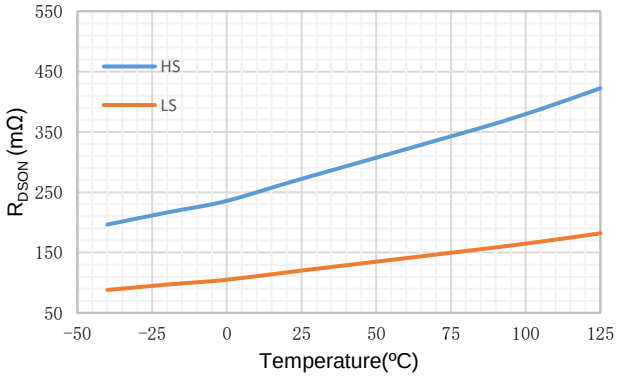


Figure 7. R_{DSON} VS Temperature

FUNCTIONAL BLOCK DIAGRAM

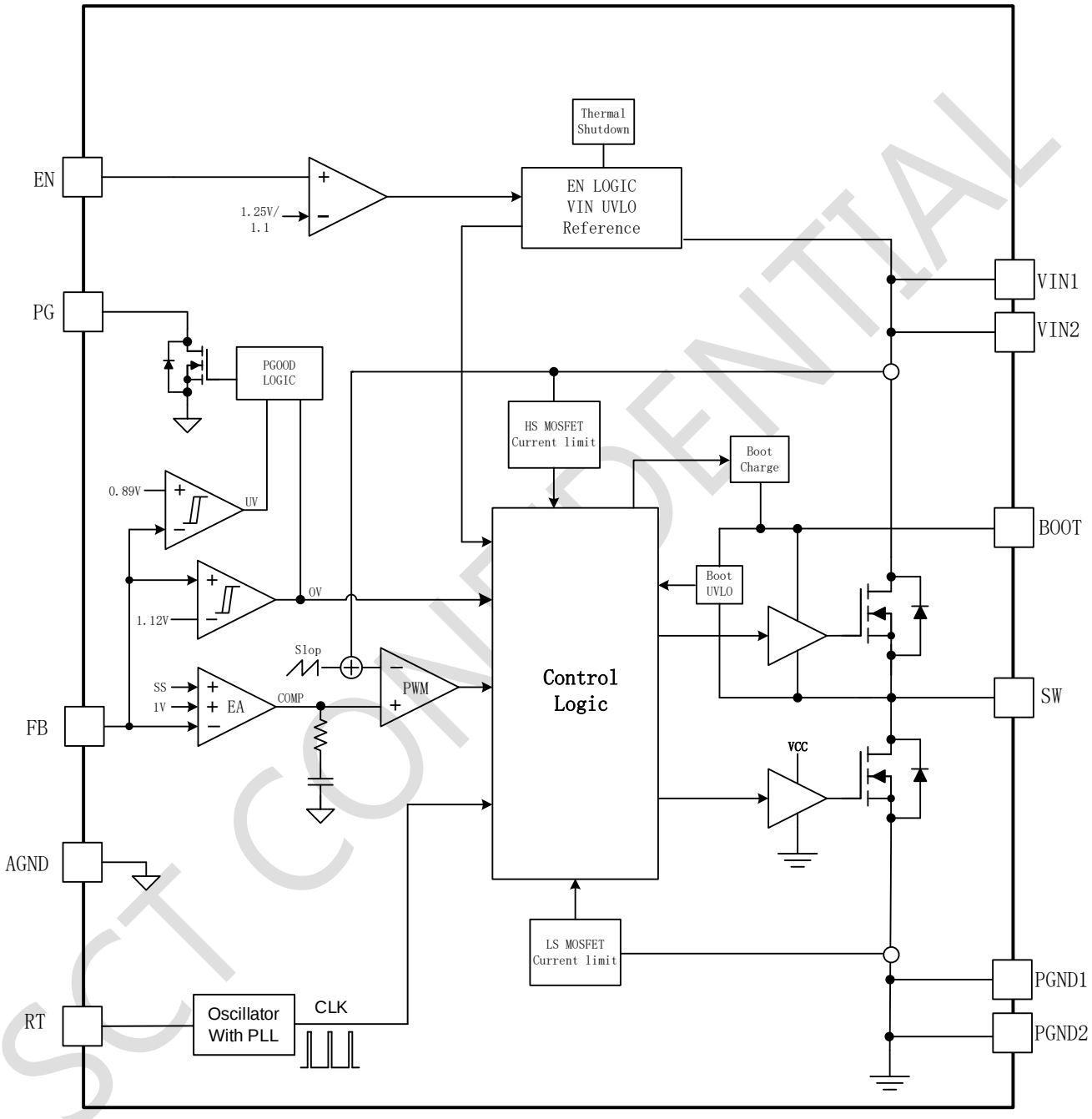


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2821 is a 4.4V-80V input, 2A output, EMI friendly synchronous buck converter with built-in 270mΩ Rdson high-side and 120mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 1.5MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimize either the power efficiency or the external components' sizes. The SCT2821 features an internal 3.5ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 36uA under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Connecting EN pin to VIN directly starts up the device automatically.

SCT2821 achieves ±8% random spread spectrum modulation expansion centered on the set switching frequency. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than apart with fixed frequency operation.

The SCT2821 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2821 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to I_{ZC}.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 1.0V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

Pulse Skipping Mode (PSM) Function

The SCT2821 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold, device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold, then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical I_{peak} inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded. To better reduce power consumption within the full input voltage range, SCT2821 will correspond to different Ipeak at different input voltages. According to the duty cycle, the minimum value of I_{peak} is 0.5A and the maximum value is 0.8A.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 36uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2821 is enabled when the VIN pin voltage rises above 3.55V and the EN pin voltage exceeds the enable threshold of 1.25V. The device is disabled when the VIN pin voltage falls below 3.25V or when the EN pin voltage is below 1.1V. For the device to remain in shutdown mode, apply a voltage below 0.66V to the EN pin. In shutdown mode, the quiescent current drops to 0.6uA (typical). At a voltage above 0.79 and below 1.25V, the internal logic circuit will be turned on, which will consume a certain amount of current.

The EN pin is a high voltage pin and cannot be left open or floating. The simplest way to enable the operation of the SCT2821 is to connect the EN to VIN. This allows self-start-up of the SCT2821 when VIN is within the operating range.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R_1 = R_2 \times (\frac{V_{rise}}{1.25} - 1) \quad (1)$$

$$V_{fall} = 1.1 \times (\frac{V_{rise}}{1.25}) \quad (2)$$

Where:

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

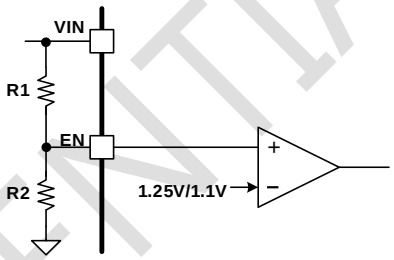


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2821 regulates the internal reference voltage at 1V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft Start and Soft Start Tracking

The SCT2821 integrates an internal soft-start circuit that ramps the reference voltage from zero voltage to 1.0V reference voltage in t_{SS}. Soft start is triggered by any of the following conditions:

• The device is activated through EN or VIN UVLO.

• Recovery from a hiccup waiting period or shutdown due to overtemperature protection.

During soft start, hiccup is disabled. These actions together provide start-up with limited inrush currents and allow the use of larger output capacitors and higher loading conditions that cause current to border on current limit during start-up without triggering hiccup. Hiccup is enabled once output reaches regulation or time exceeds t_{SS2}, whichever happens first.

When the output voltage drops below the set value, the soft start voltage will track the decrease in output voltage in a certain proportion. This situation may occur under the following conditions:

• When the input voltage is too low to maintain the set output voltage.

• When overcurrent occurs causing a decrease in output voltage.

When the above conditions are removed, the output voltage will still increase under soft start. But it should be noted that if the output voltage drops below 37.5% due to overcurrent, hiccup will be triggered.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2821 is set by placing a resistor between RT/SYNC pin and the ground or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/SYNC pin to the ground sets the switching frequency over a wide range from 200kHz to 1.5MHz. The RT/SYNC pin voltage is typical 1V. RT/SYNC pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

$$R(\mathrm{k\Omega}) = 30970 \times F_{sw}(\mathrm{kHz})^{-1.027} \qquad (4)$$

where, Fsw is switching clock frequency.

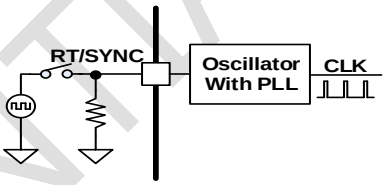


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/SYNC pin. The synchronization frequency range is from 200kHz to 1.5MHz, and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/SYNC pin with typical 20ns time delay. A square wave clock signal to RT/SYNC pin must have high level no lower than 2.75V, low level no higher than 0.45V, and pulse width larger than 100ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock is presented, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 150us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2821 implements Frequency Spread Spectrum (FSS). The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than apart with fixed frequency function. In most systems containing the SCT2821, low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered.

The FSS circuit uses pseudo-random frequency hopping to vary the switching frequency within a specific range. The jittering span is ±8% of the switching frequency. The spread spectrum is only available while the clock of the SCT2821 devices is free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

• The clock is reduced during LDO function.

• The clock is reduced at light load in PSM.

• The clock is reduced during minimum on time function.

• The clock is synchronized with an external clock.

Bootstrap Voltage Regulator and BOOT UVLO

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power

MOSFET is off and low-side power MOSFET is on. A boot diode is integrated on the SCT2821 die to minimize external component count.

The UVLO of high-side MOSFET gate driver has a threshold of 2.5V. When the voltage across bootstrap capacitor drops below 2.5V, BST UVLO occurs, the voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's function.

Low Drop-out Function

At a given clock frequency, duty cycle is limited by minimum off time. During the condition of low voltage difference from the input to the output, to maintain the output voltage from falling, the SCT2821 extends on time past the end of the clock cycle until the required peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a predetermined maximum on time (t_{LDO}) of approximately 12us passes. As a result, to ensure that the output voltage can better follow the changes in input voltage, when SCT2821 operates in LDO function, the switching frequency begins to decrease, with a minimum decrease to 85kHz. The minimum frequency limit avoids possible audio interference.

During slow power on and power off applications, due to the LDO function, the output voltage can closely track the slope changes of the input voltage. As the input voltage is reduced to near the output voltage, i.e., during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO function mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2821 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Minimum On Time Function

Even if the duty cycle at the set frequency is limited by the minimum on time, SCT2821 can still maintain stable adjustment of the output voltage during the transition from high input voltage to low output voltage.

If the input-output voltage ratio is too high, even if the current exceeds the compensation specified peak, the high side MOSFET cannot shut down quickly enough to adjust the output voltage. This will cause the output voltage to continuously increase until overvoltage protection is triggered. To avoid this situation, when the conduction time of the high side MOSFET touches the minimum on time due to the increase in input and output voltage difference, SCT2821 will switch to valley current control mode. After the high side MOSFET is turned off, the low side MOSFET will remain open until the inductor current drops below the required valley current. During this period, the next clock cycle will be blocked from starting, so the switching frequency will decrease. Since on time of high side MOSFET is fixed at its minimum value, this type of function resembles that of a device using a Constant On-Time (COT) control scheme.

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2821 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the inductor current is clamped at over current limitation, the converter cannot provide output current to satisfy loading requirement. Thus, the output capacitor is discharged, and the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP voltage ramps up to high clamp voltage. When FB voltage is below 37.5% of the reference voltage and after 256 cycles of low side current limit, the converter stops switching. After remaining OFF for 68ms， the device restarts from soft start phase. If overload or hard short condition still exists during t_{SS2} and make COMP voltage clamped at high, after t_{SS2} and FB voltage keep below 37.5% of the reference voltage for 256 cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating function.

If the FB voltage drops below 37.5% of the reference voltage due to LDO function, hiccup mode will be disabled.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2821 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 112% of internal 1V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 110% of the 1V reference voltage, the high-side MOSFET can turn on again.

Power Good

The PG pin is an open-drain output. Connect the pin to V_{OUT} or other voltage source through a pull-up resistor between 10kΩ and 100kΩ. Please ensure that the voltage connected to the PG pin does not exceed 20V.

Once the FB pin is between 89% and 110% of the internal voltage reference the PGOOD pin is de-asserted and the pin floats with 20us delay. The PG pin is pulled low when the FB is lower than 87% or greater than 112% of the nominal internal reference voltage with 20us deglitching time. Also, the PG is pulled low if Vin UVLO or thermal shutdown are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 20us deglitching time do not trip the PG flag.

Thermal Shutdown

The SCT2821 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 168°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 153°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

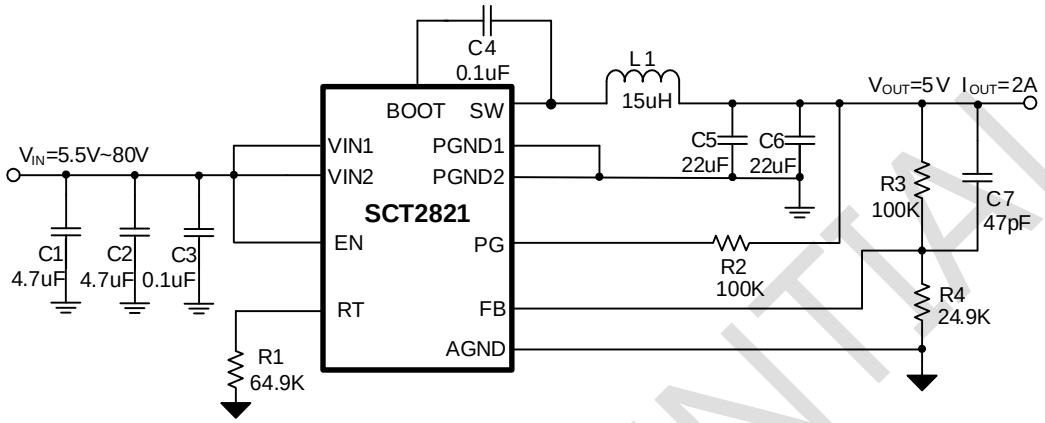


Figure 11. SCT2821 Design Example, 5V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal 5.5V to 80V
Output Voltage	5V
Maximum Output Current	2A
Switching Frequency	400kHz
Output voltage ripple (peak to peak)	12.8mV
Transient Response 0.5A to 1.5A load step	224mV

Output Voltage

The output voltage is set by an external resistor divider R_3 and R_4 in typical application schematic. Recommended R_4 resistance is 24.9KΩ. Use Equation 5 to calculate R_3.

$$R_3 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_4 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 1V.

Table 1. R_3, R_4 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_3	R_4
3.3 V	57.6 KΩ	24.9 kΩ
5 V	100 KΩ	24.9 kΩ
12 V	274 KΩ	24.9 kΩ
24 V	576 KΩ	24.9 kΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. In this design, a moderate switching frequency of 400kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from RT/SYNC to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using Equation 6 or determined from Table 2.

$$R_1(\text{k}\Omega) = 30970 \times F_{sw}(\text{kHz})^{-1.027} \quad (6)$$

where:

- F_{SW} is the desired switching frequency.

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_1 (R_{FSW})
200 kHz	133 KΩ
400 kHz	64.9 KΩ
500 kHz	52.3 KΩ
750 kHz	34.8 KΩ
1000 kHz	25.5 KΩ
1200 kHz	20.5 KΩ
1500 kHz	16.9 KΩ

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 7.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (7)$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 8 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (8)$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN\ (max)}$ is the maximum input voltage.
- $I_{OUT\ (max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 9 and Equation 10.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (9)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (10)$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 3.2A. The most conservative approach is to choose an inductor with a saturation current rating greater than 3.2A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2821 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 11.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst-case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (12)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For this example, two 4.7μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (14)$$

Where:

- $\Delta V_{OUT}$is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- $V_{IN}$is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

Table 3: Typical External Component Values

VOUT	FREQUENCY	R3	R4	R1	L1	C7	COUT
5V	400kHz	100 kΩ	24.9 kΩ	64.9 kΩ	15 uH	47 pF	44uF
12V	400kHz	274 kΩ	24.9 kΩ	64.9 kΩ	33 uH	22 pF	44uF
24V	400kHz	576 kΩ	24.9 kΩ	64.9 kΩ	56 uH	/	66uF
5V	1.2MHz	100 kΩ	24.9 kΩ	20.5 kΩ	4.7 uH	47 pF	44uF
12V	1.2MHz	274 kΩ	24.9 kΩ	20.5 kΩ	10 uH	22 pF	44uF
24V	1.2MHz	576 kΩ	24.9 kΩ	20.5 kΩ	22 uH	/	44uF

Application Waveforms

V_{IN}=48V, V_{OUT}=5V, F_{SW}=400k, unless otherwise noted

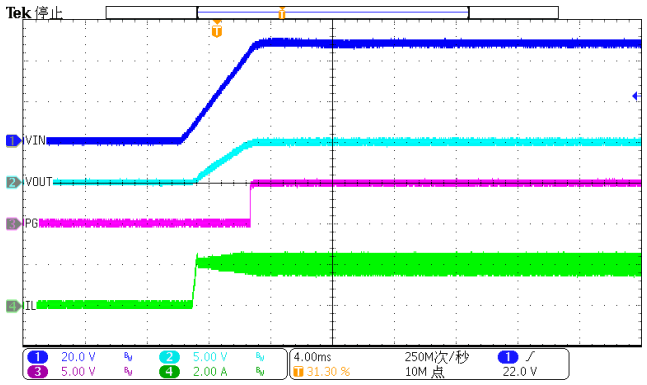


Figure 12. Power up (I_{LOAD}=2A)

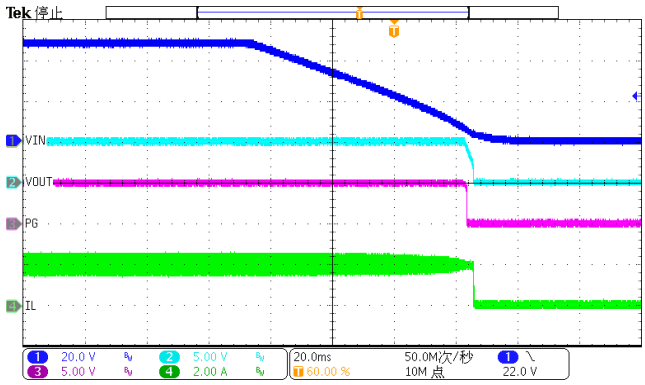


Figure 13. Power down (I_{LOAD}=2A)

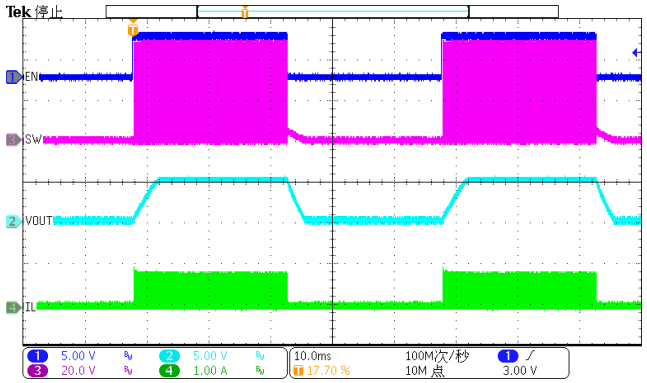


Figure 14. EN toggle (I_{LOAD}=0.1A)

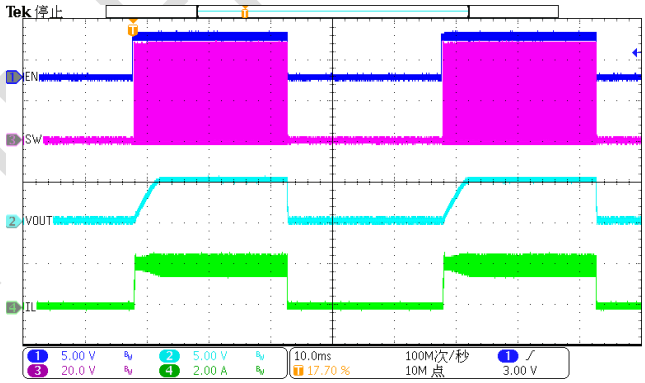


Figure 15. EN toggle (I_{LOAD}=2A)

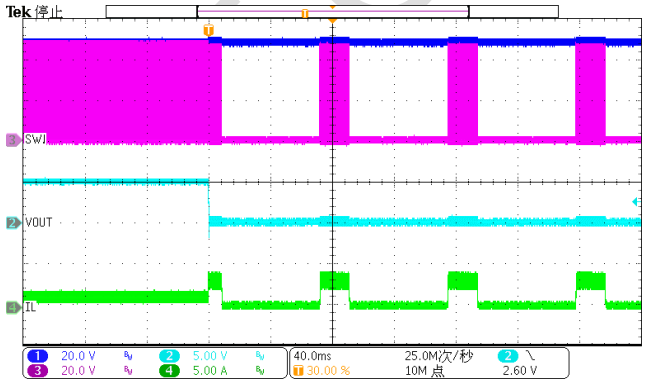


Figure 16. Over Current Protection (1A to hard short)

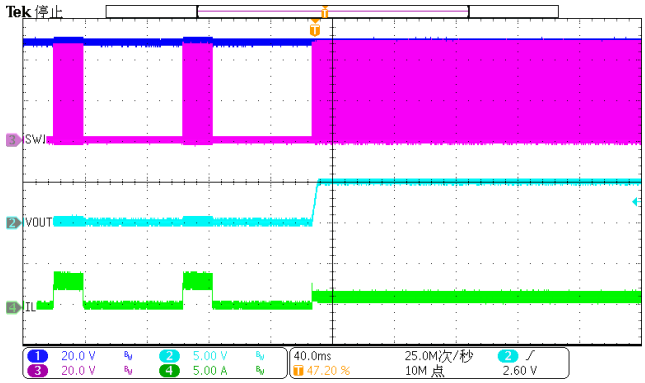


Figure 17. Over Current Release (hard short to 1A)

Application Waveforms

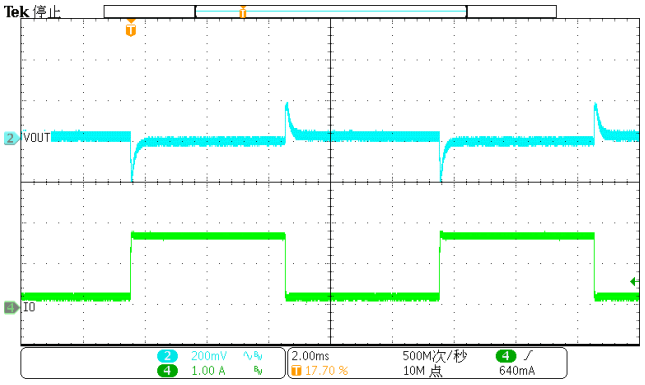


Figure 18. Load Transient (0.2A~1.8A, 1.6A/us)

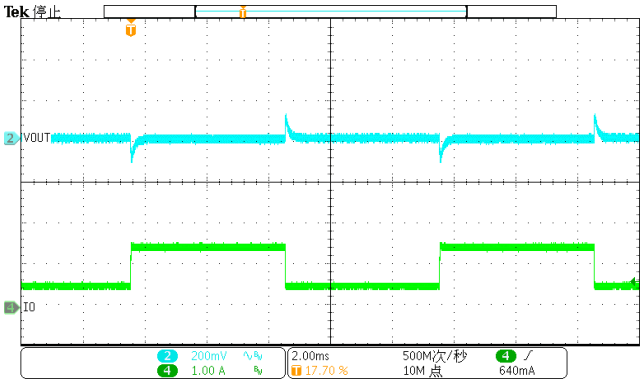


Figure 19. Load Transient (0.5A~1.5A, 1.6A/us)

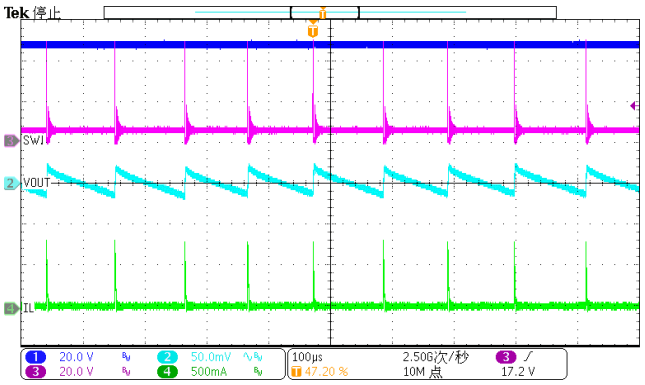


Figure 20. Output Ripple (I_{LOAD}=0.01A)

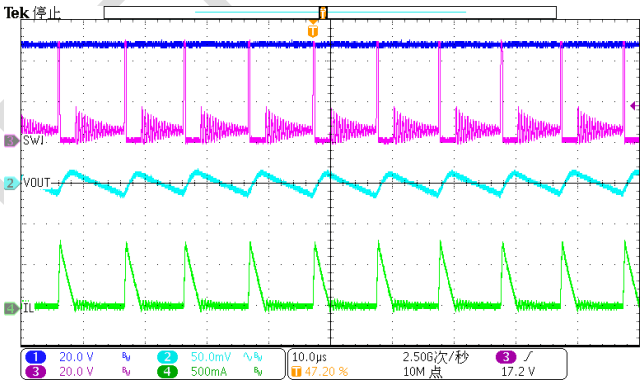


Figure 21. Output Ripple (I_{LOAD}=0.1A)

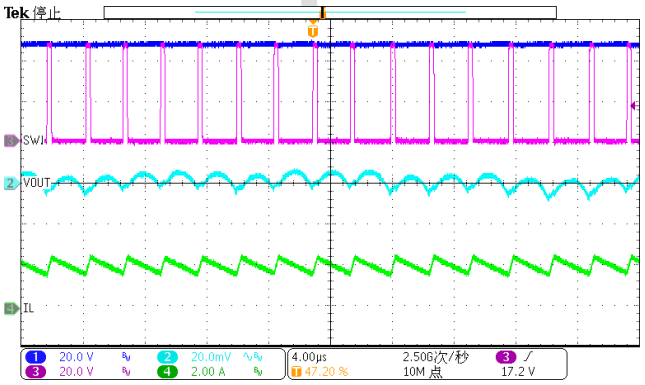


Figure 22. Output Ripple (I_{LOAD}=2A)

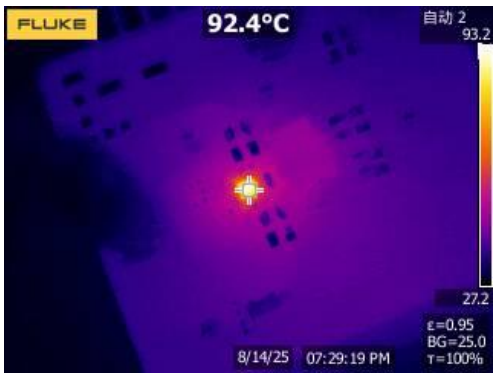


Figure 23. Thermal, 48V_{IN}, 5V_{OUT}, 1.5A

Layout Guideline

Proper PCB layout is a critical for SCT2821's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure the top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to the bottom PCB ground planes using multiple vias directly under the IC. It is recommended 10mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT/SYNC terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

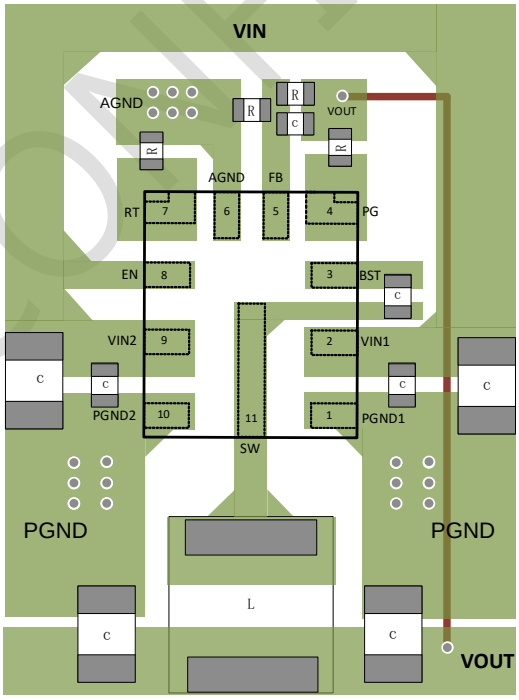
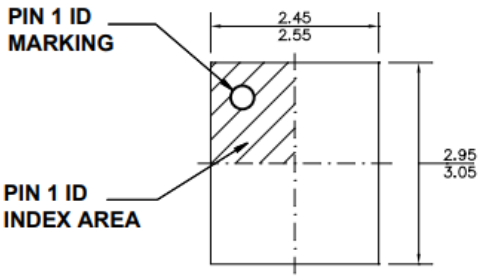
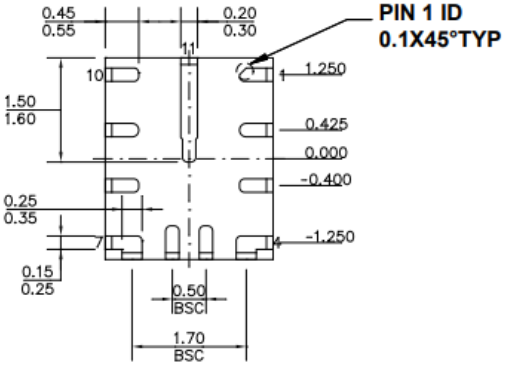


Figure 24. PCB Layout Example

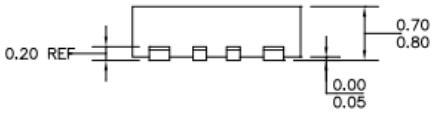
PACKAGE INFORMATION



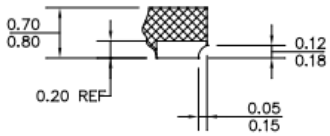
TOP VIEW



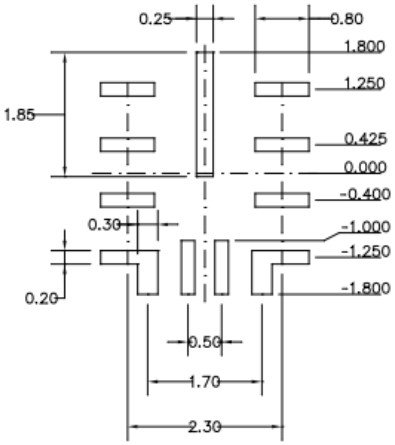
BOTTOM VIEW



SIDE VIEW



SECTION A-A

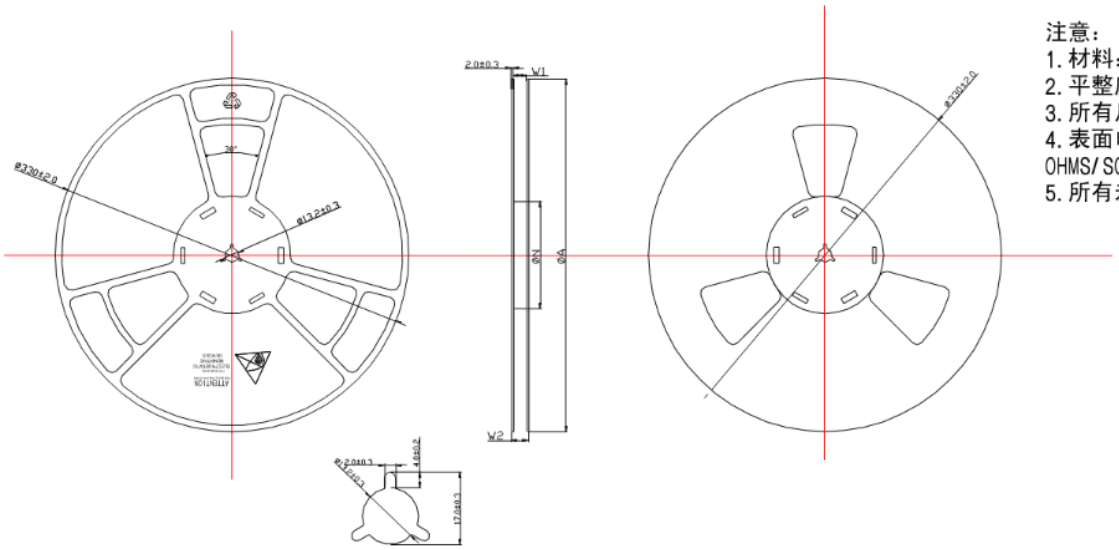


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



注意：
1. 材料：聚苯乙烯；
2. 平整度：最大允许3毫米；
3. 所有尺寸为毫米；
4. 表面电阻：10E5~10E11 OHMS/ SQ以下
5. 所有未标注公差：±0.5

PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1(Min)	W2(Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4