10W High-Integration, High-Efficiency PMIC for Wireless Power Transmitter

FEATURES

- VIN Input Voltage Range: 4.2V-13V
- PVIN Input Voltage Range: 1V-13V
- Up to 10W Power Transfer
- Integrated Full-Bridge Power Stage with 9mΩ Rdson of Power MOSFETs
- Integrated 5V-100mA LDO
- Optimized for EMI Reduction
- Build-in 3.3V-100mA LDO
- Ultra-low quiescent current in Low IQ mode , IQ <15uA
- Integrated Lossless Input Current Sensor with ±2% accuracy for FOD and current Demodulation
- Integrated voltage and current demodulation
- Integrated Q factor detection
- 3.3V and 5V PWM Signal Logic Compatible
- Input Under-Voltage Lockout
- Over Current Protection
- Over Temperature Protection
- 3mm*3.5mm FC-QFN-19L Package

APPLICATIONS

- WPC Compliant Wireless Chargers of 10W Systems for Mobiles, Tablets and Wearable Devices
- General Wireless Power Transmitters for Consumer, Industrial and Medical Equipment
- Proprietary Wireless Chargers and Transmitters

DESCRIPTION

The SCT63052 is a highly integrated Power Management IC allows achieving high performance, high efficiency and cost effectiveness of wireless power transmitter system compliant with WPC specification to support up to 10W power transfer, working with a wireless application specific controller or a general MCU based transmitter controller.

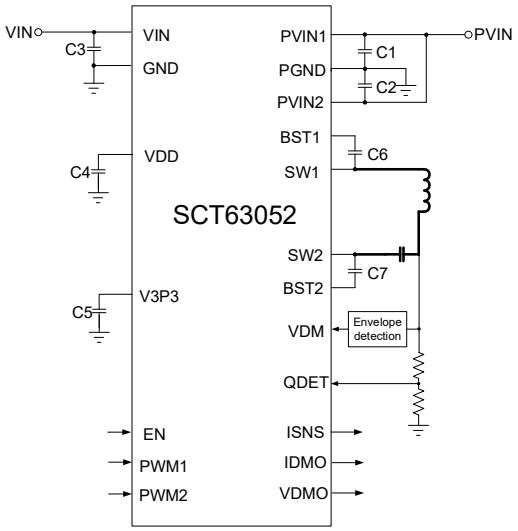
This device integrates a 4-MOSFETs full bridge power stage，gate drivers, a 5V LDO, a 3.3V LDO, communication demodulator, Q-factor detection and input current sensor for both system efficiency and easy-to-use.

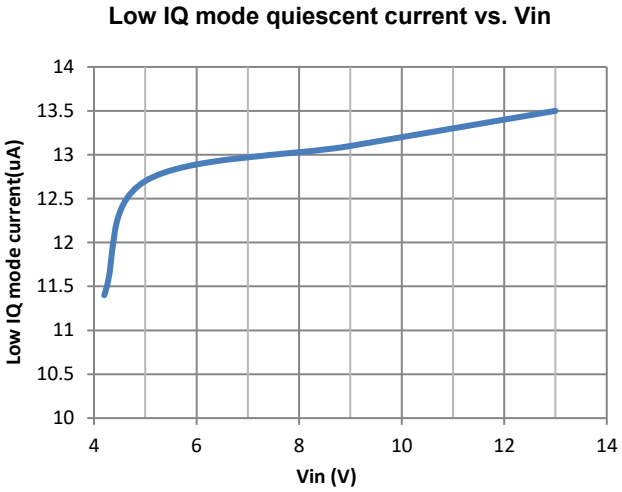
The proprietary gate driving scheme optimizes the performance of EMI reduction to save the system cost and design. The proprietary lossless current sensing circuitry with ±2% accuracy monitors input current of full bridge to support Foreign Object Detection FOD and current demodulation. The build-in 5V and 3.3V low dropout regulator LDO can provide power supplies to transmitter controller and external circuitries. The low IQ mode with ultra-low quiescent current to decrease power loss for Q factor detection.

The SCT63052 features input Under-Voltage Lock-out UVLO, over current, short circuit protection, and over temperature protection.

The SCT63052 is available in a compact 3mm*3.5mm FC-QFN package.

TYPICAL APPLICATION





REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT63052FICR	Tape & Reel	5000	3052	19	FCUTQFN3X3.5-19L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	18	V
PVIN1, PVIN2	-0.3	16	V
SW1,SW2	-1	16	V
BST1,BST2	-0.3	22	V
BST1-SW1,BST2-SW2	-0.3	6	V
VDD, V3P3, VDM, EN, PWM1, PWM2, ISNS, IDMO, VDMO, QDET	-0.3	6	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

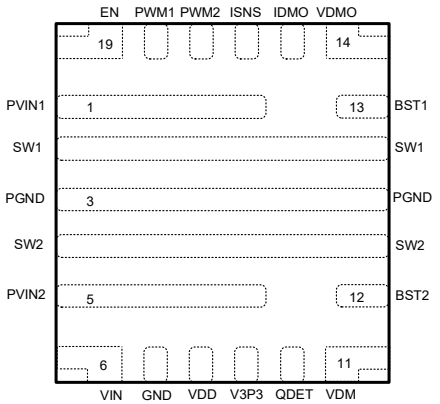


Figure 1. Top view 19-Lead QFN 3mm*3.5mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PVIN1	1	Input supply voltage of half-bridge FETs Q1 and Q2. Connected to the drain of high side FET Q1. A local bypass capacitor from PVIN1 pin to PGND pin should be added. Path from PVIN1 pin to high frequency bypass capacitor and PGND must be as short as possible.
PGND	3	PGND is the common power ground of the full bridge, connected to the source terminal of low side FETs Q2 and Q4 internally.
PVIN2	5	Input supply voltage of half-bridge FETs Q3 and Q4. Connected to the drain of high side FET Q3. A local bypass capacitor from PVIN2 pin to PGND pin should be added. Path from PVIN2 pin to high frequency bypass capacitor and PGND must be as short as possible.
VIN	6	Input supply voltage of the 5V LDO. Add a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	7	Ground.
VDD	8	Output voltage of the 5V LDO. Connect 2.2uF capacitor from this pin to GND pin. VDD is the input power supply for gate driver of power stage and the 3.3V LDO.
V3P3	9	3.3V LDO output. Connect 1uF capacitor to ground.
QDET	10	Q-factor detection input.
VDM	11	High-pass filter input. Voltage demodulation pin data packets based on coil voltage.
BST2	12	Power supply bias for the high-side power MOSFET gate driver of Q3 as shown in the block diagram. Connect a 0.1uF capacitor from BST2 pin to SW2 pin.
SW2	4	Switching node of the half-bridge FETs Q3 and Q4.
SW1	2	Switching node of the half-bridge FETs Q1 and Q2.
BST1	13	Power supply bias for the high-side power MOSFET gate driver of Q1 as shown in the block diagram. Connect a 0.1uF capacitor from BST1 pin to SW1 pin.
VDMO	14	Voltage demodulation output.
IDMO	15	Current demodulation output.
ISNS	16	Current detection output. Connect a high accuracy resistor (10KΩ±0.1% typical.) and a capacitor((4.7nF typical.) in parallel between this pin to ground. Need pull PWM1 to high and PWM2 to low when MCU calibrates ISNS offset.
PWM2	17	PWM logic input to the FET Q3 and Q4 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q4 and turns on the high-side FET Q3. Logic LOW turns off the high-side FET Q3 and turns on the low-side FET Q4. PWM2 default pull down to GND with 100kohm inner resistor.
PWM1	18	PWM logic input to the FET Q1 and Q2 as shown in the Block Diagram. Logic HIGH turns off the low-side FET Q2 and turns on the high-side FET Q1. Logic LOW turns off the high-side FET Q1 and turns on the low-side FET Q2. PWM2 default pull down to GND with 100kohm inner resistor.
EN	19	Enable pin. Pull the pin high to enable the full bridge, the full bridge starts to work if VIN higher than UVLO threshold, power stage responds to PWM input logic then. The full bridge is disabled when pull the pin to low. Pull a high voltage level pulse to EN pin can trigger the Q factor detection feature. EN pin default pull down to GND with 1Mohm inner resistor. 5V and 3.3V LDO are not controlled by the EN pin.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.2	13	V
P_{VIN}	Input voltage range	1	13	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCUTQFN3X3.5-19L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	44	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	27	

(1) Measured on JESD51-7, SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT63052 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT63052. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{PVIN1}=V_{PVIN2}=9V, VDD=5V, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input supplies and UVLO						
V_{IN}	Operating input voltage		4.2		13	V
P_{VIN}	Operating input voltage		1		13	V
V_{IN_UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		2.65 100		V mV
V_{3P3_UVLO}	V_{3P3} UVLO Threshold Hysteresis	V_{3P3} rising		2.4 200		V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0V, VIN=9V, no loading on LDO		13		μA
I_{SHDN_PVIN}	Shutdown current from PVIN1,PVIN2	EN=0V, PVIN=9V		1	3	uA
I_{VINQ}	Quiescent current from VIN pin	EN=5V, no loading on LDO		450		uA
I_{PVINQ}	Quiescent current from PVIN1, PVIN2	EN=5V, no loading on LDO		50		uA
ENABLE INPUTS and PWM logic						
V_{EN_H}	Enable high threshold		1.15	1.18		V
V_{EN_L}	Enable low threshold			1.1	1.14	V
R_{EN_PD}	EN inner pull-down resistance			1		MΩ
V_{IH}	PWM1, PWM2 Logic level high	V3P3=3.3V, VDD=5V	2.1			V
V_{IL}	PWM1, PWM2 Logic level low	V3P3=3.3V, VDD=5V			0.8	V
$R_{pull-down}$	PWM1/2 inner pull-down Res			100		kΩ
T_{min-on}	Min on time(1)			300		ns
$T_{min-off}$	Min off time(1)			300		ns
Power Stage						
$R_{DSON\_Q1\ Q3}$	High-side MOSFET Q1 Q3 on-resistance	V_{BST1}-V_{SW1}=5V, V_{BST2}-V_{SW2}=5V		9		mΩ
$R_{DSON\_Q2\ Q4}$	Low-side MOSFET Q2 Q4 on-resistance	VDD=5V		9		mΩ
I_{LIM}	How-side current limit threshold			4		A
5V LDO						
V_{DD}	Output voltage	Cout=2.2uF	4.75	5	5.25	V
I_{VDD}	Output current capability	EN=5V		100		mA
3.3V LDO						
V_{3P3}	Output voltage	Cout=1uF	3.267	3.3	3.333	V
I_{3P3}	Output current capability	EN=5V		100		mA
I_{SC}	Short current			150		mA
Current Sense						
I_{ISNSO}	DC offset current		80	100	120	μA
R_{ISNS_Gain}	Current sense Gain		98	100	102	μA/A
Protection						
T_{SD}	Thermal shutdown threshold	T_J rising		160		°C
	Hysteresis			35		°C

Notes:
1) Guaranteed by sample characterization. Not tested in production.

TYPICAL CHARACTERISTICS

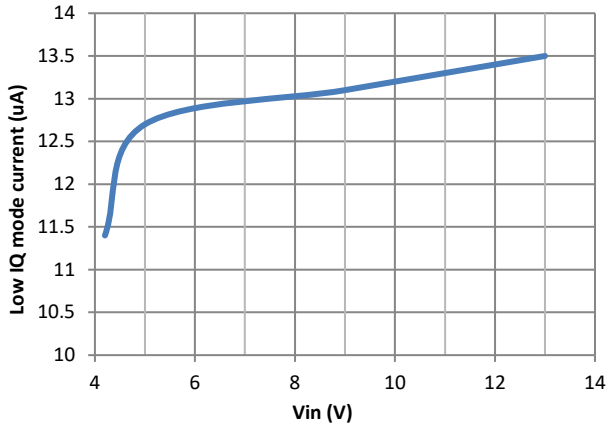


Figure 2. Low IQ mode current vs Vin

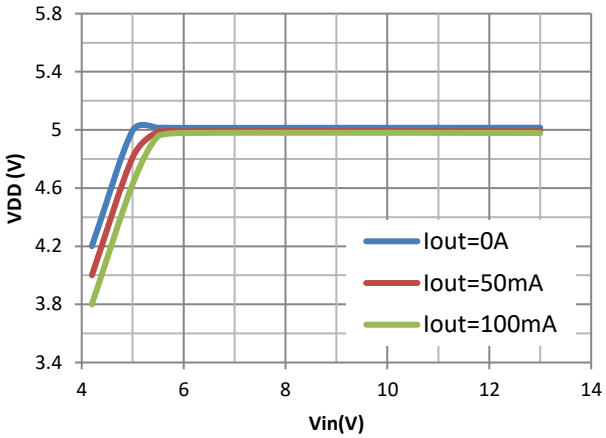


Figure 3. 5V LDO Vout vs Vin

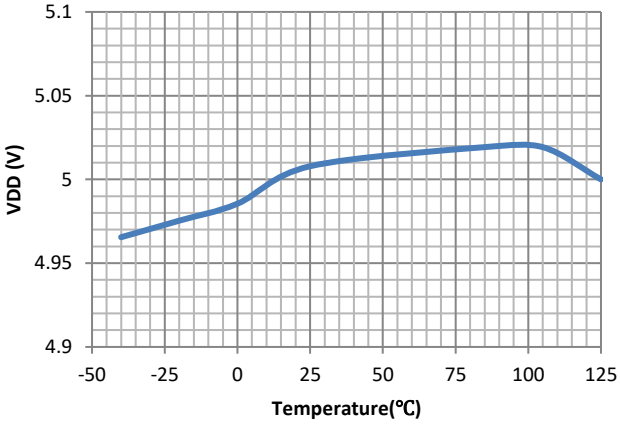


Figure 4. 5V LDO Vout vs temperature @Vin=9V

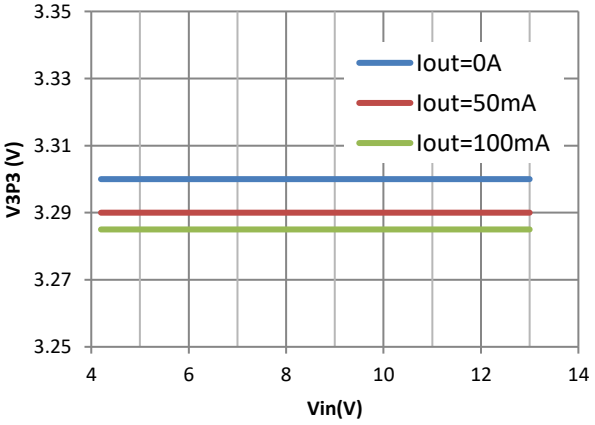


Figure 5. 3.3V LDO Vout vs Vin

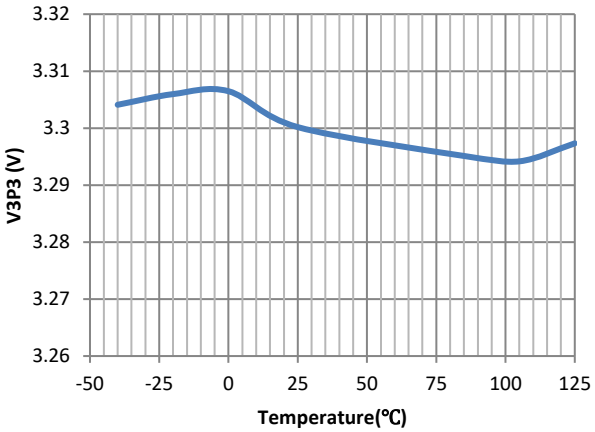


Figure 6. 3.3V LDO Vout vs temperature @Vin=9V

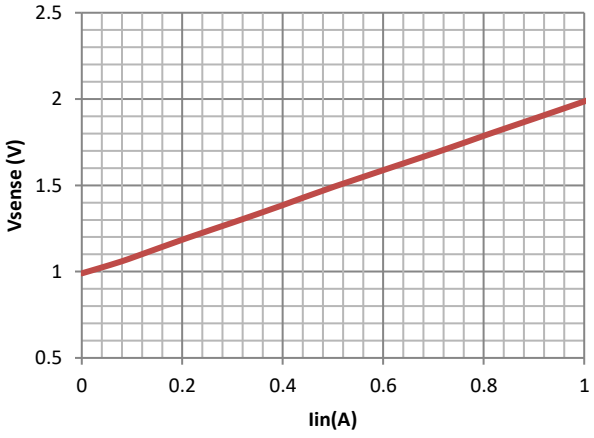


Figure 7. Current Sense Output Voltage vs Iin

FUNCTIONAL BLOCK DIAGRAM

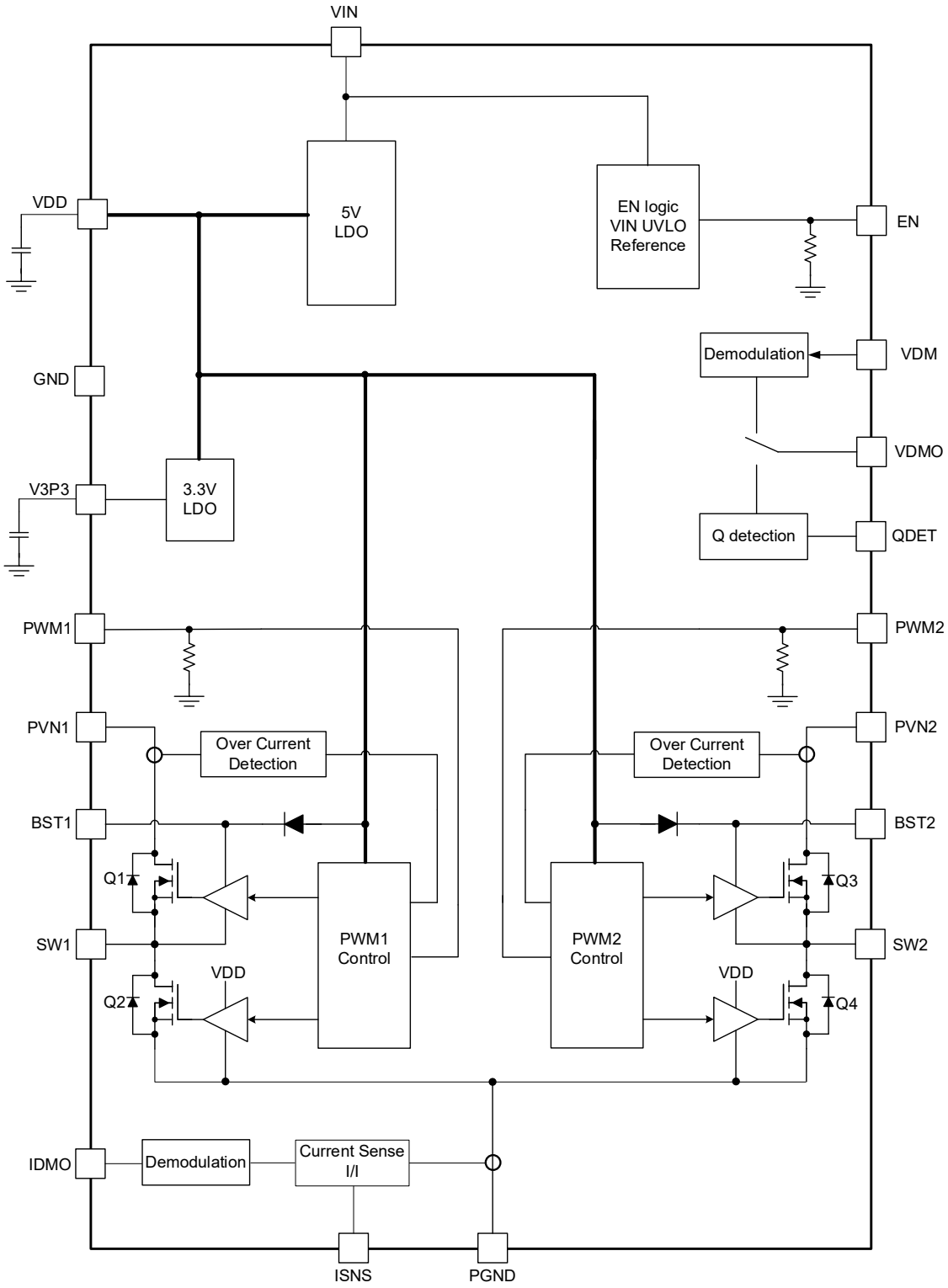


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT63052 is a highly integrated power management unit optimized for wireless power transmitter applications. This device integrates the power functions required to a wireless power transmitter including 5V output LDO as power supply for external transmitter controller, full bridge power stage to convert DC input power to AC output for driving LC resonant circuit, lossless current sensing with ±2% accuracy, 3.3V output LDO for powering MCU.

The SCT63052 has three power input pins. VIN is connected to the power FETs of 5V LDO. PVIN1 and PVIN2 are connected to the power FETs of the full bridge and conduct high currents for power transfer.

VIN and PVIN1, PVIN2 can be powered separately for more flexibility of system power design. The operating voltage range for VIN is from 4.2V to 13V. An Under-Voltage Lockout(UVLO) circuit monitors the voltage of VIN pin and disables the IC operation when VIN voltage falls below the UVLO threshold of 2.55V typically. The maximum operating voltage for PVIN is up to 13V while the minimum voltage accepted can be down to 1V.

Two independent PWM signals control two separate half bridge MOSFETs with internal adaptive non-overlap circuitry to prevent the shoot-through of MOSFETs in each bridge. PWM logics are compatible for both 3.3V and 5V IOs so the SCT63052 can accept PWM signal from the controller with using 3.3V or 5V power supply.

The full bridge of power MOSFETs includes proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching. This allows the user to reduce the system cost and design effort for EMI reduction.

The SCT63052 full protection features include VIN and VDD under-voltage lockout, over current protection with cycle-by-cycle current limit and hiccup mode, output hard short protection for 4-MOSFETs full bridge, current limit and current fold back at hard short for two LDOs and thermal shutdown protection.

Enable and Start up Sequence

When the VIN pin voltage rises above 2.65V, and the EN pin voltage exceeds the enable threshold of 1.18V, the 4-MOSFETs full bridge allows PWM signal to control for switching. And the full bridge disables when the VIN pin voltage falls below 2.55V or when the EN pin voltage is below 1.1V. PWM input cannot control full bridge of MOSFETs. Pull a high voltage level pulse to EN pin can trigger the Q factor detection feature. 5V and 3.3V LDO are not controlled by the EN pin.

5V LDO

The SCT63052 has an integrated low-dropout voltage regulator which powered from VIN and supply regulated 5V voltage on VDD pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of external transmitter controller directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the VDD pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Full bridge and PWM Control

The SCT63052 integrates full bridge power stage with only 9mohm on-resistance for each power MOSFET optimized for wireless power transmitter driving the LC resonant circuit. This full bridge is able to operate in a wide switching frequency range from 20KHz to 2000KHz for different applications.

PWM1 input controls the half bridge comprised of high side MOSFET Q1 and low side MOSFET Q2, and PWM2 input controls the half bridge comprised of high side MOSFET Q3 and low side MOSFET Q4 as shown in block diagram. The PWM1 and PWM2 independently control the SW1 and SW2 duty cycle and frequency. Logic HIGH will turn off low side FET and turn on high side FET, and logic LOW will turn off high side FET and turn on low side FET.

An external 100nF ceramic bootstrap capacitor between BST1 and SW1 pin powers floating high-side power MOSFET Q1's gate driver, and the other 100nF bootstrap capacitor between BST2 and SW2 pin powers for the Q3's. When low side FET is on which means SW is low, the bootstrap capacitor is charged through internal path by VDD power supply rail.

PWM cannot been kept as high level for more than 2ms since the voltage of bootstrap capacitor will be discharged by internal leakage current if high side FET keeps on.

Full Bridge Over Current Protection

The SCT63052 integrates cycle-by-cycle current limit and hiccup mode for over-current protection. The current of the high side FET Q1 and Q3 is sensed and compared to the current limit threshold during each switching cycle. If the current exceeds the threshold, 4A typical, the high side FET turns off immediately in present cycle to avoid current increasing even PWM signal is still kept in a high level. The over current counter is incremented. If one high side FET occurs over current in 5 consecutive cycles, then all 4 internal FETs are turned off regardless of the PWM inputs. The full bridge enters hiccup mode and will attempt to restart after a time-out period of 20ms typically.

Current Sense

The SCT63052 has a proprietary lossless average current sensing circuit that measures the average input current of full bridge with ±2% accuracy and reports measure ratio current to the ISNS pin. It is recommended to connect a typical high accuracy 10KΩ±0.1% and a 4.7nF capacitor to ISNS pin, since the tolerance depends on both the current sense circuit and the external resistor. When the full bridge of MOSFETs does not work, no current flows to PGND. The current sense amplifier output has an offset of 100μA at zero input current. DC bias helps set up a suitable voltage bias for the following analog to digital converter in MCU or amplifier for current demodulation. The equation 1 represent the corresponding relation for the output voltage on ISNS pin and average current to PGND from full bridge with 10KΩ±0.1% resistor:

$$V_{ISNS} = V_{offset} + I_{PGND} * 1V/A \qquad (V_{offset} \text{ typical is 1V at 10K}\Omega \text{ resistor}) \qquad (1)$$

Need pull PWM1 to high and PWM2 to low when MCU calibrates ISNS offset voltage, and then EN pin also need to pull low (>50us) after calibrates ISNS offset to avoid BST voltage not enough. Figure 9 is typical application sense circuit with 10KΩ±0.1% resistor.

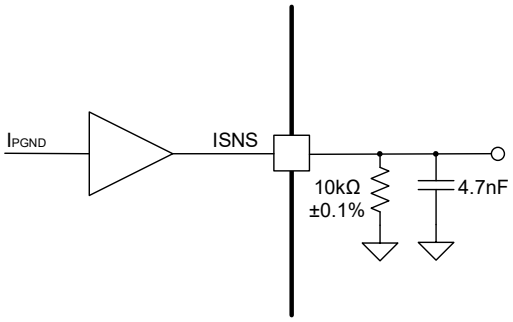


Figure 9. Current sense circuit with 10kΩ±1% resistor

3.3V LDO

The SCT63052 has an integrated low-dropout voltage regulator which is powered from VDD and supply regulated 3.3V voltage on V3V pin. The output current capability is 100mA. This LDO can be used to bias the supply voltage of MCU directly.

It is recommended to connect a decoupling ceramic capacitor of 1uF to 10uF to the V3V pin. Capacitor values outside of the range may cause instability of the internal linear regulator.

Low IQ Mode

The SCT63052 supports Low IQ Mode. Only full bridge is disabled when EN pin is low or floating. 5V and 3.3V LDO are still alive with ultra-low quiescent current to decrease power loss for Q factor detection.

Q Factor Detection

The SCT63052 integrated a low cost, reliable Q factor detection circuit to assure foreign objects detection before the selection phase. It generates a small pulse to detect any foreign object on the transmitter coil, it can detect metal on the transmitter coil easily.

After chip enable, apply a high voltage level pulse to EN pin can trigger the Q factor detection feature. The pulse width should be longer than 100us but less than 200us. SW1 will be preset to 1.5V for 1ms and then pull low to ground and this apply power to LC resonant loop and Vcoil will appear damping oscillation after SW1 short to ground. The SCT63052 will generate a pulse on VDMO pin and MCU can capture this pulse to calculate the Q factor by the pulse width as the aquation 2 shows. PWM1 and PWM2 should be low in Q factor detection phase.

$$Q = \frac{\triangle T * \pi}{10 * \ln \frac{V_{TH\_HIGH}}{V_{TH\_LOW}}} \quad (2)$$

where

- ΔT is the pulse width on VDMO pin
- V_{TH_HIGH} is high threshold 0.2V
- V_{TH_LOW} is low threshold 0.1V

Voltage and Current Demodulation

The SCT63052 integrates two demodulation schemes, one based on coil voltage information calling voltage demodulation and the other based on input average current information calling current demodulation.

The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 10. This simple implementation achieves the envelope detector function, low-pass filter as well as the DC filter function. The envelope detector applies the analog signal to VDM pin and the chip do the demodulation and output a digital signal to VDMO pin which MCU can capture the voltage demodulation results and then implement the packet decode.

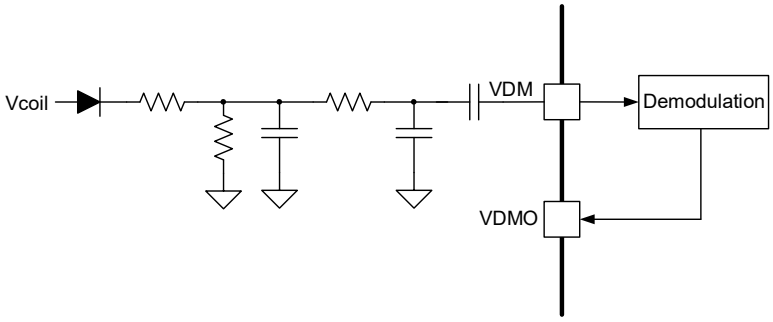


Figure 10. Envelope Detector

The current-mode detector takes the modulation information from the average input current which the chip can read from ISNS pin. The MCU can detect the demodulation results on VDMO and IDMO pins and then implement the packet decode.

Thermal Shutdown

The SCT63052 protects the device from the damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 160C, the thermal sensing circuit stops 3.3V LDO and full bridge of 4-MOSFETs' working. When the junction temperature falls below 125C, then the device restarts.

APPLICATION INFORMATION

Typical Application

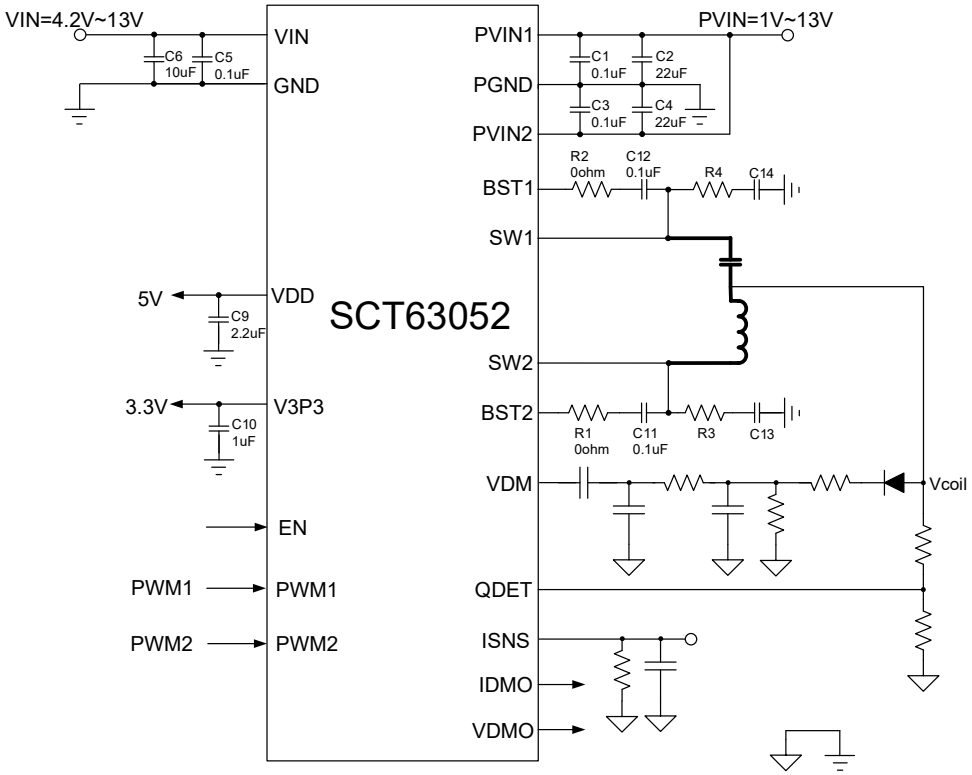


Figure 11. Same Input to VIN and PVIN

Application Waveforms

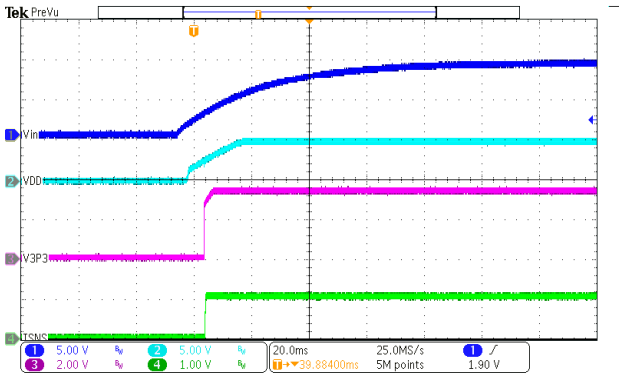


Figure 12. Power Up

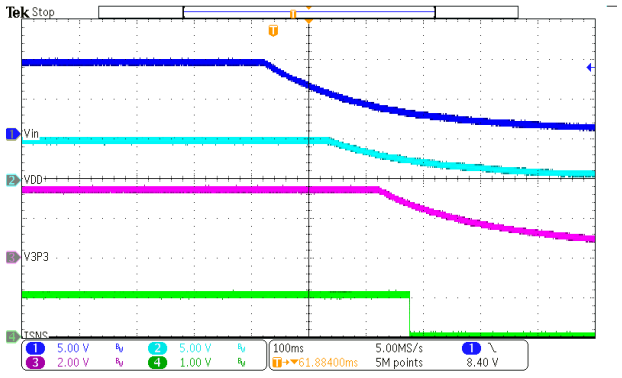


Figure 13. Power Down

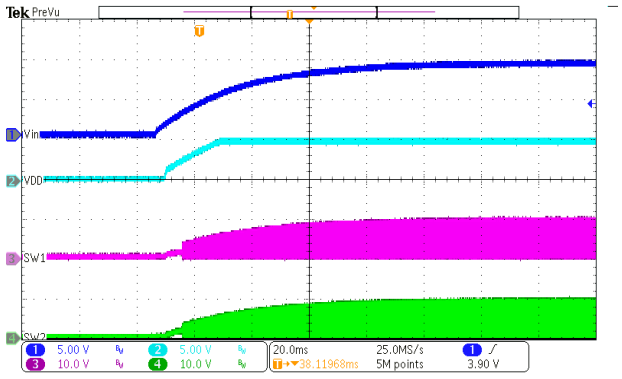


Figure 14. Power Up

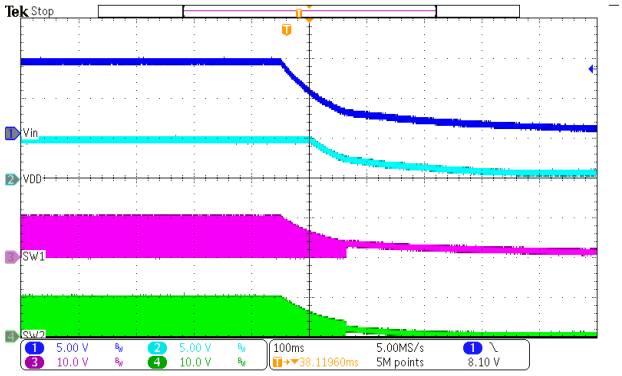


Figure 15. Power Down

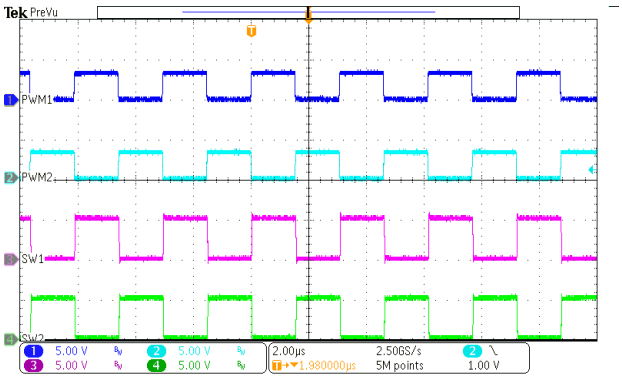


Figure 16. Full bridge @Vin=5V, RX=2.5W

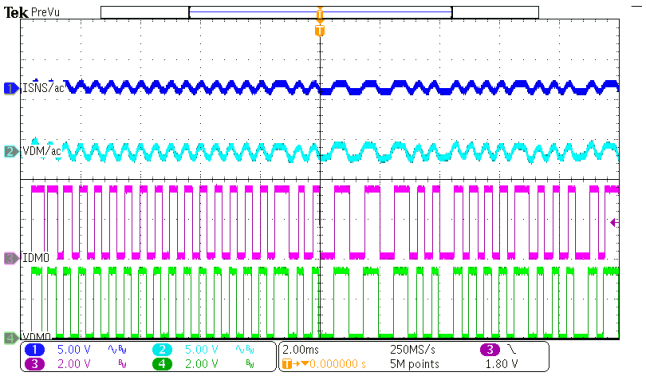


Figure 17. VDMO/IDMO Demodulation Output

Layout Guideline

Proper PCB layout is a critical for SCT63052's stable and efficient operation. For better results, follow these guidelines as below:

1. Bypass capacitors from PVIN to PGND should put next to PVIN and PGND pin as close as possible especially for the two small capacitors.
2. PGND connect to bottom layer by via between capacitors.
3. Bypass capacitors from VIN to GND should put next to VIN and GND pin as close as possible especially for the small capacitor.
4. Bypass capacitor for VDD place next to VDD pin.
5. Bypass capacitor for V3P3 place next to V3P3 pin.

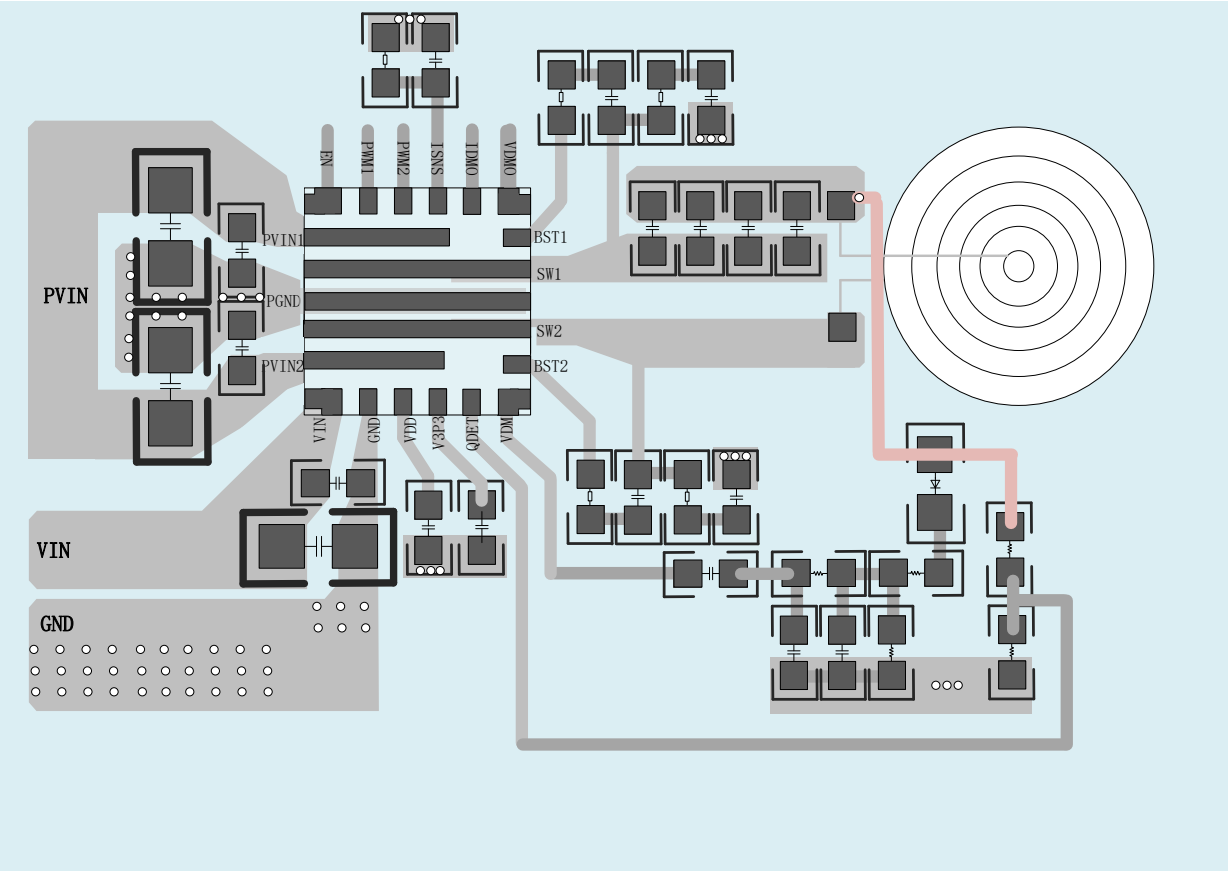
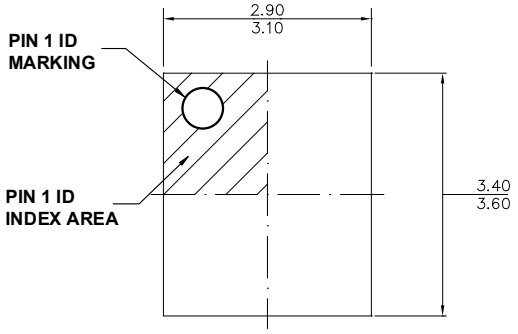
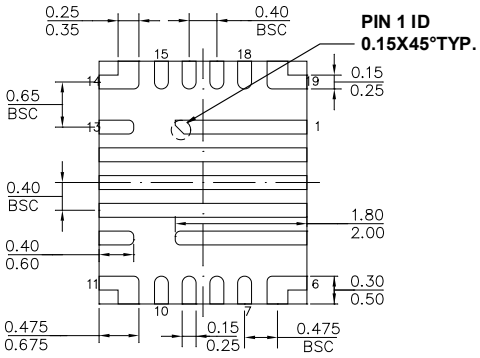


Figure 18. PCB Layout Example

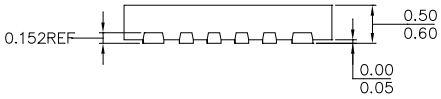
PACKAGE INFORMATION



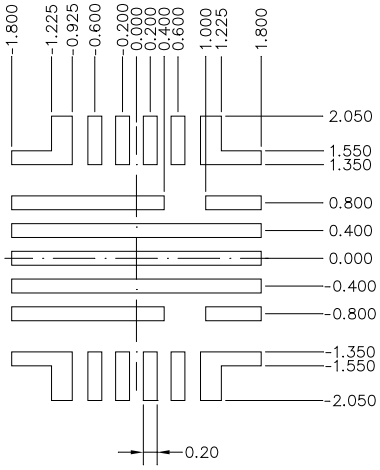
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION