

## 36V Vin Five Channels PMIC for Safety Applications

### FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1
- Wide Input Voltage Range: 3.5V-36V
- One Synchronous HV Buck Converter VOUT1:
  - Up to 3A Continuous Output Current
  - Output Voltage Range of 3.3V
- Dual Synchronous LV Buck Converters VOUT2, VOUT3:
  - Up to 2A Continuous Output Current
  - Output Voltage Range 0.8V to 2.35V with 50mV Steps
- One Synchronous LV Boost Converter VOUT4:
  - Up to 500mA Continuous Output Current
  - Output Voltage of 5V
- One Load Switch VOUT5:
  - Up to 800mA Continuous Output Current
  - Output Voltage of 3.3V
- +/- 1.5% Feedback Reference Voltage
- Fixed 2.2MHz Switching Frequency with Integrated Frequency Dither for EMI Mitigation
- FCCM/PFM Selectable
- Sleep mode to save power dissipation
- Programmable Power Sequencer for VOUT2, VOUT3, VOUT4 and VOUT5
- RESETB Output for System Management
- Simple/QA Watchdog
- Integrated Protection Features:
  - Hiccup Over Current Protection
  - Output Over-voltage/Under-voltage Protection
  - Adjustable Input Voltage Under-Voltage Lockout
  - Thermal Shutdown Protection
- Functional Safety Features:
  - Compliance with ISO26262 Development
  - Hardware Integrity up to Support ASIL-B System
  - ASIL-B Device Certification by TUV
  - BIST
- Up to 1MHz I2C Interface with Optional Packet Error-Checking (PEC)
- Available in QFN-24 (4mm\*4mm)

### DESCRIPTION

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for SoCs in automotive and industrial radar applications.

The SCT61450S integrates one 3A HV Buck, two identical 2A LV Bucks, one 500mA LV Boost and one 800mA LV Load Switch. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter RESET state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61450S device has protection features such as thermal shutdown, short-circuit protection and over-voltage protection. Sleep mode reduces the total supply current to 0.85 mA.

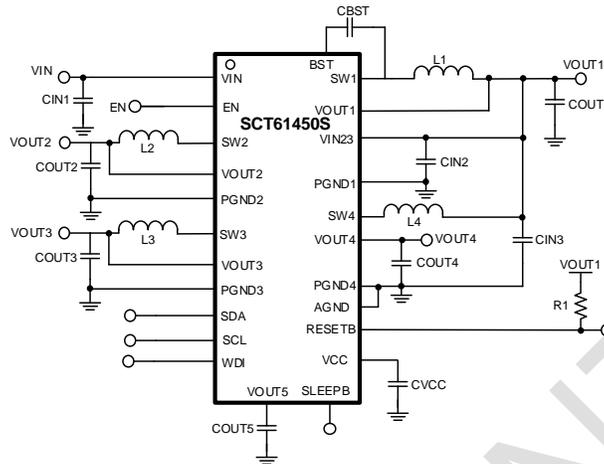
The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked during power up stage.

The device is available in a QFN-24(4mm\*4mm) package with wettable flanks.

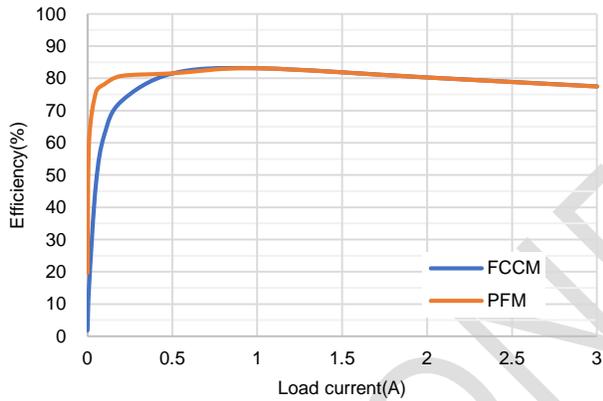
### APPLICATIONS

- ADAS
- 77GHz Radar
- Safety MCU

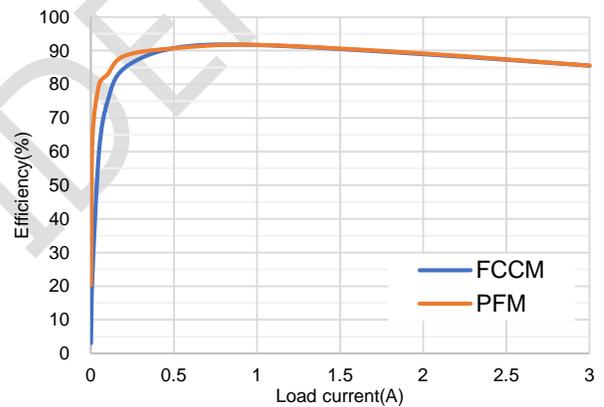
**TYPICAL APPLICATION**



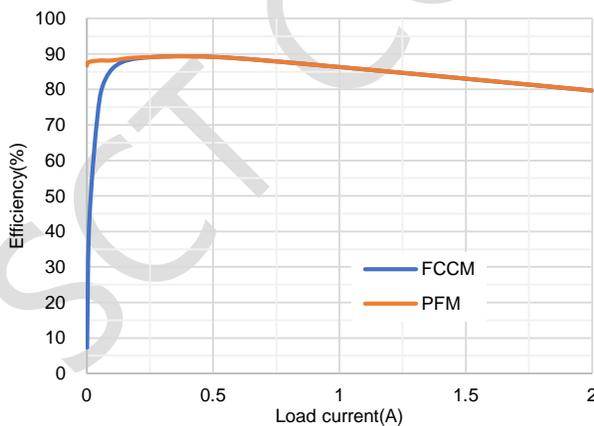
SCT61450S Radar PMIC Typical Application Circuit



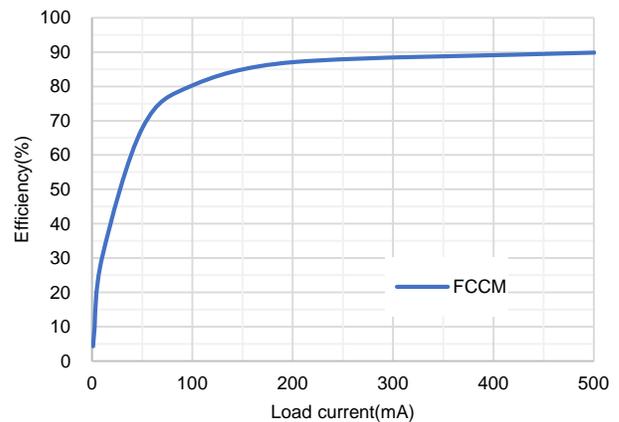
Buck1 Efficiency vs Load Current,  $V_{OUT1}=3.3V$ ,  $f_{SW1}=2.2MHz$



Buck1 Efficiency vs Load Current,  $V_{OUT1}=3.3V$ ,  $f_{SW1}=400kHz$



Buck2/3 Efficiency vs Load Current,  $V_{OUT2/3}=1.2V$



Boost Efficiency vs. Load Current,  $V_{OUT4}=5V$

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 1.0: Released to Market

Revision 1.1: Add slee mode and watchdog description, update thermal resistance and layout guideline, correct typo

## DEVICE ORDER INFORMATION

| PART NUMBER                       | PACKAGING TYPE | STANDARD PACK QTY | PACKAGE MARKING | PINS | PACKAGE DESCRIPTION | MSL |
|-----------------------------------|----------------|-------------------|-----------------|------|---------------------|-----|
| SCT61450S-xxxxFDAR <sup>(1)</sup> | Tape & Reel    | 5000              | 450S            | 24   | FCTQFN4x4-24L       | 1   |
| SCT61450S-0001FDAR                | Tape & Reel    | 5000              | 450S            | 24   | FCTQFN4x4-24L       | 1   |

1) "xxxx" is the specific suffix code for different configuration, contact SCT for details

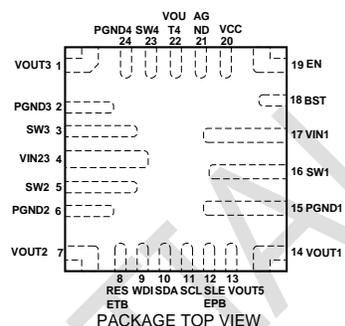
| PART NUMBER        | CHIP_ID | CONFIG_T1 | CONFIG_EN | CONFIG_PU1 | CONFIG_PU2 | VOUT2         | VOUT3         | I2C ADDRESS |
|--------------------|---------|-----------|-----------|------------|------------|---------------|---------------|-------------|
| SCT61450S-0001FDAR | 41h     | 00h       | 3Dh       | 00h        | 11h        | 06h<br>(1.1V) | 0Eh<br>(1.5V) | 38h         |

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted<sup>(1)</sup>

| DESCRIPTION                          | MIN                     | MAX                    | UNIT |
|--------------------------------------|-------------------------|------------------------|------|
| VIN, EN                              | -0.3                    | 42(46V trans<br>100ms) | V    |
| SW1                                  | -0.3(-1V trans<br>30ns) | 42                     | V    |
| BST-SW1                              | -0.3                    | 6                      | V    |
| Others                               | -0.3                    | 6                      | V    |
| Junction temperature <sup>(2)</sup>  | -40                     | 150                    | °C   |
| Storage temperature T <sub>STG</sub> | -65                     | 150                    | °C   |

## PIN CONFIGURATION



Top View: 24-Lead FCTQFN 4mmx4mm

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 175°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

## PIN FUNCTIONS

| NAME   | NO. | DESCRIPTION  |
|--------|-----|--|
| VOUT3  | 1   | Voltage sense for the output of Buck3. The device regulates VOUT3 voltage to the setting value. Connect this pin to LV Buck3 output voltage via short trace.   |
| PGND3  | 2   | Power ground pin of LV Buck3.  |
| SW3    | 3   | Regulator switching node of LV Buck3. Connect SW3 to an external power inductor.   |
| VIN23  | 4   | Supply voltage for LV Buck2 and Buck3. Must connect this pin to HV Buck1 output voltage directly. Connect a bypass bulk capacitor between this pin to ground. Recommend to put a high-frequency bypass ceramic capacitor to this pin as close as possible. |
| SW2    | 5   | Regulator switching node of LV Buck2. Connect SW2 to an external power inductor  |
| PGND2  | 6   | Power ground pin of LV Buck2.  |
| VOUT2  | 7   | Voltage sense for the output of Buck2. The device regulates VOUT2 voltage to the setting value. Connect this pin to LV Buck2 output voltage via short trace.   |
| RESETB | 8   | Open-Drain Reset Output. This output remains low for the programmed hold time after all outputs are built. Connect this pin to high level with a pull-up resistor. Float this pin if not used.   |
| WDI    | 9   | Window watchdog input.   |
| SDA    | 10  | Serial data line. Open-Drain I/O, connect this pin to high level with a pull-up resistor. Connect this pin to ground if not used.  |
| SCL    | 11  | Serial clock line. Connect this pin to ground if not used.   |
| SLEEPB | 12  | Sleep mode input, IC will enter SLEEP state if pull this pin to ground after blanking time. Pull this pin from low to logic high will wake up the IC and enter NORMAL state. Do not float this pin. Connect to logic high if not used.                     |
| VOUT5  | 13  | Output of the load switch. Connect a bypass capacitor between this pin to ground.  |

**PIN FUNCTIONS (continued)**

| NAME  | NO. | DESCRIPTION  |
|-------|-----|--|
| VOUT1 | 14  | Voltage sense for the output of Buck1. The device regulates VOUT1 voltage to the setting value. Power supply of internal load switch VOUT5. The device regulates VOUT1 voltage to the value of 3.3V typical. Connect this pin to HV Buck1 output voltage via short trace.  |
| PGND1 | 15  | Power ground pin of HV Buck1.  |
| SW1   | 16  | Regulator switching node of HV Buck1. Connect SW1 to an external power inductor.   |
| VIN   | 17  | Input supply voltage. Connect a local bypass capacitor from VIN pin to ground. Path from VIN pin to high frequency bypass capacitor and ground must be as short as possible.   |
| BST   | 18  | Power supply bias for high-side power MOSFET gate driver of Buck1. Connect a 0.1uF capacitor from BST pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.   |
| EN    | 19  | Enable pin. All five outputs will be activated once voltage upon EN reaches high threshold. The input voltage lockout threshold can be adjusted by connecting this pin to the input voltage through a resistor divider. The EN pin is internally pulled-down through 2.1MΩ resistor. Connect to VIN pin if not used. |
| VCC   | 20  | Output of the internal VCC regulator. Connect a ceramic bypass capacitor from this pin to PGND.  |
| AGND  | 21  | Analog ground pin of device. Connect this pin to power ground directly.  |
| VOUT4 | 22  | Output pin of LV Boost4. Put output capacitor between this pin and ground.   |
| SW4   | 23  | Regulator switching node of LV Boost4. Connect SW4 to an external power inductor.  |
| PGND4 | 24  | Power ground pin of LV Boost4.   |

# SCT61450S

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER         | DEFINITION                     | MIN | MAX  | UNIT |
|-------------------|--------------------------------|-----|------|------|
| V <sub>IN</sub>   | Input voltage range            | 3.5 | 36   | V    |
| V <sub>OUT2</sub> | LV buck2 output voltage range  | 0.8 | 2.35 | V    |
| V <sub>OUT3</sub> | LV buck3 output voltage range  | 0.8 | 2.35 | V    |
| T <sub>J</sub>    | Operating junction temperature | -40 | 150  | °C   |

## ESD RATINGS

| PARAMETER        | DEFINITION                                  | MIN | MAX | UNIT |
|------------------|---|-----|-----|------|
| V <sub>ESD</sub> | Human Body Model(HBM), per AEC-Q100-002     | -2  | +2  | kV   |
|                  | Charged Device Model(CDM), per AEC-Q100-011 | -1  | +1  | kV   |

## THERMAL INFORMATION

| PARAMETER              | THERMAL METRIC  | TQFN-24 | UNIT |
|------------------------|---|---------|------|
| R <sub>θJA</sub>       | Junction to ambient thermal resistance <sup>(1)</sup>       | 39.68   | °C/W |
| Ψ <sub>JT</sub>        | Junction-to-top characterization parameter                  | 1.78    |      |
| Ψ <sub>JB</sub>        | Junction-to-board characterization parameter <sup>(1)</sup> | 3.26    |      |
| R <sub>θJC (top)</sub> | Junction to case (top) thermal resistance <sup>(1)</sup>    | 24.67   |      |
| R <sub>θJB</sub>       | Junction to board thermal resistance <sup>(1)</sup>         | 3.46    |      |

(1) SCT provides R<sub>θJA</sub> and R<sub>θJC</sub> numbers only as reference to estimate junction temperatures of the devices. R<sub>θJA</sub> and R<sub>θJC</sub> are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61450S is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61450S. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R<sub>θJA</sub> and R<sub>θJC</sub>.

**ELECTRICAL CHARACTERISTICS**

$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 150^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

| SYMBOL                         | PARAMETER                       | TEST CONDITION  | MIN | TYP  | MAX | UNIT      |
|--------------------------------|---------------------------------|---|-----|------|-----|-----------|
| <b>Power Supply and Output</b> |                                 |   |     |      |     |           |
| $V_{IN}$                       | Operating input voltage         |   | 3.5 |      | 36  | V         |
| $V_{IN\_UVLO\_RISING}$         | Input UVLO rising threshold     | $VIN\_START[1:0]=00b$   | 3   | 3.2  | 3.4 | V         |
|                                |                                 | $VIN\_START[1:0]=01b$   | 3.8 | 4    | 4.2 | V         |
|                                |                                 | $VIN\_START[1:0]=10b$   | 4.8 | 5    | 5.2 | V         |
|                                |                                 | $VIN\_START[1:0]=11b$   | 5.8 | 6    | 6.2 | V         |
| $V_{IN\_UVLO\_FALLING}$        | Input UVLO falling threshold    | $VIN\_STOP[1:0]=00b$  | 2.5 | 2.8  | 3.1 | V         |
|                                |                                 | $VIN\_STOP[1:0]=01b$  | 3.2 | 3.5  | 3.8 | V         |
|                                |                                 | $VIN\_STOP[1:0]=10b$  | 4.2 | 4.5  | 4.8 | V         |
|                                |                                 | $VIN\_STOP[1:0]=11b$  | 5.2 | 5.5  | 5.8 | V         |
| $V_{IN\_OVP}$                  | Input OVP                       | $V_{IN}$ rising   | 40  | 43   | 45  | V         |
| $V_{IN\_OVP\_HYS}$             | Hysteresis                      |   |     | 3    |     | V         |
| $I_{SD}$                       | Shutdown current                | EN low  |     | 0.5  | 10  | $\mu A$   |
| $I_q$                          | Quiescent current from $V_{IN}$ | No load, FCCM, $V_{OUT1} = 3.3V^{(1)}$                        |     | 20   |     | mA        |
|                                |                                 | No load, PFM, $V_{OUT1} = 3.3V^{(1)}$                         |     | 1    |     | mA        |
|                                |                                 | Sleep mode, $V_{OUT1} = 3.3V$ , no load, other rails disabled |     | 0.5  | 2   | mA        |
|                                |                                 | All channels off via I2C                                      |     | 0.85 | 2   | mA        |
| <b>VCC Power</b>               |                                 |   |     |      |     |           |
| $V_{CC}$                       | Internal linear regulator       |   | 4.5 | 4.7  | 4.9 | V         |
| $V_{CC\_UVLO}$                 | VCC UVLO                        | $V_{CC}$ rising   | 2.6 | 2.8  | 3   | V         |
| $V_{CC\_UVLO\_HYS}$            | Hysteresis                      |   |     | 200  |     | mV        |
| $V_{CCOV\_THR}$                | VCC OV Threshold                | $V_{CC}$ rising   | 5   | 5.3  | 5.6 | V         |
| $V_{CCOV\_HYS}$                | Hysteresis                      |   |     | 250  |     | mV        |
| $I_{VCC}$                      | VCC sourcing current limit      | $V_{CC} = 4.4V$   |     | 70   |     | mA        |
| <b>Enable and RESETB</b>       |                                 |   |     |      |     |           |
| $V_{EN\_H}$                    | Enable high threshold           | $V_{EN}$ ramping up   |     | 1.2  | 1.4 | V         |
| $V_{EN\_L}$                    | Enable low threshold            | $V_{EN}$ ramping down   | 0.8 | 1.0  |     | V         |
| $R_{EN\_DOWN}$                 | Enable pin pull-down resistance |   |     | 2.1  |     | $M\Omega$ |
| $T_{RSTB}$                     | RESETB pin holding time         | $RESETB\_HT[1:0]=00b$   |     | 10   |     | ms        |
|                                |                                 | $RESETB\_HT[1:0]=01b$   |     | 20   |     |           |
|                                |                                 | $RESETB\_HT[1:0]=10b$   |     | 30   |     |           |
|                                |                                 | $RESETB\_HT[1:0]=11b$   |     | 40   |     |           |
| $I_{RST\_LKG}$                 | Output-High leakage current     |   |     |      | 1   | $\mu A$   |
| $V_{RST\_L}$                   | RESETB output low level         | Sinking -2mA  |     |      | 0.2 | V         |

# SCT61450S

## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 150^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

| SYMBOL                  | PARAMETER                                    | TEST CONDITION                        | MIN  | TYP | MAX | UNIT       |
|-------------------------|--|---------------------------------------|------|-----|-----|------------|
| <b>VOUT1 (HV Buck)</b>  |  |                                       |      |     |     |            |
| $V_{ACC1}$              | Voltage accuracy                             | $T_J = 25^{\circ}C$                   | -1   |     | 1   | %          |
|                         |  | $T_J = -40^{\circ}C\sim 150^{\circ}C$ | -1.5 |     | 1.5 | %          |
| $R_{DSON\_H1}$          | High-side MOSFET on-resistance               | $V_{BOOT}-V_{SW}=5V$                  |      | 75  | 150 | m $\Omega$ |
| $R_{DSON\_L1}$          | Low-side MOSFET on-resistance                |                                       |      | 50  | 120 | m $\Omega$ |
| $I_{LIM\_HS1}$          | High-side power MOSFET current limit         |                                       | 4.2  | 5.2 | 6.2 | A          |
| $I_{LIM\_LSP1}$         | Low-side power MOSFET positive current limit |                                       | 3.2  | 4.2 | 5.2 | A          |
| $I_{LIM\_LSN1}$         | Low-side power MOSFET negative current limit |                                       | 0.8  | 2   | 3.2 | A          |
| $R_{DIS1}$              | Discharge resistance                         | Output disabled                       |      | 100 | 200 | $\Omega$   |
| $t_{ON\_MIN1}$          | Minimum on-time                              |                                       |      | 80  |     | ns         |
| $\theta_{Phase1}^{(1)}$ | Switching phase                              |                                       |      | 0   |     | deg        |
| <b>VOUT2 (LV Buck)</b>  |  |                                       |      |     |     |            |
| $V_{S2}^{(1)}$          | Supply voltage range                         |                                       | 3    |     | 5.5 | V          |
| $V_{ACC2}$              | Voltage accuracy                             | $T_J = 25^{\circ}C$                   | -1   |     | 1   | %          |
|                         |  | $T_J = -40^{\circ}C\sim 150^{\circ}C$ | -1.5 |     | 1.5 | %          |
| $R_{DSON\_H2}$          | High-side MOSFET on-resistance               |                                       |      | 65  | 150 | m $\Omega$ |
| $R_{DSON\_L2}$          | Low-side MOSFET on-resistance                |                                       |      | 50  | 120 | m $\Omega$ |
| $I_{LIM\_HS2}$          | High-side power MOSFET current limit         |                                       | 2.8  | 3.6 | 4.4 | A          |
| $I_{LIM\_LSP2}$         | Low-side power MOSFET positive current limit |                                       | 2.2  | 3.2 | 4.2 | A          |
| $I_{LIM\_LSN2}$         | Low-side power MOSFET negative current limit |                                       | 1    | 2   | 3   | A          |
| $R_{DIS2}$              | Discharge resistance                         | Output disabled                       |      | 50  | 100 | $\Omega$   |
| $t_{ON\_MIN2}$          | Minimum on-time                              |                                       |      | 90  |     | ns         |
| $\theta_{Phase2}^{(1)}$ | Switching phase                              |                                       |      | 0   |     | deg        |
| <b>VOUT3 (LV Buck)</b>  |  |                                       |      |     |     |            |
| $V_{S3}^{(1)}$          | Supply voltage range                         |                                       | 3    |     | 5.5 | V          |
| $V_{ACC3}$              | Voltage accuracy                             | $T_J = 25^{\circ}C$                   | -1   |     | 1   | %          |
|                         |  | $T_J = -40^{\circ}C\sim 150^{\circ}C$ | -1.5 |     | 1.5 | %          |
| $R_{DSON\_H3}$          | High-side MOSFET on-resistance               |                                       |      | 65  | 150 | m $\Omega$ |
| $R_{DSON\_L3}$          | Low-side MOSFET on-resistance                |                                       |      | 50  | 120 | m $\Omega$ |
| $I_{LIM\_HS3}$          | High-side power MOSFET current limit         |                                       | 2.8  | 3.6 | 4.4 | A          |

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 150^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

| SYMBOL                  | PARAMETER                                    | TEST CONDITION  | MIN | TYP | MAX | UNIT     |
|-------------------------|--|-----------------|-----|-----|-----|----------|
| $I_{LIM\_LSP3}$         | Low-side power MOSFET positive current limit |                 | 2.2 | 3.2 | 4.2 | A        |
| $I_{LIM\_LSN3}$         | Low-side power MOSFET negative current limit |                 | 1   | 2   | 3   | A        |
| $R_{DIS3}$              | Discharge resistance                         | Output disabled |     | 55  | 100 | $\Omega$ |
| $t_{ON\_MIN3}$          | Minimum on-time                              |                 |     | 90  |     | ns       |
| $\theta_{Phase3}^{(1)}$ | Switching phase                              |                 |     | 180 |     | deg      |

**VOUT4 (LV Boost)**

|                         |   |                                       |      |     |     |            |
|-------------------------|---|---------------------------------------|------|-----|-----|------------|
| $V_{S4}^{(1)}$          | $V_{S4}^{(1)}$                                |                                       | 3    |     | 4.5 | V          |
| $V_{ACC4}$              | Voltage accuracy                              | $T_J = 25^{\circ}C$                   | -1   |     | 1   | %          |
|                         |   | $T_J = -40^{\circ}C\sim 150^{\circ}C$ | -1.5 |     | 1.5 | %          |
| $R_{DSON\_H4}$          | High-side MOSFET on-resistance                |                                       |      | 180 | 280 | m $\Omega$ |
| $R_{DSON\_L4}$          | Low-side MOSFET on-resistance                 |                                       |      | 60  | 100 | m $\Omega$ |
| $I_{LIM\_LS4}$          | Low-side power MOSFET current limit           |                                       | 1.4  | 2   | 2.6 | A          |
| $I_{LIM\_HSP4}$         | High-side power MOSFET current limit          |                                       | 0.9  | 1.4 | 1.9 | A          |
| $I_{LIM\_HSN4}$         | High-side power MOSFET negative current limit |                                       | 200  | 500 | 800 | mA         |
| $R_{DIS4}$              | Discharge resistance                          | Output disabled                       |      | 200 | 300 | $\Omega$   |
| $t_{ON\_MIN4}$          | Minimum on-time                               |                                       |      | 80  |     | ns         |
| $\theta_{Phase4}^{(1)}$ | Switching phase                               |                                       |      | 180 |     | deg        |
| $R_{DSON\_H4}$          | High-side MOSFET on-resistance                |                                       |      | 180 | 280 | m $\Omega$ |

**VOUT5 (Load Switch)**

|                |                                |                 |     |     |     |            |
|----------------|--------------------------------|-----------------|-----|-----|-----|------------|
| $V_{S5}$       | Supply voltage range           |                 | 3   |     | 4.5 | V          |
| $R_{DSON\_H5}$ | High-side MOSFET on-resistance |                 |     | 100 | 200 | m $\Omega$ |
| $I_{LIM\_HS5}$ | Power MOSFET current limit     |                 | 1.5 | 2   | 2.5 | A          |
| $R_{DIS5}$     | Discharge resistance           | Output disabled |     | 100 | 200 | $\Omega$   |

**Soft Start and Delay**

|                        |                             |              |   |     |    |    |
|------------------------|-----------------------------|--------------|---|-----|----|----|
| $T_{SS}$               | Soft-start time             | SS=0 to 1.1V |   | 1   |    | ms |
| $T_{EN\_ON}^{(1)}$     | Device on time from EN high |              |   | 2.8 |    | ms |
| $T_{ON\_DELAY2}^{(1)}$ | On delay for VOUT2          |              | 0 |     | 75 | ms |
| $T_{ON\_DELAY3}^{(1)}$ | On delay for VOUT3          |              | 0 |     | 75 | ms |
| $T_{ON\_DELAY4}^{(1)}$ | On delay for VOUT4          |              | 0 |     | 75 | ms |
| $T_{ON\_DELAY5}^{(1)}$ | On delay for VOUT5          |              | 0 |     | 75 | ms |

# SCT61450S

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub>=12V, T<sub>J</sub>=-40°C~150°C, typical values are tested under 25°C.

| SYMBOL                          | PARAMETER   | TEST CONDITION                        | MIN  | TYP   | MAX  | UNIT |
|---------------------------------|---|---------------------------------------|------|-------|------|------|
| <b>Switching Frequency</b>      |   |                                       |      |       |      |      |
| F <sub>SW</sub>                 | LV Buck&Boost Switching frequency                   |                                       | 1.98 | 2.2   | 2.42 | MHz  |
| F <sub>SW1</sub>                | HV Buck switching frequency                         | High frequency option                 | 1.98 | 2.2   | 2.42 | MHz  |
|                                 |   | Low frequency option                  | 360  | 400   | 440  | kHz  |
| F <sub>FSS_PERIOD</sub>         | Frequency spread spectrum period                    | FSS_PERIOD[0]=0b                      |      | 4.5   |      | kHz  |
|                                 |   | FSS_PERIOD[0]=1b                      |      | 10    |      |      |
| F <sub>FSS_RANGE</sub>          | Frequency spread spectrum in percentage of Fsw      | FSS_RANGE[1:0]=00b                    |      | ±5    |      | %    |
|                                 |   | FSS_RANGE[1:0]=01b                    |      | ±2.5  |      |      |
|                                 |   | FSS_RANGE[1:0]=10b                    |      | ±7.5  |      |      |
|                                 |   | FSS_RANGE[1:0]=11b                    |      | ±3.75 |      |      |
| <b>Protection</b>               |   |                                       |      |       |      |      |
| V <sub>OVUVACC</sub>            | OV/UV accuracy                                      |                                       | -1.5 |       | 1.5  | %    |
| V <sub>OVTH</sub>               | Output over-voltage threshold for all outputs       | PG1/2/3/4/5_SEL[1:0]=01, VOUT rising  |      | 106   |      | %    |
|                                 |   | Hysteresis                            |      | 2     |      | %    |
| V <sub>UVTH</sub>               | Output under-voltage threshold for all outputs      | PG1/2/3/4/5_SEL[1:0]=01, VOUT falling |      | 94    |      | %    |
|                                 |   | Hysteresis                            |      | 2     |      | %    |
| V <sub>DOVPTH</sub>             | Output deep over-voltage threshold for all outputs  | DEEP_OVP_SEL[1:0]=00, VOUT rising     | 110  | 115   | 120  | %    |
|                                 |   | Hysteresis                            |      | 2     |      | %    |
| V <sub>DUVPTH</sub>             | Output deep under-voltage threshold for all outputs | DEEP_UVP_SEL[1:0]=00, VOUT falling    | 70   | 75    | 80   | %    |
|                                 |   | Hysteresis                            |      | 2     |      | %    |
| T <sub>HIC</sub> <sup>(1)</sup> | Hiccup time   |                                       |      | 80    |      | ms   |
| T <sub>SD</sub>                 | Thermal shutdown threshold                          | T <sub>J</sub> rising                 |      | 175   |      | °C   |
|                                 | Hysteresis  |                                       |      | 20    |      | °C   |
| <b>Low Power Interface</b>      |   |                                       |      |       |      |      |
| R <sub>SLEEPB</sub>             | SLEEPB Input Pulldown                               | EN high                               |      | 1.8   |      | MΩ   |
| V <sub>SLEEPB_HI</sub>          | Threshold for SLEEPB pin                            | SLEEPB voltage rising                 |      | 1.2   | 1.4  | V    |
| V <sub>SLEEPB_LO</sub>          |   | SLEEPB voltage falling                | 0.8  | 1     |      | V    |
| <b>Watch Dog Interface</b>      |   |                                       |      |       |      |      |
| V <sub>WDL_HI</sub>             | Threshold for WDI pin                               | WDI voltage rising                    |      | 1.2   | 1.4  | V    |
| V <sub>WDL_LO</sub>             |   | WDI voltage falling                   | 0.8  | 1     |      | V    |
| T <sub>WDL_DEG_RISING</sub>     | Deglitch time for WDI pin                           | WDI voltage rising                    |      | 30    |      | us   |
| T <sub>WD</sub>                 | Watchdog timer accuracy                             |                                       | -10  |       | 10   | %    |

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 150^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

**I2C Interface**

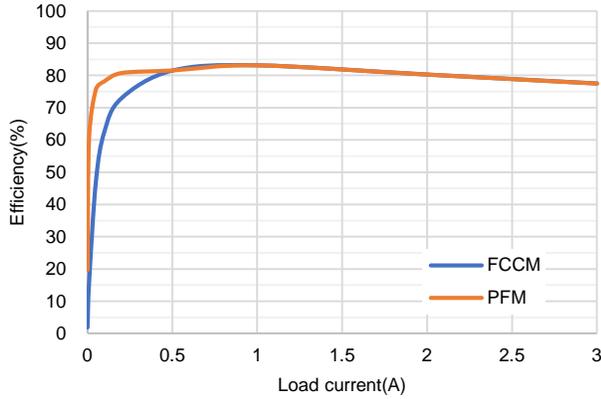
|                     |  |                |     |     |
|---------------------|--|----------------|-----|-----|
| $V_{IH}$            | High-level input voltage               |                | 1.2 | V   |
| $V_{IL}$            | Low-level input voltage                |                | 0.4 | V   |
| $V_{OL}$            | Low-level output voltage               | $I_{SINK}=4mA$ | 0.4 | V   |
| $F_{SCL}^{(1)}$     | SCL clock frequency                    |                | 1   | MHz |
| $T_{LOW}^{(1)}$     | Low period of the SCL clock            |                | 500 | ns  |
| $T_{HIGH}^{(1)}$    | High period of the SCL clock           |                | 260 | ns  |
| $T_{HD\_STA}^{(1)}$ | Hold time (repeated) START condition   |                | 260 | ns  |
| $T_{SU\_STA}^{(1)}$ | Set-up time (repeated) START condition |                | 260 | ns  |
| $T_{HD\_DAT}^{(1)}$ | Data hold time                         |                | 0   | ns  |
| $T_{SU\_DAT}^{(1)}$ | Data set-up time                       |                | 50  | ns  |
| $T_R^{(1)}$         | Rise time of both SCL and SDA signals  |                | 120 | ns  |
| $T_F^{(1)}$         | Fall time of both SCL and SDA signals  |                | 120 | ns  |
| $T_{SU\_STO}^{(1)}$ | Set-up time for STOP condition         |                | 260 | ns  |
| $CB^{(1)}$          | Capacitive load for each bus line      |                | 550 | pF  |

(1) Guaranteed by sample and design characterization, not tested in production.

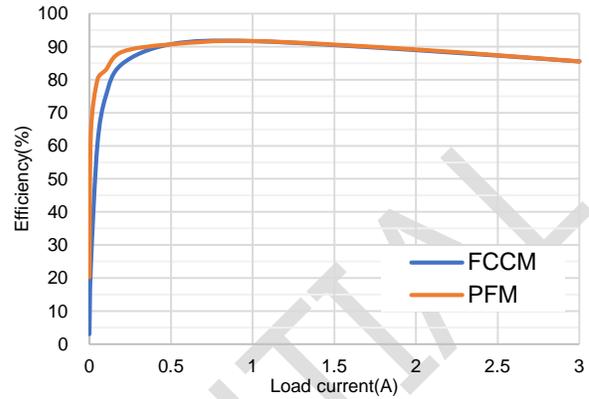
# SCT61450S

## TYPICAL CHARACTERISTICS

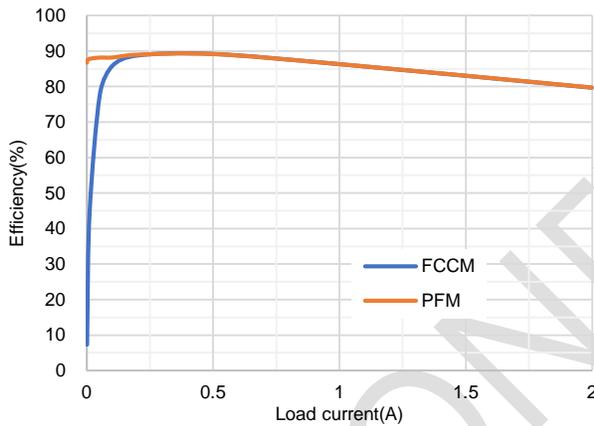
$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , unless otherwise noted.



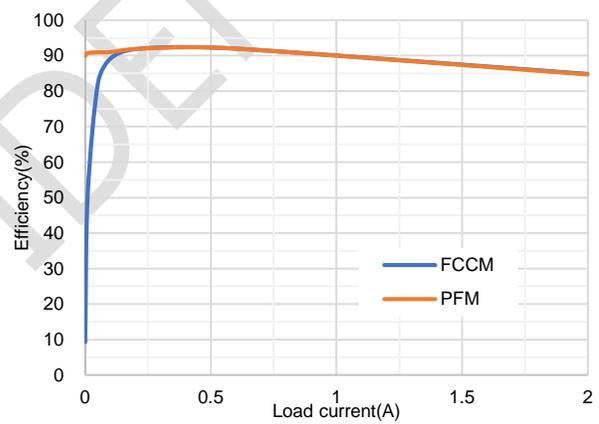
Buck1 Efficiency vs Load Current,  $V_{OUT1}=3.3V$ ,  $f_{SW1}=2.2MHz$



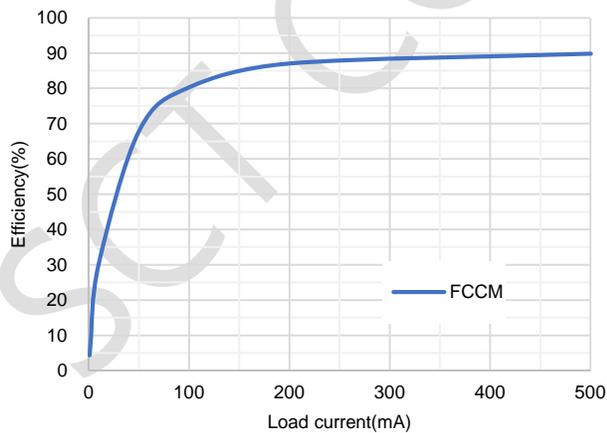
Buck1 Efficiency vs Load Current,  $V_{OUT1}=3.3V$ ,  $f_{SW1}=400kHz$



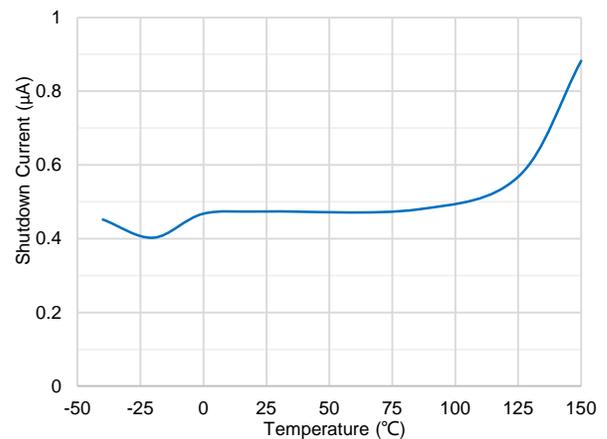
Buck2/3 Efficiency vs Load Current,  $V_{OUT2/3}=1.2V$



Buck2/3 Efficiency vs Load Current,  $V_{OUT2/3}=1.8V$



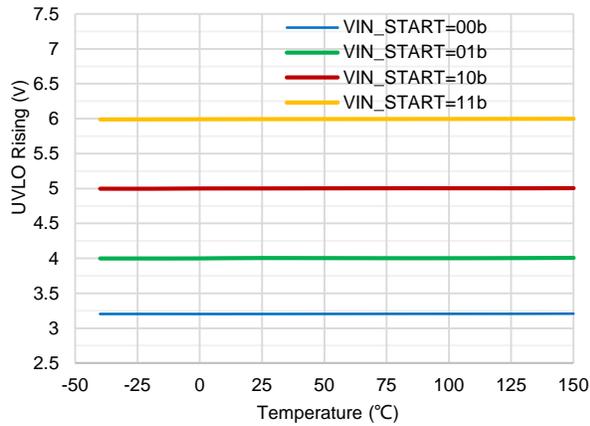
Boost Efficiency vs. Load Current,  $V_{OUT4}=5V$



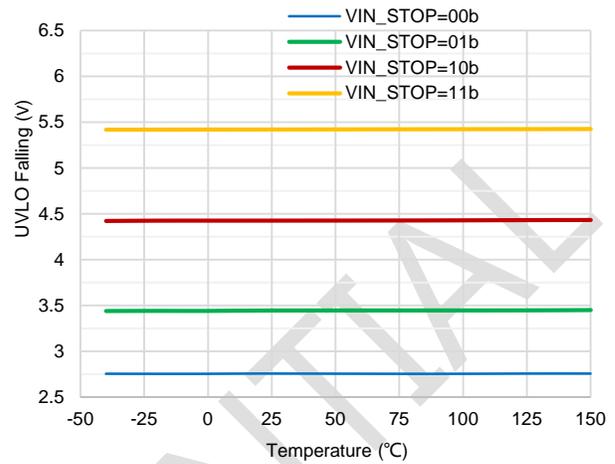
Shutdown Current vs. Temperature

## TYPICAL CHARACTERISTICS (continued)

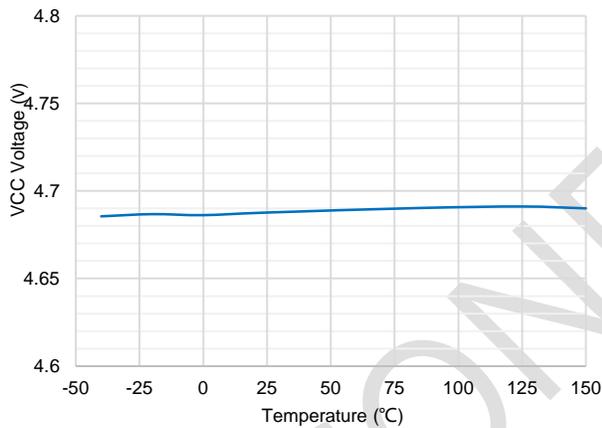
$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , unless otherwise noted.



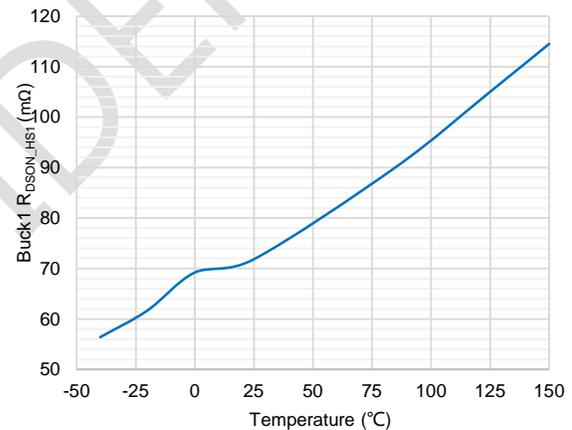
UVLO Rising Threshold vs. Temperature



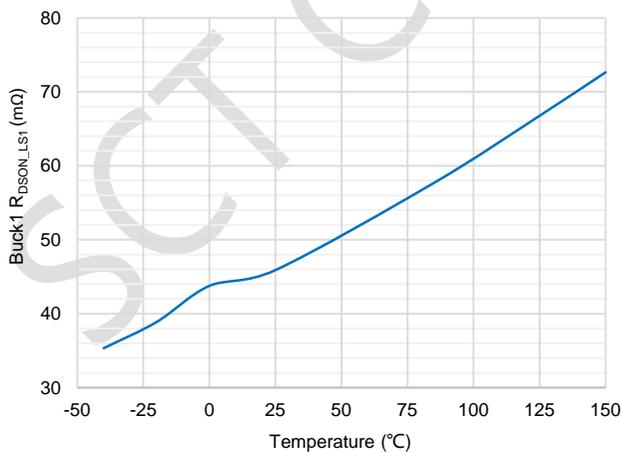
UVLO Falling Threshold vs. Temperature



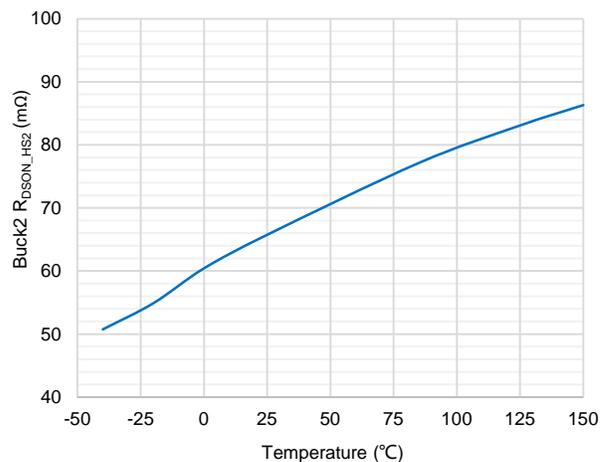
VCC vs. Temperature



Buck1 R<sub>DSON\_HS1</sub> vs. Temperature



Buck1 R<sub>DSON\_LS1</sub> vs. Temperature

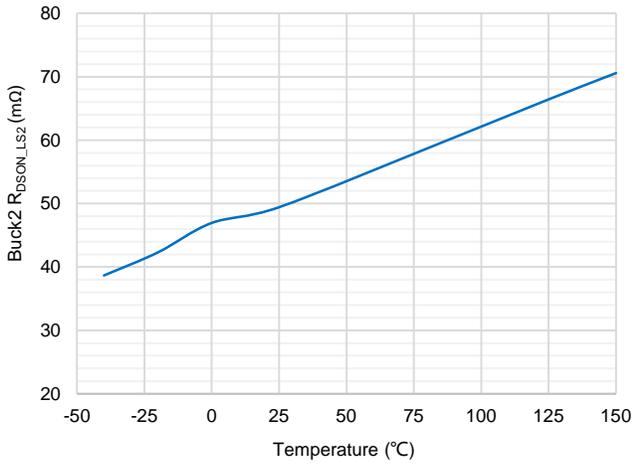


Buck2 R<sub>DSON\_HS2</sub> vs. Temperature

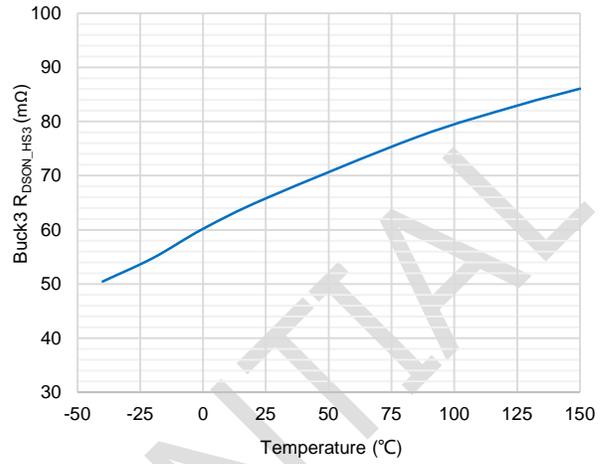
# SCT61450S

## TYPICAL CHARACTERISTICS (continued)

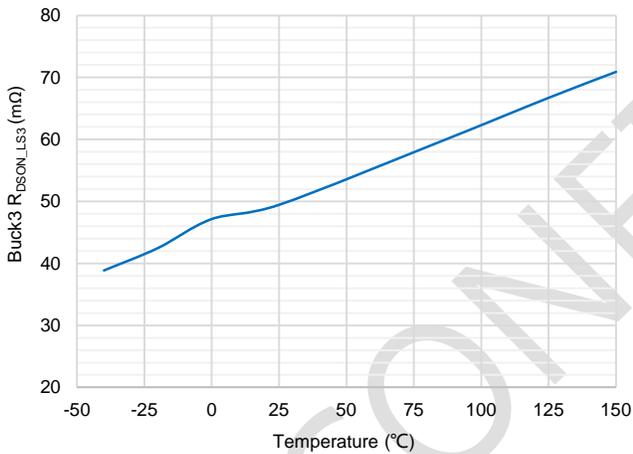
$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , unless otherwise noted.



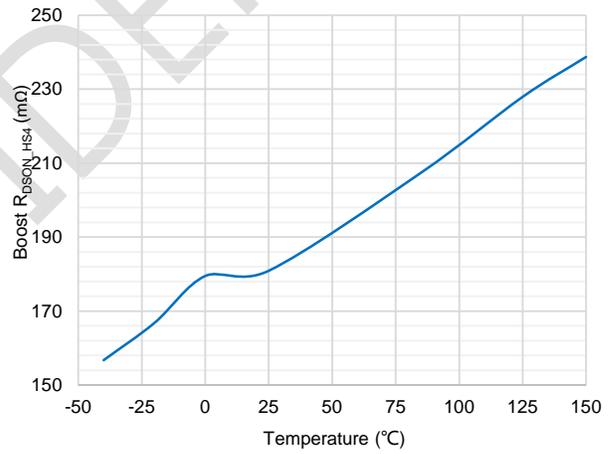
Buck2  $R_{DSON\_LS2}$  vs. Temperature



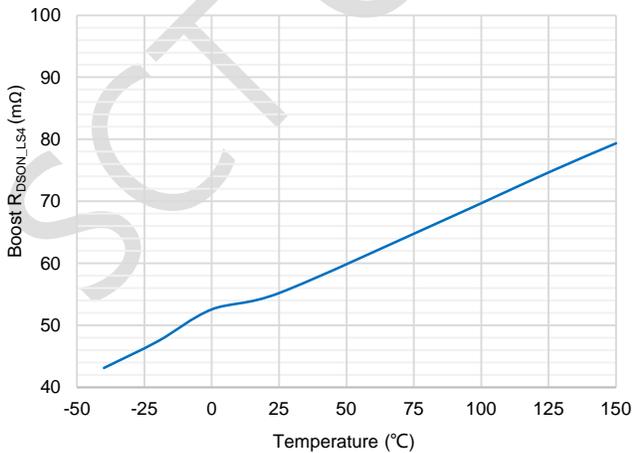
Buck3  $R_{DSON\_HS3}$  vs. Temperature



Buck3  $R_{DSON\_LS3}$  vs. Temperature



Boost  $R_{DSON\_HS4}$  vs. Temperature



Boost  $R_{DSON\_LS4}$  vs. Temperature

FUNCTIONAL BLOCK DIAGRAM

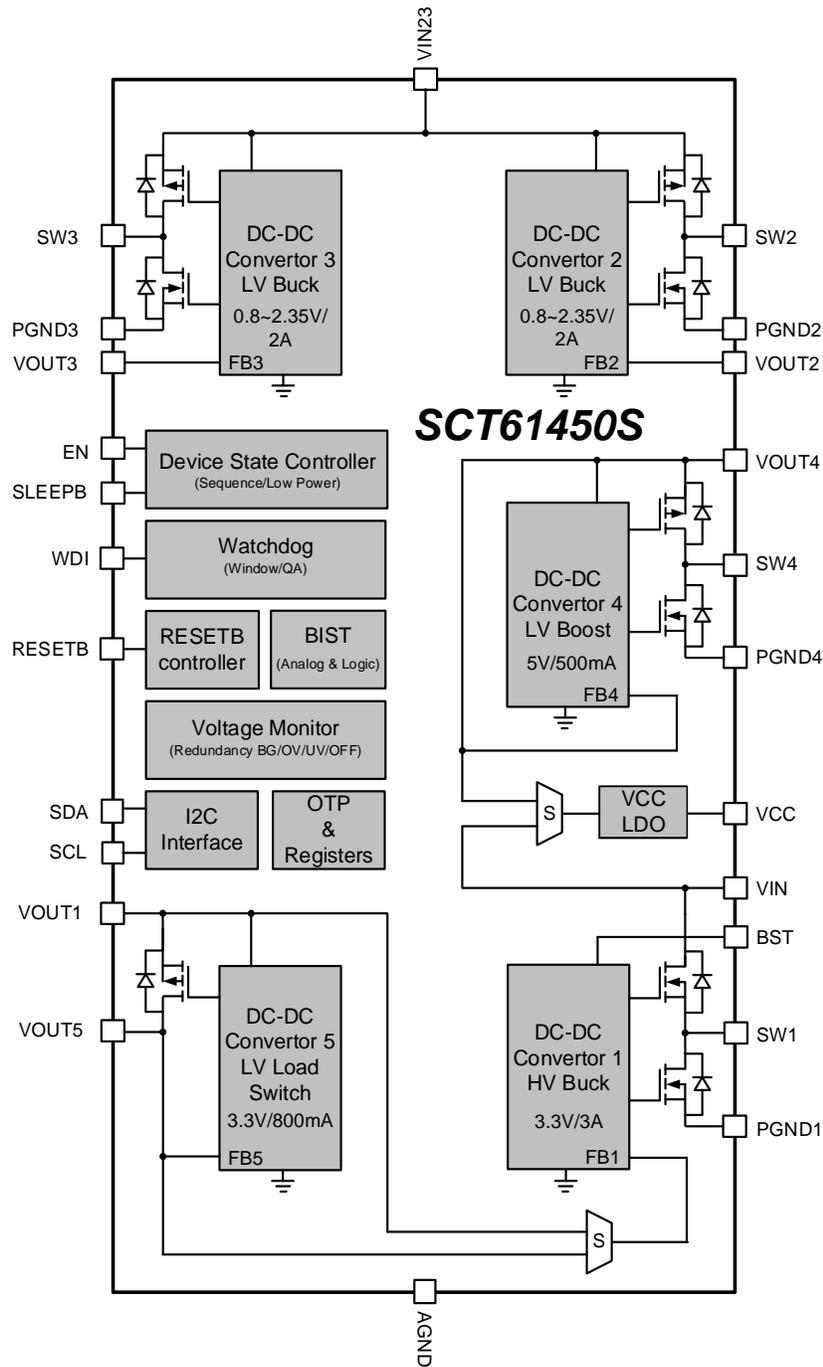


Figure 1. Functional Block Diagram

## OPERATION

### Overview

The SCT61450S device is a wide input power management IC with five channels output. The device is designed for SoCs in automotive and industrial radar applications. The SCT61450S integrates one 3A HV Buck, two identical 2A LV Bucks, one 500mA LV Boost and one 800mA LV Load Switch. Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61450S device has protection features such as thermal shutdown, short-circuit protection and over-voltage/under-voltage protection. Sleep mode reduces the total supply current to 1 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked before power up stage. Safety features ensure compliance with ISO26262 standard and functional safety up to ASIL-B level.

### Operating State Machine

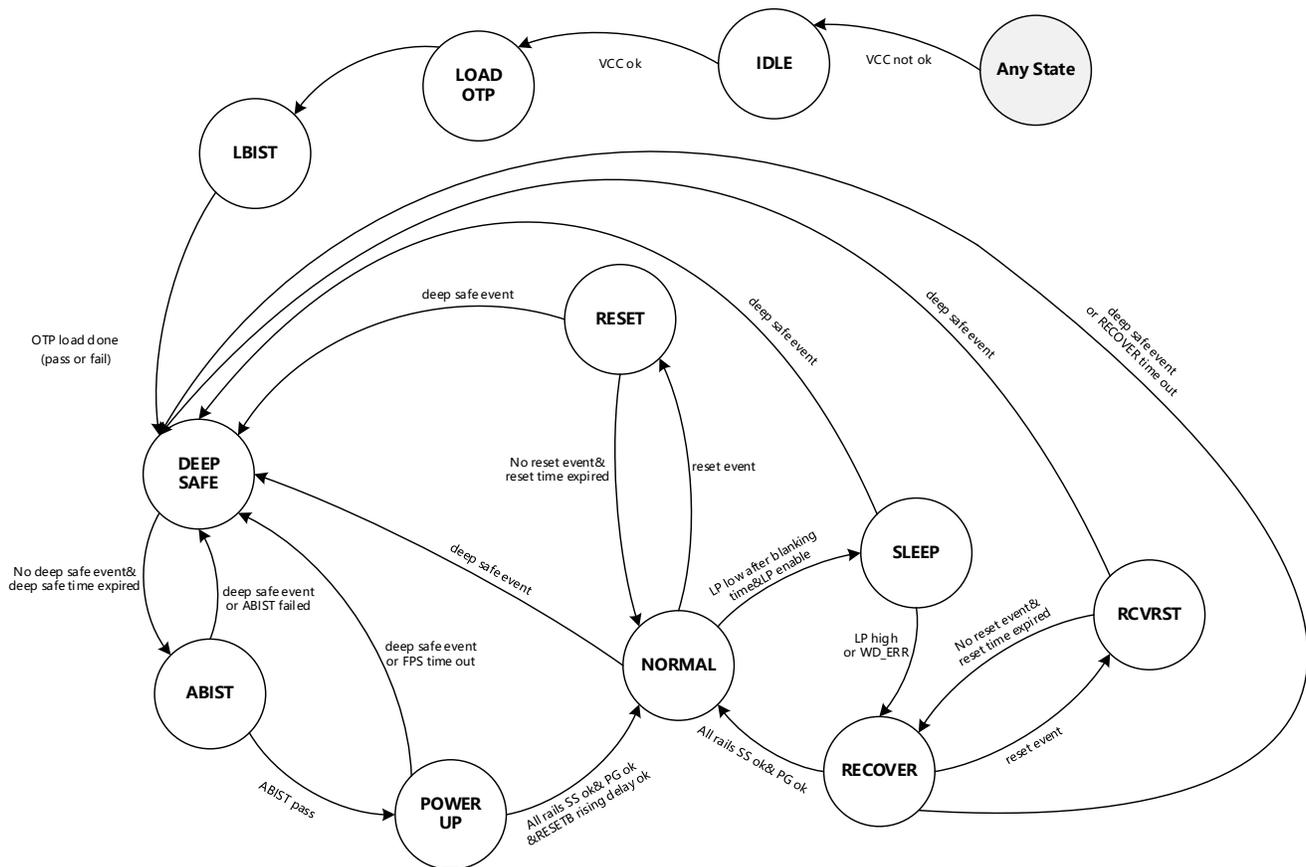


Table 1. State and Function Matrix Table

| State    | Function |          |                |          |          |          |           |              |          |        |                  |     |
|----------|----------|----------|----------------|----------|----------|----------|-----------|--------------|----------|--------|------------------|-----|
|          | I2C      | OTP load | Register reset | HV BUCK1 | LV BUCK2 | LV BUCK3 | LV BOOST4 | LOAD SWITCH5 | Watchdog | OCP    | DOVP/DUVP detect | TSD |
| IDLE     | OFF      | OFF      | ON             | OFF      | OFF      | OFF      | OFF       | OFF          | OFF      | OFF    | OFF              | OFF |
| LOADOTP  | OFF      | ON       | OFF            | OFF      | OFF      | OFF      | OFF       | OFF          | OFF      | OFF    | OFF              | OFF |
| LBIST    | OFF      | OFF      | OFF            | OFF      | OFF      | OFF      | OFF       | OFF          | OFF      | OFF    | OFF              | OFF |
| DEEPSAFE | ON       | OFF      | OFF            | OFF      | OFF      | OFF      | OFF       | OFF          | OFF      | OFF    | OFF              | OFF |
| ABIST    | ON       | OFF      | OFF            | OFF      | OFF      | OFF      | OFF       | OFF          | OFF      | OFF    | OFF              | OFF |
| POWERUP  | ON       | OFF      | OFF            | UP       | UP       | UP       | UP        | UP           | UP       | OFF    | ON               | ON  |
| NORMAL   | ON       | OFF      | OFF            | ON       | ON       | ON       | ON        | ON           | ON       | ON     | ON               | ON  |
| RESET    | ON       | OFF      | OFF            | ON       | ON       | ON       | ON        | ON           | ON       | OFF    | ON               | ON  |
| SLEEP    | OFF      | OFF      | OFF            | ON       | ON/OFF   | ON/OFF   | ON/OFF    | ON/OFF       | ON/OFF   | ON/OFF | ON               | ON  |
| RECOVER  | ON       | OFF      | OFF            | ON       | ON/UP    | ON/UP    | ON/UP     | ON/UP        | ON/UP    | ON     | ON               | ON  |
| RCVRST   | ON       | OFF      | OFF            | ON       | ON/UP    | ON/UP    | ON/UP     | ON/UP        | ON/UP    | OFF    | ON               | ON  |

Table 2. State and Functional Pin Matrix Table

| State    | SLEEPB    | RESETB    |
|----------|-----------|-----------|
| IDLE     | Tri-state | Tri-state |
| LOADOTP  | X         | LOW       |
| DEEPSAFE | X         | LOW       |
| ABIST    | X         | LOW       |
| POWERUP  | X         | LOW       |
| NORMAL   | HIGH      | HIGH      |
| RESET    | X         | LOW       |
| SLEEP    | LOW       | HIGH      |
| RECOVER  | X         | HIGH      |
| RCVRST   | X         | LOW       |

## IDLE State

The device will enter IDLE state whenever VCC is below the UVLO threshold. All functional blocks are disabled and all registers are reset. The device will exit IDLE state and jump to LOADOTP state only when VCC reaches its rising threshold 2.8V.

## LOADOTP State

Once the device enters OTPLOAD state, the OTP CRC mechanism will be activated and check through all data. Only when CRC check is passed, the device will load all non-volatile memory to register. And after that, the device will enter LBIST state regardless of CRC check pass or fail. The CRC check result will be recorded in register **SYS\_STATE**.

## LBIST State

The diagnostics of the monitoring and protection circuits in the digital core is performed by the LBIST. The LBIST is implemented in this state and check result will be recorded in register **SYS\_STATE**. When LBIST is complete and passed, the device transit to DEEPSAFE state immediately. If failed, the device will stay in LBIST and no functional circuit will be activated. There is a tradeoff between LBIST diagnostic coverage and running time, the LBIST can be disabled by programmed configuration in factory.

## DEEPSAFE State

In DEEPSAFE state, all power rails are shut off and indicator pins are pulled low. Regardless of current state, the device will always jump to DEEPSAFE state when any deep safe event occurs. I2C interface and thermal shutdown protection are activated. MCU is able to communicate with device through I2C and read fault register to locate fault. If there is no deep safe event and deep safe timeout is expired, the device will enter ABIST state automatically.

Deep safe events are listed as below:

- VOUT1's output is out of deep OV/UV protection range or OCP
- VOUT2's output is out of deep OV/UV protection range or OCP
- VOUT3's output is out of deep OV/UV protection range or OCP
- VOUT4's output is out of deep OV/UV protection range or OCP

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- VOUT5's output is out of deep OV/UV protection range or OCP
- Tj reaches Thermal Shutdown Point
- VIN/EN UVLO
- VCC OVP
- VIN OVP
- RESETB Stuck
- Loss of ground

## ABIST State

To ensure safety mechanism work well, the device will check through all critical analog comparators before output start-up. If ABIST check is failed, the device will go back to DEEPSAFE state. ABIST will be implemented every time SCT61450S enter ABIST state, the device will transit to POWERUP state once ABIST is passed. Any ABIST failure will be recorded in register **SYS\_STATE**.

## POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG\_PU1** and **CONFIG\_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state and RESETB will output high. If deep safe event occurs, the state will transit to DEEPSAFE state directly.

## NORMAL State

The NORMAL state is the normal running of device with all outputs on. The RESETB pin is released after specific delay time upon entering this state. If watchdog is enabled by register **CONFIG\_WD3**, watchdog window will start after setting delay time. The delay time is configured by **WD\_1UD[2:0]** in register **CONFIG\_WD3**. MCU should feed the watchdog via WDI pin or write answer to specified register periodically. When operating in NORMAL state, the device will go to RESET state once reset event occurs. When **LOWPOWER\_EN[0]** = 1, the device goes to SLEEP state if SLEEPB pin is pulled low.

## RESET State

All outputs keep on in this state, the device will transit from NORMAL state to RESET state when any of below reset event occurs:

- VOUT1's output is out of OV/UV protection range
- VOUT2's output is out of OV/UV protection range
- VOUT3's output is out of OV/UV protection range
- VOUT4's output is out of OV/UV protection range
- VOUT5's output is out of OV/UV protection range
- Watchdog Failure

When the device enters RESET state, the RESETB pin will assert for a holding time. The device will go back to NORMAL state automatically once the holding time is expired and no reset event, which can be configured in register **CONFIG\_T1** via I2C. Upon entering NORMAL state Watchdog failure counter will be reset and start running again. Then MCU should feed the watchdog again.

## SLEEP State

SLEEPB pin is monitored during NORMAL state. When the SLEEPB pin is pulled low longer than blank time and **LOWPOWER\_EN[0]**=1, the device will transit to SLEEP state. This is an extremely power-saving state with VOUT1

rail on, other rails are optional depending on register **CONFIG\_ENLP**. Most unnecessary circuits will turn off to save power consumption. Deep safe event is still valid to provide protection. Note the RESETB pin is still high during this state to keep MCU alive. Once SLEEPB pin is pulled high longer than deglitch time, the device will exit from sleep mode and go to RECOVER state. The rest channels will then recover.

## RECOVER State

Once the device is awake from sleep mode, the RECOVER state is an intermediate state before device go back to NORMAL state. The channels which are disabled in SLEEP state will start up according to programmed turn on delay. After all output are built up successfully, the device will then enter NORMAL state. If there is reset event during RECOVER state, the device will go to RCVRST state.

## RCVRST State

RCVRST state is extra reset state to assert RESETB pin, other rails will still start up in programmed sequence. This state aims to provide possible reset events including OV/UV and watchdog detection for those continuously enabled rails. The device will go back to RECOVER state automatically after once the holding time is expired and no reset event.

## VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplify the system design.

## High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks and one boost employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4/5.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180° phase-shifted clock.

The VOUT4 is a LV synchronous boost converter also power by VOUT1. It's regulated at 5V with up to 500mA continuous current.

The VOUT5 is a load switch output powered by VOUT1, the integrated MOSFET on-resistance is 100mΩ.

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG\_PGSEL1** and **CONFIG\_PGSEL2**.

## Deep Over Voltage Protection

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If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP\_OVP\_SEL[1:0]**.

## Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP\_UVP\_SEL[1:0]**.

## Thermal Shutdown

The thermal shutdown protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 155°C, the device will restart with internal soft start phase.

## Over Current Protection (OCP)

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When peak current point is kicked for continuous 32 times, the converter stops switching, the device will jump to DEEPSAFE state. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

For the boost, the device provides a load disconnect function, which completely disconnects the output from the input during overload. Then output short to ground fault is protected.

## Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61450S implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency within dedicated range and period triangular or pseudo modulation. Therefore, the SCT61450S can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

## Frequency Foldback

To avoid meeting minimum on time, the HV buck VOUT1 will reduce switching frequency actively when input voltage rising high. Other channel's frequency is unchanged.

When VIN greatly drops and minimum off time of HV buck VOUT1 is kicked, the VOUT1 enter dropout mode and also reduce its frequency to get max output.

## RESETB Indicator

The RESETB indicator will assert when reset event occurs. It will reset MCU if it fails to feed watchdog, MCU then can reloading program to ensure the program run well. The RESETB pin is an open-drain output and can be connected to various I/O level through pull-up resistor. The reset event mapping to RESETB pin can be configured through changing the register **RSTMAP**.

## Active Output Discharge

Once any output is shutoff due to deep safe events or disabled by I2C command, there is an active output discharge path will be turned on for each channel.

## VCC Regulator

The VCC supplied by VIN to provide power to the internal circuitry. A decoupling capacitor need to be placed between VCC and AGND. Note the VCC is not allowed to power external device due to limited current capability. The VCC voltage is continuously monitored, any over-voltage on it will force the device shutdown.

## Sleep Mode

The SCT61450S integrates an ultra power-saving mode with VOUT1 on. When in sleep mode, the disabled channels will shutoff and the alive channels will operate under PFM to further improve efficiency. Only after all disabled channels shutoff, pulling SLEEPB pin high can wake up the device and exit sleep mode. It can coordinate with MCU to achieve sleep mode system with extremely low consuming current from battery. If **LOWPOWER\_EN[0]=0**, the device will ignore the inputs from SLEEPB pin and never enter sleep mode.

There are two cases for the device to enter sleep mode: a) **LOWPOWER\_EN[0]=0** in OTP setting, the MCU must set bit **LOWPOWER\_EN[0]=1** in register **CONFIG\_ENLP** to enable sleep mode first, then pull SLEEPB pin low. When the device exit sleep mode, the bit **LOWPOWER\_EN[0]** will be reset automatically. b) **LOWPOWER\_EN[0]=1** in OTP setting, pull SLEEPB pin low will bring device to sleep mode directly. When the device exit sleep mode, the bit **LOWPOWER\_EN[0]** will also be reset automatically. Master must set bit **LOWPOWER\_EN[0]=1** to enter sleep mode again.

If bit **WD\_EN[0]=1** when entering sleep mode, watchdog window timer counts during sleep mode. The device will exit sleep mode once a WD failure occurs and enter RCVRST state. An appropriate window length setting can help the MCU be monitored by watchdog over the duration of sleep mode. Besides, watchdog expiration error can increase fault coverage even the MCU can't send watchdog response.

To avoid spike and noise on SLEEPB pin, the pin rising/falling deglitch time and blank time can be configured by register **CONFIG\_SLEEPB**.

## Watchdog

During NORMAL state, the watchdog can monitor the MCU with programmable cycle. Everytime the device enters NORMAL state and RESETB pin is released, the watchdog will be activated if WDDIS pin is low and bit **WD\_EN[0]=1b**. There will be extension cycles if **WD\_EN[0]=1b** when entering NORMAL state, which is used to wait MCU's program loading process and can be configured by bit **WD\_1UD[2:0]**. During the close window of first update extension, any WDI or **WD\_KEY** signals will be ignored and WD error counter keeps zero.

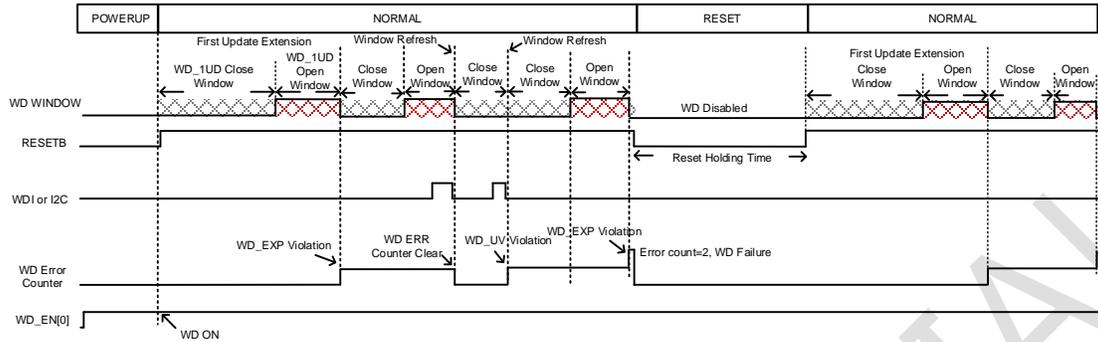
## Simple Watchdog

If **WD\_MODE[0] = 1**, the device will implement simple watchdog, the MCU should provide trigger pulse to WDI pin or write any byte to specific register **WD\_KEY** within the open window. The length of open window and closed window can be configured by I2C. A correct watchdog trigger will restart the whole window cycle immediately. Giving pulse or writing byte to register **WD\_KEY** during the closed window will result in **WD\_UV[0]** violation and will restart the whole window cycle immediately. If MCU doesn't send high pulse or write byte to **WD\_KEY** before the whole window is expired, **WD\_EXP[0]** violation occurs. Any violation will make the WD error counter plus one. When WD error counter reaches the **WD\_FAIL\_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

## QA Watchdog

If **WD\_MODE[0] = 0**, the device will implement Question and Answer (QA) watchdog and signals on WDI pin are ignored. In QA watchdog mode, MCU should read register **WD\_KEY** to get the answer through I2C. Then MCU response the watchdog in open window through writing the specific answer to register **WD\_KEY**. A correct watchdog trigger will refresh the whole window cycle immediately and the **WD\_KEY** register being updated. Writing the incorrect answer to the **WD\_KEY** will result in the value written being ignored and a **WD\_LFSR[0]** violation. Writing the correct response during a closed window will result in the write being ignored and a **WD\_UV[0]** violation. If MCU doesn't write byte to **WD\_KEY** and the whole window is expired, **WD\_EXP[0]** violation occurs. LFSR polynomial:  $x^8 + x^6 + x^5 + x^4 + 1$ . Any violation except **WD\_LFSR[0]** violation will make the WD error counter plus one. When WD error counter reaches the **WD\_FAIL\_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

Simple Mode With  
WD ON by Default



Simple Mode With  
WD OFF by Default

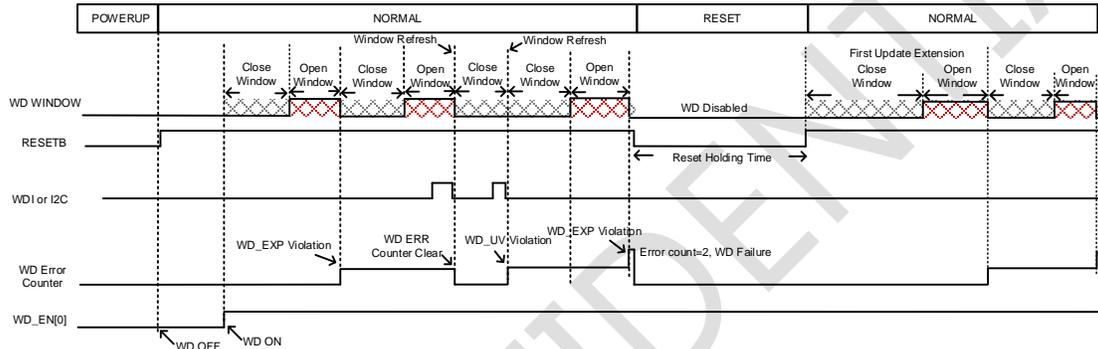
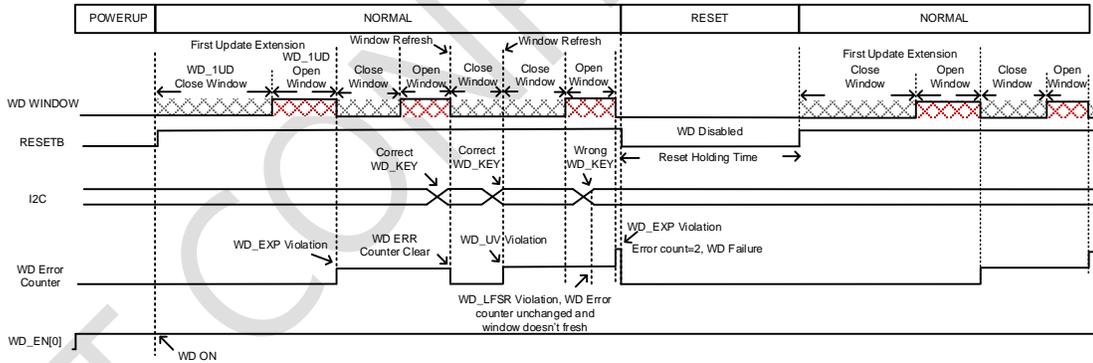


Figure 3a. Simple Watchdog Error Timing

QA Mode With  
WD ON by Default



QA Mode With  
WD OFF by Default

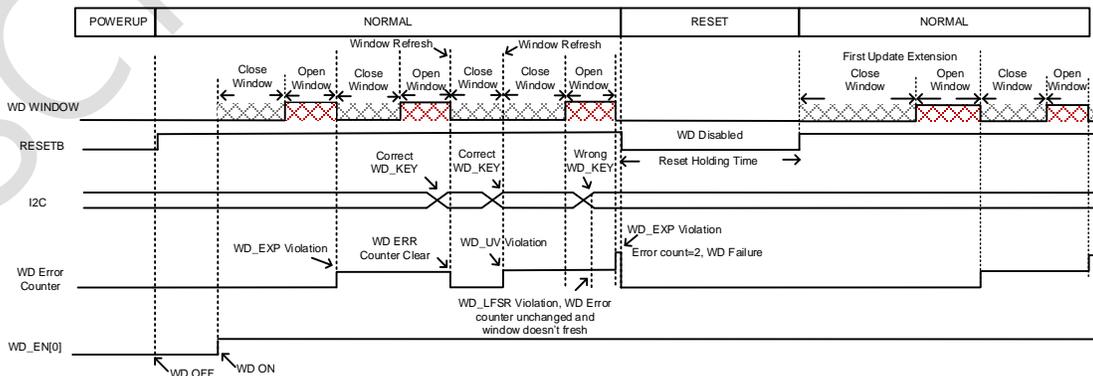


Figure 3b. QA Watchdog Error Timing

## I2C Interface

The SCT61450S integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61450S is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61450S supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

## Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

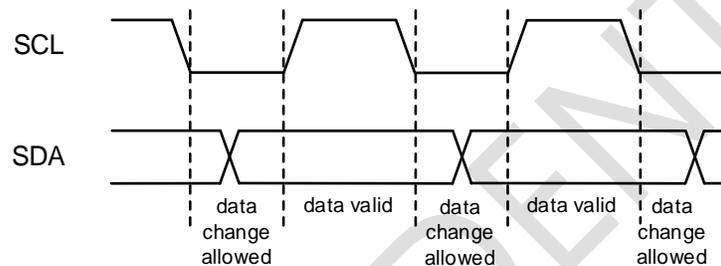


Figure 4. Data Validity Diagram

## START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

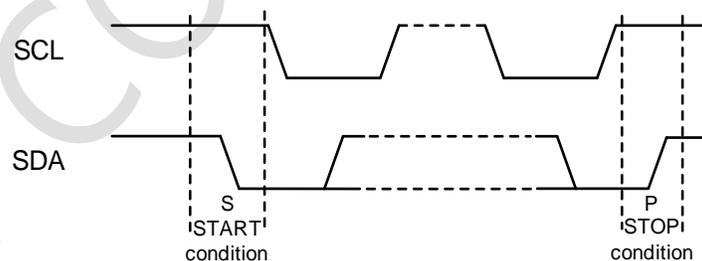


Figure 5. START and STOP Conditions Diagram

## Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61450S will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to

# SCT61450S

indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

## Packet Error Checking (PEC)

The SCT61450S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of  $x^8 + x^2 + x + 1$ . The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated over the entire message from the first START condition. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC\_EN** in register **CONFIG\_FSS**.

## Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

## Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 6 illustrates the proper format for one frame.

Write Byte



Write Byte with PEC



Read Byte



Read Byte with PEC

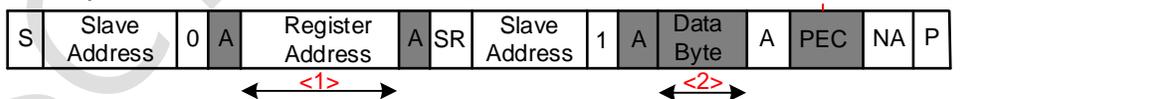


Figure 6. Transmission Data Format Diagram

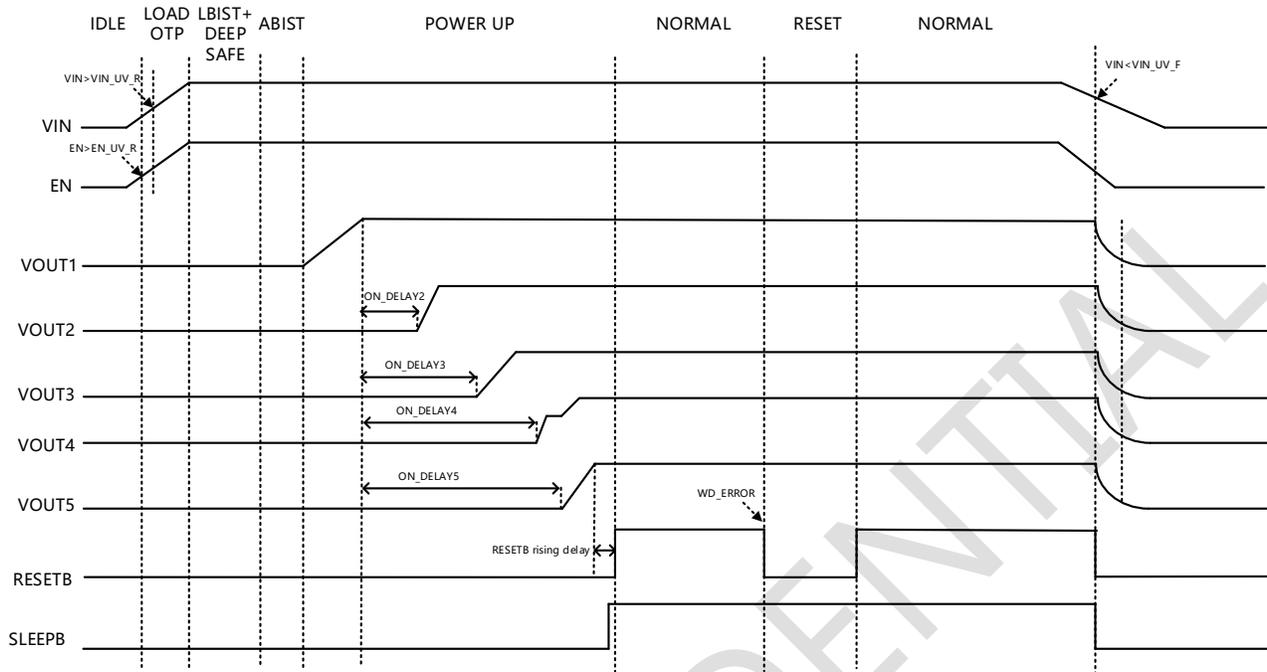


Figure 7. Power on Sequence

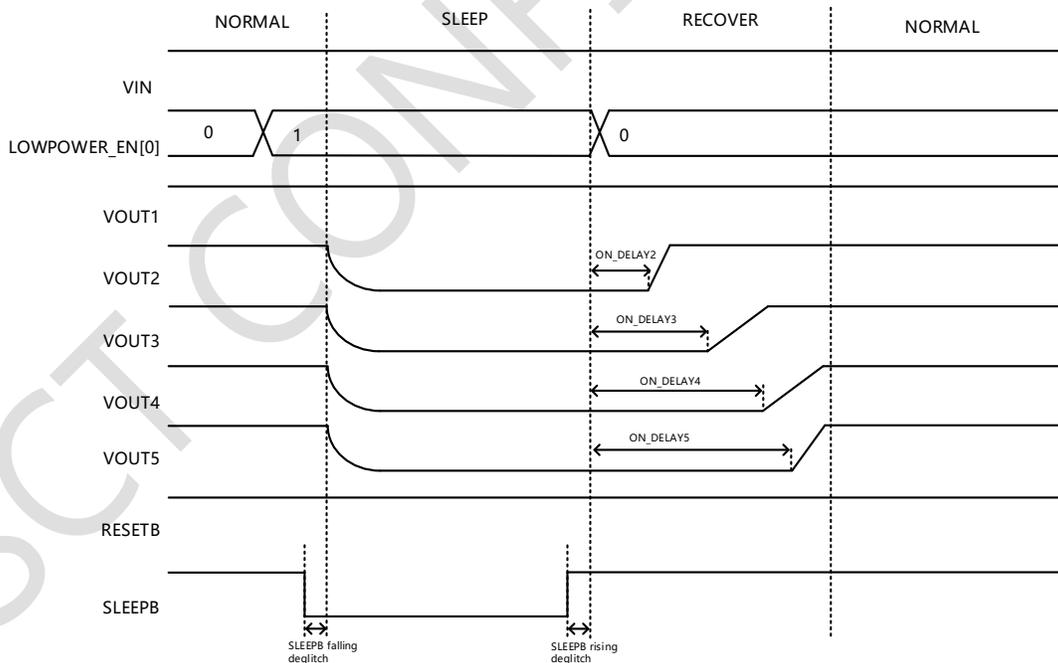


Figure 8. Sleep Mode Entry and Exit Diagram

## APPLICATION INFORMATION

### Typical Application

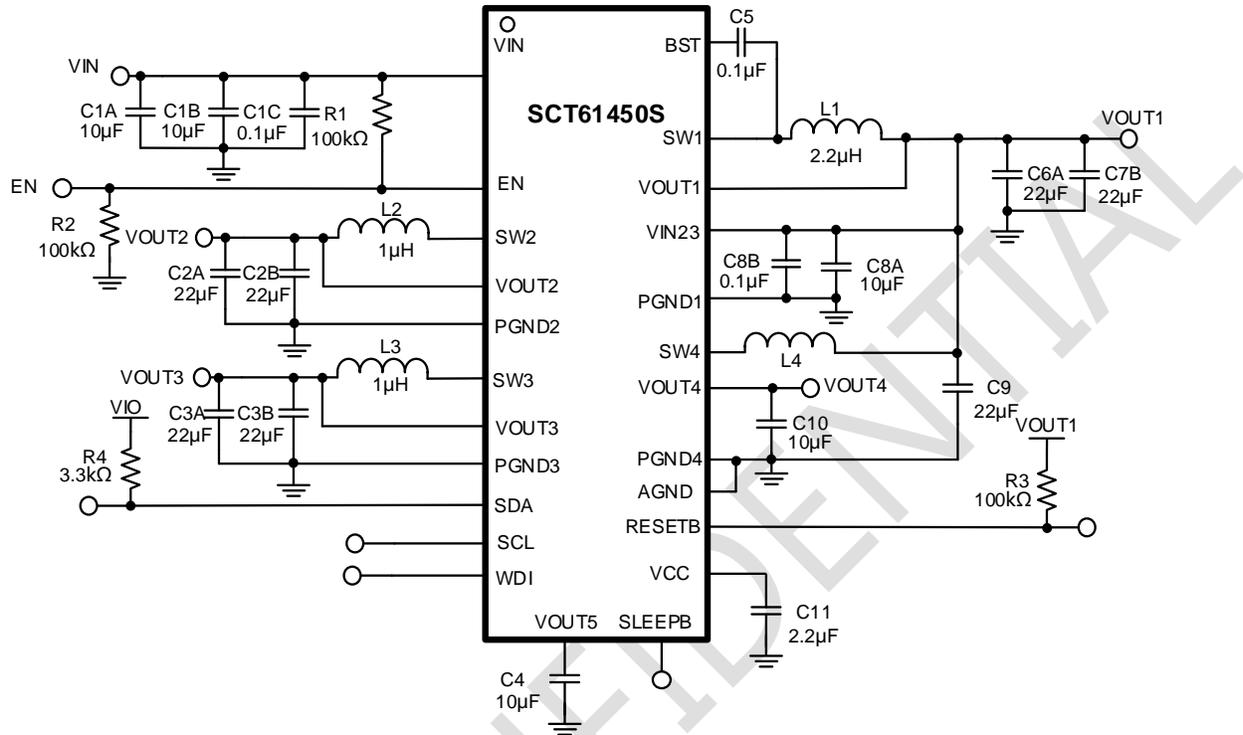


Figure 9. Application Schematic, 3.5V to 36V, PMIC Regulator at 2.2MHz

#### Design Parameters

| Design Parameters                    | Example Value  |
|--------------------------------------|--|
| Input Voltage                        | 12V Normal 3.5V to 36V   |
| Output Voltage                       | VOUT1: 3.3V<br>VOUT2: 1.1V<br>VOUT3: 1.5V<br>VOUT4: 5V<br>VOUT5: 3.3V          |
| Maximum Output Current               | VOUT1: 3A (in total)<br>VOUT2: 2A<br>VOUT3: 2A<br>VOUT4: 500mA<br>VOUT5: 800mA |
| Switching Frequency                  | 2.2MHz   |
| Output Voltage Ripple (peak to peak) | VOUT1: 10mV<br>VOUT2: 5mV<br>VOUT3: 5mV<br>VOUT4: 20mV<br>VOUT5: 2mV           |

### Under Voltage Lock-Out

An external voltage divider network of  $R_1$  from the input to EN pin and  $R_2$  from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of  $R_1$  and  $R_2$  resistors.

$$V_{rise} = \left(1 + \frac{R_1}{R_2}\right) * V_{ENrise} \quad (1)$$

$$V_{fall} = \left(1 + \frac{R_1}{R_2}\right) * V_{ENfall} \quad (2)$$

where

- $V_{rise}$  is rising threshold of Vin UVLO
- $V_{fall}$  is falling threshold of Vin UVLO
- $V_{ENrise}$  is rising threshold of EN UVLO
- $V_{ENfall}$  is falling threshold of EN UVLO

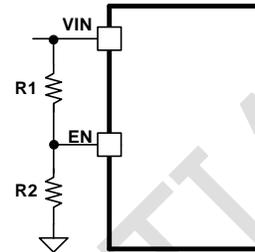


Figure 10. System UVLO by enable divide

### Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

For a buck converter, the peak-to-peak ripple current in the inductor  $I_{LPP}$  can be calculated as in Equation 3.

$$I_{LPP\_BUCK} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (3)$$

Where

- $I_{LPP\_BUCK}$  is the inductor peak-to-peak current of buck
- $L$  is the inductance of inductor
- $f_{SW}$  is the switching frequency
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * \left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) \quad (4)$$

Where

- $L_{MIN}$  is the minimum inductance required
- $V_{IN(max)}$  is the maximum input voltage
- $I_{OUT(max)}$  is the maximum DC load current

- LIR is coefficient of  $I_{LPP}$  to  $I_{OUT}$

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor,  $I_{LPEAK}$  and  $I_{LRMS}$  can be calculated as in equation 5 and equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (6)$$

Where

- $I_{LPEAK}$  is the inductor peak current
- $I_{OUT}$  is the DC load current
- $I_{LPP}$  is the inductor peak-to-peak current
- $I_{LRMS}$  is the inductor RMS current

For a boost converter, the peak-to-peak ripple current in the inductor  $I_{LPP}$  can be calculated as

$$I_{LPP\_BOOST} = \frac{1}{L \times \left( \frac{1}{V_{OUT}-V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (7)$$

Where

- $I_{LPP\_BOOST}$  is the inductor peak-to-peak current of boost
- $L$  is the inductance of inductor
- $f_{SW}$  is the switching frequency
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage

Calculate the inductor DC current as in equation 8

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (8)$$

Therefore, the peak switching current of inductor,  $I_{LPEAK}$ , is calculated as

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \quad (9)$$

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device. The most conservative approach is to choose an inductor with a saturation current rating greater than peak current limit. Because of the maximum  $I_{LPEAK}$  limited by device, the maximum output current that the device can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

## Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to  $V_{IN}$  and GND pins as possible.

For buck converter, the voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation10.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst case condition occurs at  $V_{IN}=2*V_{OUT}$ , where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For the boost converter power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 10 $\mu$ F input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

### Bootstrap Capacitor Selection

A 0.1 $\mu$ F ceramic capacitor must be connected between BST pin and SW1 pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

### Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 13 desired.

$$\Delta V_{OUT\_BUCK} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (13)$$

Where

- $\Delta V_{OUT\_BUCK}$  is the output voltage ripple of buck converter
- $f_{SW}$  is the switching frequency
- L is the inductance of inductor
- $C_{OUT}$  is the output capacitance
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10 $\mu$ F ceramic output capacitors work for most applications.

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For boost converter, typically, a 10µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. From the required output voltage ripple, use the below equation to calculate the minimum required effective capacitance

$$\Delta V_{OUT\_BOOST} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (14)$$

where

- $\Delta V_{OUT\_BOOST}$  is output voltage ripple caused by charging and discharging of the output capacitor of boost
- $V_{IN\_MIN}$  is the minimum input voltage of boost converter.
- $V_{OUT}$  is the output voltage.
- $I_{OUT}$  is the output current.
- $f_{SW}$  is the converter switching frequency.

**Table 3. Recommended BOM for Typical Application**

| Output Rail | Frequency (MHz) | L (uH) | Input Capacitor (uF) | Output Capacitor (uF) |
|-------------|-----------------|--------|----------------------|-----------------------|
| Buck1       | 2.2             | 2.2    | 2 x 10+1 x 0.1       | 2 x 22                |
| Buck2       | 2.2             | 1      | 10+1 x 0.1           | 2 x 22                |
| Buck3       | 2.2             | 1      |                      | 2 x 22                |
| Boost4      | 2.2             | 1      | 22                   | 10                    |
| Loadswitch5 | -               | -      | -                    | 10                    |
| VCC         | -               | -      | -                    | 2.2                   |

## Application Waveforms

$V_{in}=12V$ ,  $V_{OUT1}=3.3V$ ,  $V_{OUT2}=1.1V$ ,  $V_{OUT3}=1.5V$ ,  $V_{OUT4}=5V$ ,  $V_{OUT5}=3.3V$ , unless otherwise noted

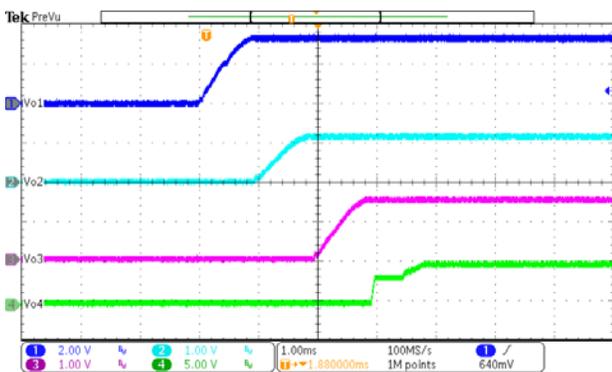


Figure 11. Power On ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

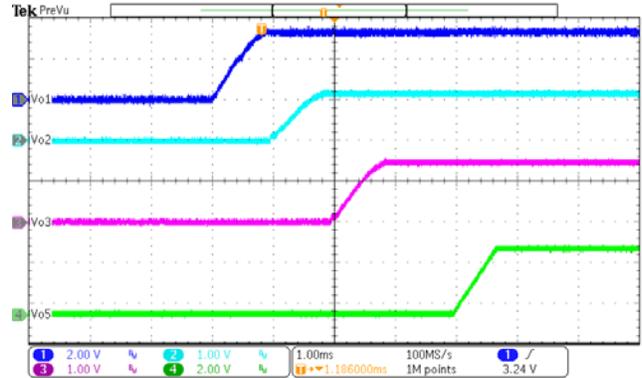


Figure 12. Power On ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

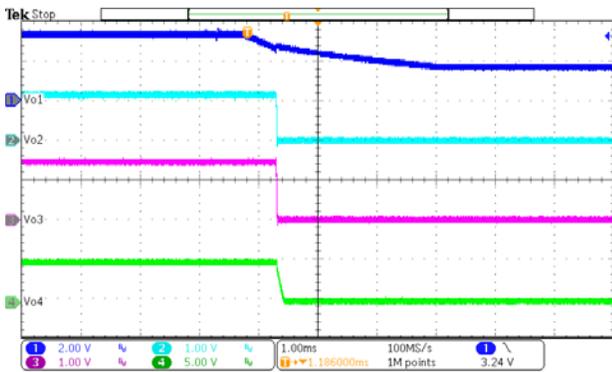


Figure 13. Power Off ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

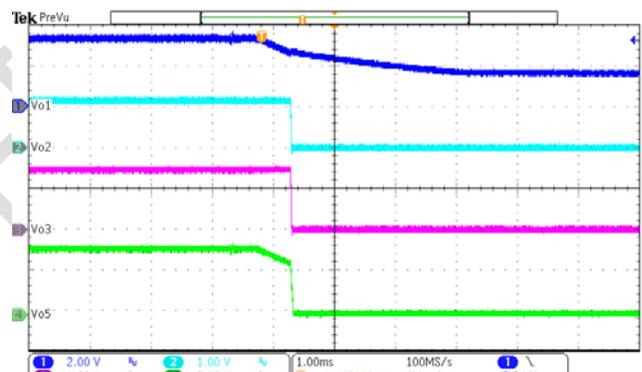


Figure 14. Power Off ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

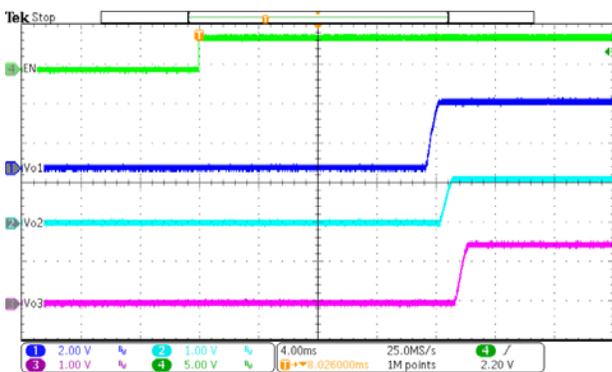


Figure 15. EN On ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

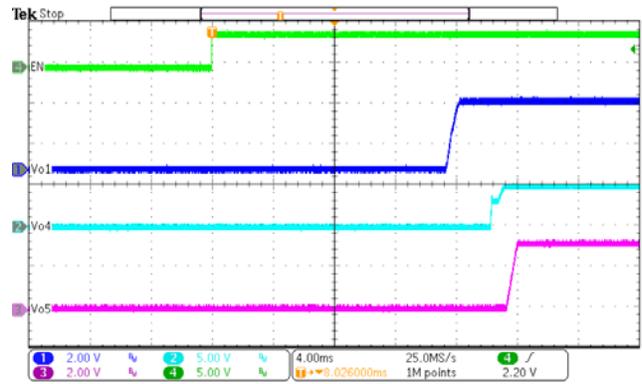


Figure 16. EN On ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

# SCT61450S

## Application Waveforms (continued)

$V_{in}=12V$ ,  $V_{OUT1}=3.3V$ ,  $V_{OUT2}=1.15V$ ,  $V_{OUT3}=1.5V$ ,  $V_{OUT4}=5V$ ,  $V_{OUT5}=3.3V$ , unless otherwise noted

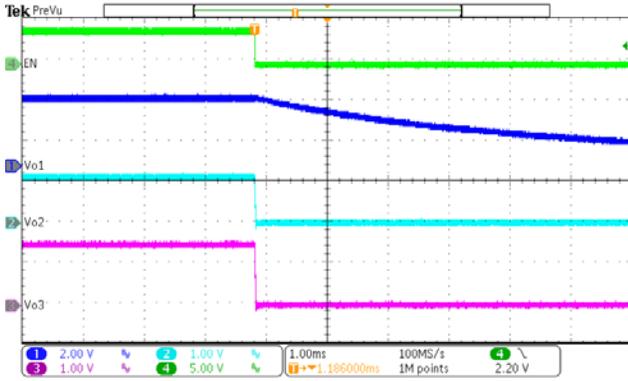


Figure 17. EN Off ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

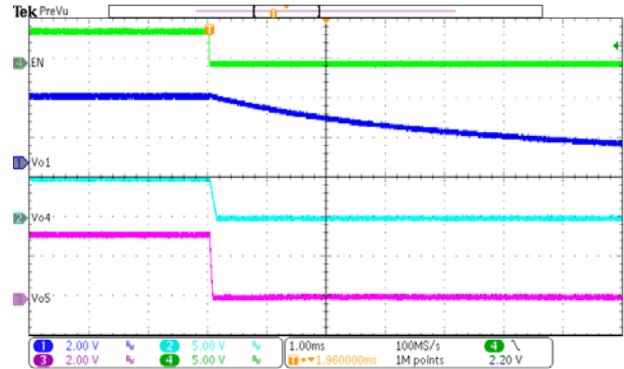


Figure 18. EN Off ( $I_{o2}=I_{o3}=2A$ ,  $I_{o4}=0.5A$ ,  $I_{o5}=0.8A$ )

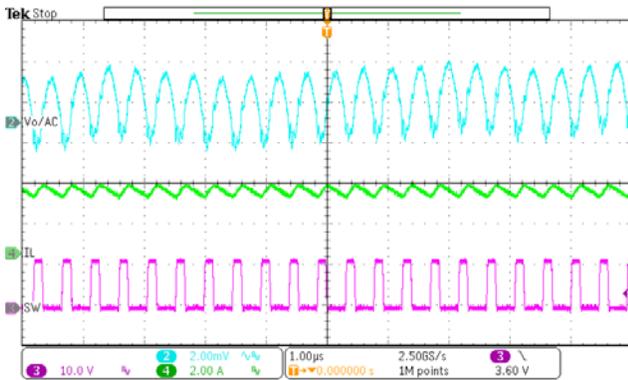


Figure 19. Buck1 Steady State ( $I_{o1} = 3A$ )

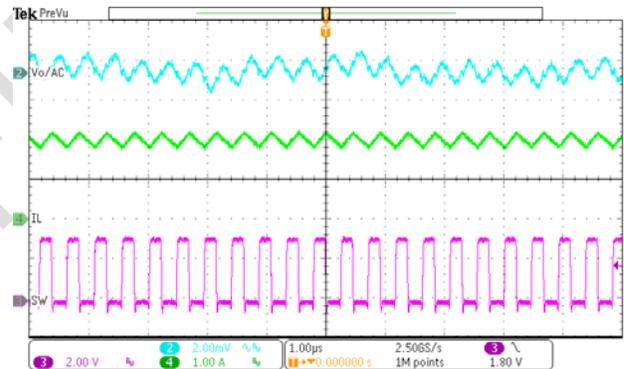


Figure 20. Buck2 Steady State ( $I_{o2} = 2A$ )

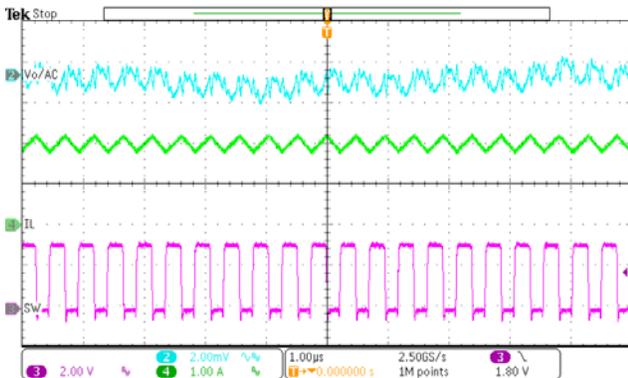


Figure 21. Buck3 Steady State ( $I_{o3} = 2A$ )

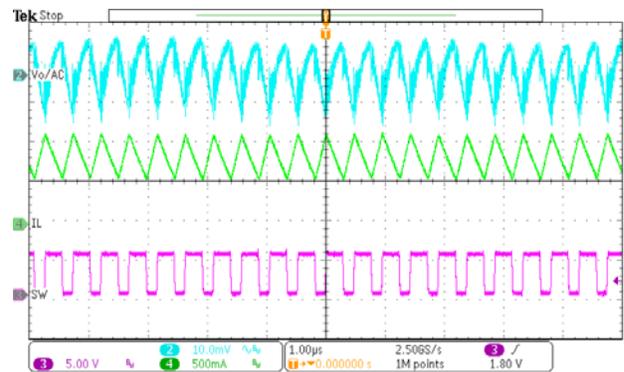


Figure 22. Boost4 Steady State ( $I_{o4} = 500mA$ )

**Application Waveforms (continued)**

$V_{in}=12V$ ,  $V_{OUT1}=3.3V$ ,  $V_{OUT2}=1.15V$ ,  $V_{OUT3}=1.5V$ ,  $V_{OUT4}=5V$ ,  $V_{OUT5}=3.3V$ , unless otherwise noted

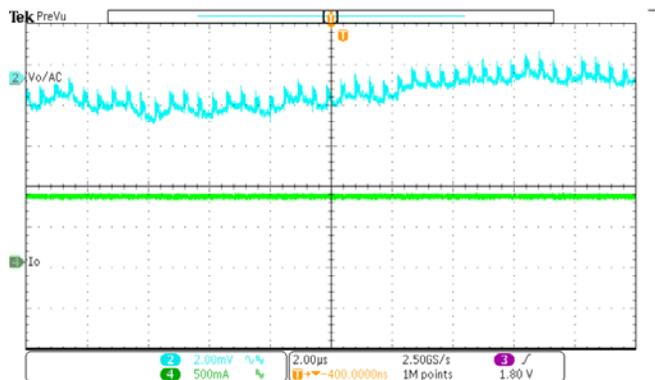


Figure 23. Loadswitch Steady State ( $I_{o5} = 800mA$ )

## Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impedance.
3. Place a low ESR ceramic capacitor as close to VIN1 and VIN23 pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

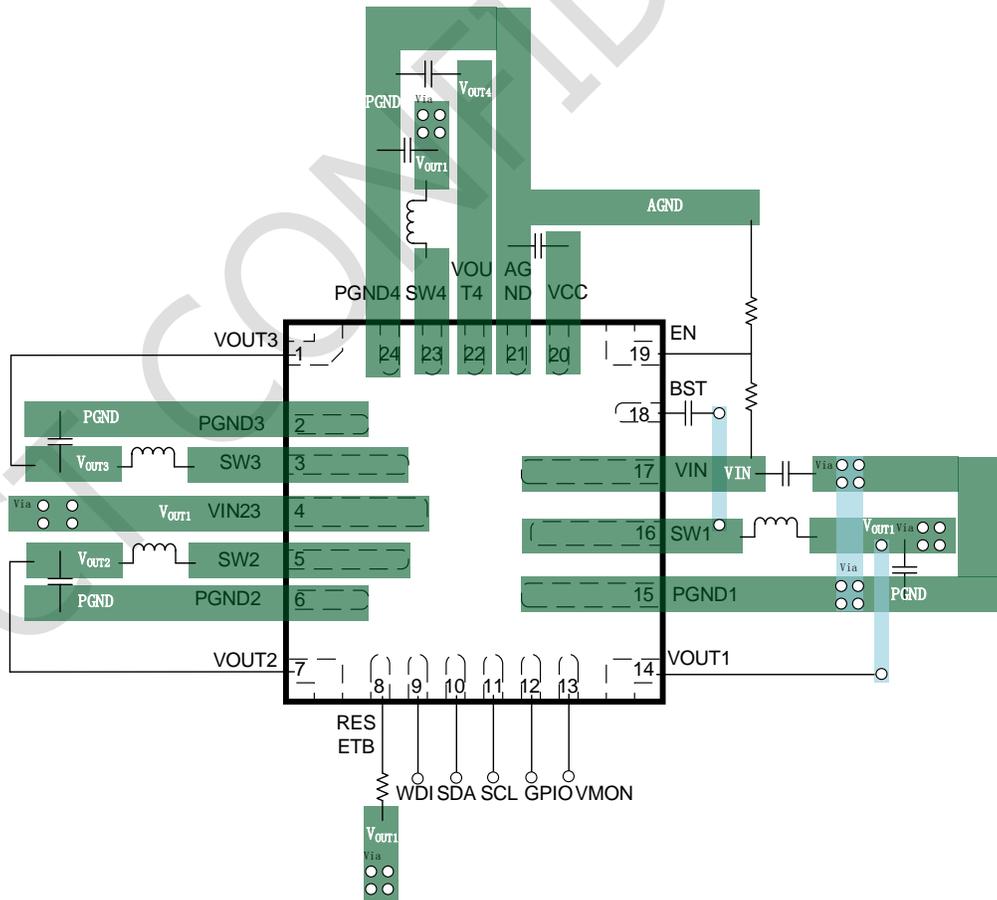


Figure 24. PCB Layout Example

## Register Map

| ADDRESS | REGISTER      | DEFAULT VALUE | OTP ACCESS | I2C LOCK | WD LOCK |
|---------|---------------|---------------|------------|----------|---------|
| 0x00    | CHIPID        | -             | Y          | N        | N       |
| 0x01    | CONFIG_FSS    | 70h           | Y          | Y        | N       |
| 0x02    | CONFIG_T1     | 00h           | Y          | Y        | N       |
| 0x03    | CONFIG_T2     | 1Fh           | Y          | Y        | N       |
| 0x05    | CONFIG_EN     | 3Dh           | Y          | Y        | N       |
| 0x06    | CONFIG_PU1    | 00h           | Y          | Y        | N       |
| 0x07    | CONFIG_PU2    | 11h           | Y          | Y        | N       |
| 0x08    | RSTMAP        | 3Fh           | Y          | Y        | N       |
| 0x0A    | STATUV        | 00h           | N          | N        | N       |
| 0x0B    | STATOV        | 00h           | N          | N        | N       |
| 0x0C    | STATOFF       | 00h           | N          | N        | N       |
| 0x0D    | STATD         | 00h           | N          | N        | N       |
| 0x0E    | STATWD        | 00h           | N          | N        | N       |
| 0x0F    | VOUT2         | 06h           | Y          | Y        | N       |
| 0x10    | VOUT3         | 0Eh           | Y          | Y        | N       |
| 0x11    | CONFIG_MISC   | 00h           | Y          | Y        | N       |
| 0x12    | CONFIG_PFM    | 00h           | Y          | Y        | N       |
| 0x13    | CONFIG_WD1    | 87h           | Y          | N        | Y       |
| 0x14    | CONFIG_WD2    | 0Eh           | Y          | N        | Y       |
| 0x15    | CONFIG_WD3    | 13h           | Y          | N        | Y       |
| 0x16    | WD_KEY        | AAh           | Y          | N        | N       |
| 0x17    | WD_LOCK       | 00h           | N          | N        | N       |
| 0x18    | CONFIG_ENLP   | 2Ch           | Y          | Y        | N       |
| 0x19    | CONFIG_PGSEL1 | 01h           | Y          | Y        | N       |
| 0x1A    | CONFIG_PGSEL2 | 55h           | Y          | Y        | N       |
| 0x1B    | CONFIG_SLEEPB | 30h           | Y          | Y        | N       |
| 0x1C    | I2C_LOCK      | 01h           | N          | N        | N       |
| 0x22    | SYS_STATE     | 00h           | N          | N        | N       |

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| CHIPID [7:0]  |           |      |   |                              |
|---------------|-----------|------|---|------------------------------|
| ADDRESS: 0x00 |           |      |   |                              |
| BITS          | FIELD     | TYPE | DESCRIPTION   | DECODE                       |
| [7:6]         | RESERVED  | R    | /   | Reserved, always read as 01b |
| [5:0]         | CONFIG_ID | W/R  | Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers. | See Ordering Information     |

| CONFIG_FSS [7:0] |               |      |   |   |
|------------------|---------------|------|---|---|
| ADDRESS: 0x01    |               |      |   |   |
| BITS             | FIELD         | TYPE | DESCRIPTION   | DECODE  |
| [7]              | EN_HOLD       | W/R  | Enable Hold. Overrides the EN pin to keep the device enabled. This bit is cleared when RESETB is asserted.  | 0 = EN pin controls power down<br>1 = Device enabled. Ignores EN pin state  |
| [6]              | FSS_EN        | W/R  | Frequency Spread Spectrum Enable.   | 0 = Disabled<br>1 = Enabled   |
| [5]              | FSS_MODE      | W/R  | Frequency Spread Spectrum Mode.   | 0 = Pseudorandom Modulation<br>1 = Triangle Modulation                      |
| [4]              | FSS_PERIOD    | W/R  | Frequency Spread Period.  | 0 = 4.5KHz<br>1 = 10KHz   |
| [3:2]            | FSS_RANGE     | W/R  | Frequency Spread Spectrum Range.  | 00 = $\pm 5\%$ ; 01 = $\pm 2.5\%$ ; 10 = $\pm 7.5\%$ ;<br>11 = $\pm 3.75\%$ |
| [1]              | PMIC_RESET_EN | W/R  | Enable PMIC reset Function. After this bit is set to 1, writing EN_ALL[0]=0 will shut down all power channels, reset all registers and restart automatically. | 0 = Disabled<br>1 = Enabled   |
| [0]              | PEC_EN        | W/R  | Packet Error Checking Enable. Set this bit to a 1 to enable PEC or 0 to disable PEC.  | 0 = Disabled<br>1 = Enabled   |

| CONFIG_T1 [7:0] |             |      |   |   |
|-----------------|-------------|------|---|---|
| ADDRESS: 0x02   |             |      |   |   |
| BITS            | FIELD       | TYPE | DESCRIPTION   | DECODE  |
| [7:6]           | RESETB_HT   | W/R  | RESETB Hold Time Selection. This is the amount of time that the RESET pin is active (low) after the event that caused the RESET pin to activate is removed. | 00 = 10ms; 01 = 20ms; 10 = 30ms; 11 = 40ms  |
| [5:4]           | RESETB_DLYR | W/R  | RESETB Rising delay when state change from POWERUP to NORMAL  | 00 = 2.5ms; 01 = 5ms; 10 = 7.5ms; 11 = 10ms   |
| [3:2]           | RESERVED    | R    | /   | /   |
| [1:0]           | DELAY_SCALE | W/R  | Power up and Recover On Delay Scale.  | 00: Scale=0.5ms. Delay ranges from 0~7.5ms<br>01: Scale =1ms. Delay ranges from 0-15ms<br>10: Scale=2.5ms. Delay ranges from 0-37.5ms |

|  |  |  |  |  |
|--|--|--|--|--|
|  |  |  |  | 11: Scale =5ms. Delay ranges from 0-75ms |
|--|--|--|--|--|

| CONFIG_T2 [7:0] |          |      |   |   |
|-----------------|----------|------|---|---|
| ADDRESS: 0x03   |          |      |   |   |
| BITS            | FIELD    | TYPE | DESCRIPTION   | DECODE  |
| [7:6]           | RESERVED | R    | /   | /   |
| [5]             | DF_SCALE | W/R  | OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators. | Analog Filter Time = 10us.<br>Added Digital Filter Time:<br>=DF[4:0] x 2μs, when DF_SCALE=0,<br>=DF[4:0] x 10μs, when DF_SCALE=1. |
| [4:0]           | DF       | W/R  |   |   |

| CONFIG_EN [7:0] |          |      |  |   |
|-----------------|----------|------|--|---|
| ADDRESS: 0x05   |          |      |  |   |
| BITS            | FIELD    | TYPE | DESCRIPTION  | DECODE                                    |
| [7:6]           | RESERVED | R    | /  | /   |
| [5]             | EN5      | W/R  | Enable for Load Switch OUT5. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state. | 0 = Output Disabled<br>1 = Output Enabled |
| [4]             | EN4      | W/R  | Enable for LV BOOST OUT4. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.    | 0 = Output Disabled<br>1 = Output Enabled |
| [3]             | EN3      | W/R  | Enable for LV BUCK OUT3. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.     | 0 = Output Disabled<br>1 = Output Enabled |
| [2]             | EN2      | W/R  | Enable for LV BUCK OUT2. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.     | 0 = Output Disabled<br>1 = Output Enabled |
| [1]             | RESERVED | R    | /  | /   |
| [0]             | EN_ALL   | W/R  | Enable for all channel   | 0 = Output Disabled<br>1 = Output Enabled |

| CONFIG_PU1 [7:0] |           |      |  |  |
|------------------|-----------|------|--|--|
| ADDRESS: 0x06    |           |      |  |  |
| BITS             | FIELD     | TYPE | DESCRIPTION                              | DECODE   |
| [7:4]            | ON_DELAY5 | W/R  | OUT5 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, tON_DELAY5 = ON_DELAY5[3:0] x 0.5ms<br>when DELAY_SCALE=01, tON_DELAY5 = ON_DELAY5[3:0] x 1ms<br>when DELAY_SCALE=10, tON_DELAY5 = ON_DELAY5[3:0] x 2.5ms<br>when DELAY_SCALE=11, tON_DELAY5 = ON_DELAY5[3:0] x 5ms |
| [3:0]            | ON_DELAY4 | W/R  | OUT4 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, tON_DELAY4 = ON_DELAY4[3:0] x 0.5ms<br>when DELAY_SCALE=01, tON_DELAY4 = ON_DELAY4[3:0] x 1ms<br>when DELAY_SCALE=10, tON_DELAY4 = ON_DELAY4[3:0] x 2.5ms<br>when DELAY_SCALE=11, tON_DELAY4 = ON_DELAY4[3:0] x 5ms |

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| CONFIG_PU2 [7:0] |           |      |  |  |
|------------------|-----------|------|--|--|
| ADDRESS: 0x07    |           |      |  |  |
| BITS             | FIELD     | TYPE | DESCRIPTION                              | DECODE   |
| [7:4]            | ON_DELAY3 | W/R  | OUT3 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, tON_DELAY3 = ON_DELAY3[3:0] x 0.5ms<br>when DELAY_SCALE=01, tON_DELAY3 = ON_DELAY3[3:0] x 1ms<br>when DELAY_SCALE=10, tON_DELAY3 = ON_DELAY3[3:0] x 2.5ms<br>when DELAY_SCALE=11, tON_DELAY3 = ON_DELAY3[3:0] x 5ms |
| [3:0]            | ON_DELAY2 | W/R  | OUT2 Power-Up and Recover Turn On delay. | when DELAY_SCALE=00, tON_DELAY2 = ON_DELAY2[3:0] x 0.5ms<br>when DELAY_SCALE=01, tON_DELAY2 = ON_DELAY2[3:0] x 1ms<br>when DELAY_SCALE=10, tON_DELAY2 = ON_DELAY2[3:0] x 2.5ms<br>when DELAY_SCALE=11, tON_DELAY2 = ON_DELAY2[3:0] x 5ms |

| RSTMAP [7:0]  |            |      |                                 |  |
|---------------|------------|------|---------------------------------|--|
| ADDRESS: 0x08 |            |      |                                 |  |
| BITS          | FIELD      | TYPE | DESCRIPTION                     | DECODE   |
| [7:6]         | RESERVED   | R    | /                               | /  |
| [5]           | RSTMAP_VO5 | W/R  | RESETB Pin Mapping for OUT5.    | 0 = OV[5] and UV[5] not mapped to RESETB pin<br>1 = OV[5] and UV[5] are mapped to RESETB pin |
| [4]           | RSTMAP_VO4 | W/R  | RESETB Pin Mapping for OUT4.    | 0 = OV[4] and UV[4] not mapped to RESETB pin<br>1 = OV[4] and UV[4] are mapped to RESETB pin |
| [3]           | RSTMAP_VO3 | W/R  | RESETB Pin Mapping for OUT3.    | 0 = OV[3] and UV[3] not mapped to RESETB pin<br>1 = OV[3] and UV[3] are mapped to RESETB pin |
| [2]           | RSTMAP_VO2 | W/R  | RESETB Pin Mapping for OUT2.    | 0 = OV[2] and UV[2] not mapped to RESETB pin<br>1 = OV[2] and UV[2] are mapped to RESETB pin |
| [1]           | RSTMAP_VO1 | W/R  | RESETB Pin Mapping for OUT1.    | 0 = OV[1] and UV[1] not mapped to RESETB pin<br>1 = OV[1] and UV[1] are mapped to RESETB pin |
| [0]           | RSTMAP_WD  | W/R  | RESETB Pin Mapping for WD ERROR | 0 = WD ERROR is not mapped to RESETB pin<br>1 = WD ERROR is mapped to RESETB pin             |

| STATUV [7:0]  |          |               |  |  |
|---------------|----------|---------------|--|--|
| ADDRESS: 0x0A |          |               |  |  |
| BITS          | FIELD    | TYPE          | DESCRIPTION  | DECODE   |
| [7]           | UV       | Read<br>Clear | UV Comparator Status for all channels with Digital Filter. | 0 = All enabled channels are above UV threshold after DF<br>1 = Any enabled channel is below UV threshold after DF |
| [6]           | RESERVED | R             | /  | /  |
| [5]           | UV_WAR5  | Read<br>Clear | UV warning for OUT5, Digital Filter is not included        | 0 = OUT5 is above UV threshold before DF<br>1 = OUT5 is below UV threshold before DF                               |
| [4]           | UV_WAR4  | Read<br>Clear | UV warning for OUT4, Digital Filter is not included        | 0 = OUT4 is above UV threshold before DF<br>1 = OUT4 is below UV threshold before DF                               |
| [3]           | UV_WAR3  | Read<br>Clear | UV warning for OUT3, Digital Filter is not included        | 0 = OUT3 is above UV threshold before DF<br>1 = OUT3 is below UV threshold before DF                               |
| [2]           | UV_WAR2  | Read<br>Clear | UV warning for OUT2, Digital Filter is not included        | 0 = OUT2 is above UV threshold before DF<br>1 = OUT2 is below UV threshold before DF                               |
| [1]           | UV_WAR1  | Read<br>Clear | UV warning for OUT1, Digital Filter is not included        | 0 = OUT1 is above UV threshold before DF<br>1 = OUT1 is below UV threshold before DF                               |
| [0]           | RESERVED | R             | /  | /  |

| STATOV [7:0]  |          |               |  |  |
|---------------|----------|---------------|--|--|
| ADDRESS: 0x0B |          |               |  |  |
| BITS          | FIELD    | TYPE          | DESCRIPTION  | DECODE   |
| [7]           | OV       | Read<br>Clear | OV Comparator Status for all channels with Digital Filter. | 0 = All enabled channels are below OV threshold after DF<br>1 = Any enabled channel is above OV threshold after DF |
| [6]           | RESERVED | R             | /  | /  |
| [5]           | OV_WAR5  | Read<br>Clear | OV warning for OUT5, Digital Filter is not included        | 0 = OUT5 is below OV threshold before DF<br>1 = OUT5 is above OV threshold before DF                               |
| [4]           | OV_WAR4  | Read<br>Clear | OV warning for OUT4, Digital Filter is not included        | 0 = OUT4 is below OV threshold before DF<br>1 = OUT4 is above OV threshold before DF                               |
| [3]           | OV_WAR3  | Read<br>Clear | OV warning for OUT3, Digital Filter is not included        | 0 = OUT3 is below OV threshold before DF<br>1 = OUT3 is above OV threshold before DF                               |

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|     |          |               |   |  |
|-----|----------|---------------|---|--|
| [2] | OV_WAR2  | Read<br>Clear | OV warning for OUT2, Digital Filter is not included | 0 = OUT2 is below OV threshold before DF<br>1 = OUT2 is above OV threshold before DF |
| [1] | OV_WAR1  | Read<br>Clear | OV warning for OUT1, Digital Filter is not included | 0 = OUT1 is below OV threshold before DF<br>1 = OUT1 is above OV threshold before DF |
| [0] | RESERVED | R             | /   | /  |

## STATOFF [7:0]

ADDRESS: 0x0C

| BITS  | FIELD    | TYPE          | DESCRIPTION                    | DECODE   |
|-------|----------|---------------|--------------------------------|--|
| [7:6] | RESERVED | R             | /                              | /  |
| [5]   | OFF5     | Read<br>Clear | OFF Comparator Status for OUT5 | 0 = OUT5 is above OFF threshold<br>1 = OUT5 is below OFF threshold |
| [4]   | OFF4     | Read<br>Clear | OFF Comparator Status for OUT4 | 0 = OUT4 is above OFF threshold<br>1 = OUT4 is below OFF threshold |
| [3]   | OFF3     | Read<br>Clear | OFF Comparator Status for OUT3 | 0 = OUT3 is above OFF threshold<br>1 = OUT3 is below OFF threshold |
| [2]   | OFF2     | Read<br>Clear | OFF Comparator Status for OUT2 | 0 = OUT2 is above OFF threshold<br>1 = OUT2 is below OFF threshold |
| [1]   | OFF1     | Read<br>Clear | OFF Comparator Status for OUT1 | 0 = OUT1 is above OFF threshold<br>1 = OUT1 is below OFF threshold |
| [0]   | RESERVED | R             | /                              | /  |

## STATD [7:0]

ADDRESS: 0x0D

| BITS | FIELD          | TYPE          | DESCRIPTION  | DECODE   |
|------|----------------|---------------|--|--|
| [7]  | RESERVED       | R             | /  | /  |
| [6]  | CLK_ERR        | Read<br>Clear | CLK fault indicator  | 0 = No fault detected<br>1 = CLK error detected  |
| [5]  | SUP_ERR        | Read<br>Clear | Supply fault indicator, include VCC OV fault and VIN OV fault              | 0 = No fault detected<br>1 = VCC OV or VIN OV detected   |
| [4]  | RST_ENTER      | Read<br>Clear | RESET state indicator  | 0 = No fault detected<br>1 = RESET state has entered since the last read.                                      |
| [3]  | DEEPSAFE_ENTER | Read<br>Clear | DEEPSAFE state indicator   | 0 = No fault detected<br>1 = DEEPSAFE state has entered since the last read.                                   |
| [2]  | PIN_ERR        | Read<br>Clear | Pin fault indicator, include RESETB Pin stuck fault and GND pin LOSS fault | 0 = No fault detected<br>1 = RESETB Short to supply detected or pull-down fail or GND LOSS since the last read |
| [1]  | THSD           | Read<br>Clear | Thermal Shutdown Indication  | 0 = No thermal shutdown<br>1 = Thermal shutdown has occurred since last read                                   |
| [0]  | INTERR         | Read<br>Clear | Internal Error, include OTP CRC failure and ABIST failure                  | 0 = No internal error detected<br>1 = Internal error detected  |

| STATWD [7:0]  |             |               |  |  |
|---------------|-------------|---------------|--|--|
| ADDRESS: 0x0E |             |               |  |  |
| BITS          | FIELD       | TYPE          | DESCRIPTION  | DECODE   |
| [7:6]         | RESERVED    | R             | /  | /  |
| [5]           | RESETB_STAT | R             | RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.            | 0 = RESETB is low<br>1 = RESETB is high                      |
| [4]           | WD_OPEN     | R             | Watchdog Open Window. This bit indicates that it is permissible to update the watchdog. This bit shows real-time status. | 0 = Watchdog update not open<br>1 = Watchdog ok to update    |
| [3]           | WD_ERR      | R             | Watchdog ERROR for 1 time or 2 times (config by WD_FAIL_CNT), LFSR mismatch is not included                              | 0 = No error detected<br>1 = Error detected                  |
| [2]           | WD_LFSR     | Read<br>Clear | LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.                                  | 0 = LFSR key match<br>1 = LFSR key mismatch since last read  |
| [1]           | WD_UV       | Read<br>Clear | Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.                              | 0 = No violation detected<br>1 = Watchdog updated too early  |
| [0]           | WD_EXP      | Read<br>Clear | Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.                   | 0 = Watchdog timer not expired<br>1 = Watchdog timer expired |

| VOUT2 [7:0]   |          |      |                      |  |
|---------------|----------|------|----------------------|--|
| ADDRESS: 0x0F |          |      |                      |  |
| BITS          | FIELD    | TYPE | DESCRIPTION          | DECODE   |
| [7:5]         | RESERVED | R    | /                    | /  |
| [4:0]         | OUT2     | W/R  | OUT2 Voltage Setting | $V_{OUT2} = OUT2[4:0] \times 50mV + 0.8V$<br>(0.8V to 2.35V) |

| VOUT3 [7:0]   |          |      |                      |  |
|---------------|----------|------|----------------------|--|
| ADDRESS: 0x10 |          |      |                      |  |
| BITS          | FIELD    | TYPE | DESCRIPTION          | DECODE   |
| [7:5]         | RESERVED | R    | /                    | /  |
| [4:0]         | OUT3     | W/R  | OUT3 Voltage Setting | $V_{OUT3} = OUT3[4:0] \times 50mV + 0.8V$<br>(0.8V to 2.35V) |

| CONFIG_MISC [7:0] |            |      |  |  |
|-------------------|------------|------|--|--|
| ADDRESS: 0x11     |            |      |  |  |
| BITS              | FIELD      | TYPE | DESCRIPTION  | DECODE                                     |
| [7:5]             | RESERVED   | R    | /  | /  |
| [4]               | VIN_OVP_EN | W/R  | Enable of VIN OVP. When VIN > 43V, part enter DEEPSAFE mode. | 0 = Disabled<br>1 = Enabled                |
| [3:2]             | VIN_START  | W/R  | VIN start threshold at VIN rising                            | 00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V       |
| [1:0]             | VIN_STOP   | W/R  | VIN stop threshold at VIN falling                            | 00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V |

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| CONFIG_PFM [7:0] |          |      |  |                     |
|------------------|----------|------|--|---------------------|
| ADDRESS: 0x12    |          |      |  |                     |
| BITS             | FIELD    | TYPE | DESCRIPTION                                      | DECODE              |
| [7:4]            | RESERVED | R    | /  | /                   |
| [3]              | PFM4     | W/R  | BOOST4 FCCM/PFM mode selection when NORMAL mode. | 0 = FCCM<br>1 = PFM |
| [2]              | PFM3     | W/R  | BUCK3 FCCM/PFM mode selection when NORMAL mode.  | 0 = FCCM<br>1 = PFM |
| [1]              | PFM2     | W/R  | BUCK2 FCCM/PFM mode selection when NORMAL mode.  | 0 = FCCM<br>1 = PFM |
| [0]              | PFM1     | W/R  | BUCK1 FCCM/PFM mode selection when NORMAL mode.  | 0 = FCCM<br>1 = PFM |

| CONFIG_WD1 [7:0] |          |      |                              |  |
|------------------|----------|------|------------------------------|--|
| ADDRESS: 0x13    |          |      |                              |  |
| BITS             | FIELD    | TYPE | DESCRIPTION                  | DECODE   |
| [7]              | WD_MODE  | W/R  | Watchdog Mode Selection      | 0 = QA watchdog enabled<br>1 = Simple watchdog enabled |
| [6]              | WD_SCALE | W/R  | Watchdog Clock Divider Scale | 0 = 128us<br>1 = 128us*64                              |
| [5:0]            | WD_CLK   | W/R  | Watchdog Clock Divider       | $t_{WDCLK} = (WD\_CLK[5:0]+1) \times WD\_SCALE$        |

| CONFIG_WD2 [7:0] |           |      |   |  |
|------------------|-----------|------|---|--|
| ADDRESS: 0x14    |           |      |   |  |
| BITS             | FIELD     | TYPE | DESCRIPTION   | DECODE   |
| [7:4]            | WD_TCLOSE | W/R  | Watchdog Close Window Duration Time. Sets the number of watchdog clock cycles before the open window starts.  | $t_{WD\_CLOSE} = t_{WDCLK} \times (WD\_TCLOSE [3:0]+1) \times 8$ |
| [3:0]            | WD_TOPEN  | W/R  | Watchdog Open Window Duration Time. Sets the number of watchdog clock cycles after the close window finishes. | $t_{WD\_OPEN} = t_{WDCLK} \times (WD\_TOPEN[3:0]+1) \times 8$    |

| CONFIG_WD3 [7:0] |             |      |  |                             |
|------------------|-------------|------|--|-----------------------------|
| ADDRESS: 0x15    |             |      |  |                             |
| BITS             | FIELD       | TYPE | DESCRIPTION  | DECODE                      |
| [7:5]            | RESERVED    | R    | /  | /                           |
| [4]              | WD_FAIL_CNT | W/R  | Watchdog Failure counter configuration. When Watchdog failure times reach the counter, report to RESETB and status register. | 0 = 1 time<br>1 = 2 times   |
| [3]              | WD_EN       | W/R  | Watchdog Enable  | 0 = Disabled<br>1 = Enabled |

|       |        |     |  |  |
|-------|--------|-----|--|--|
| [2:0] | WD_1UD | W/R | First Update Extension. Sets the number of extra watchdog window cycles after POR to the normal watchdog window. | $t1STWD\_CLOSE = tWD\_CLOSE \times (WD\_1UD [2:0] + 1)$<br>$t1STWD\_OPEN = tWD\_OPEN \times (WD\_1UD [2:0] + 1)$ |
|-------|--------|-----|--|--|

| WD_KEY [7:0]  |        |      |               |  |
|---------------|--------|------|---------------|--|
| ADDRESS: 0x16 |        |      |               |  |
| BITS          | FIELD  | TYPE | DESCRIPTION   | DECODE   |
| [7:0]         | WD_KEY | W/R  | Watchdog Key. | <p>The current key can be read from this register. To update the watchdog, the next value in the sequence must be written to this register. If configured as a simple windowed watchdog, writing any value to the WDKEY register will refresh the watchdog and the value written will be ignored.</p> <p>If configured as a QA watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in QA mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in QA mode during a closed window will result in the write being ignored and a WD_UV violation.</p> <p>LFSR polynomial: <math>x^8 + x^6 + x^5 + x^4 + 1</math></p> |

| WD_LOCK [7:0] |          |      |                          |  |
|---------------|----------|------|--------------------------|--|
| ADDRESS: 0x17 |          |      |                          |  |
| BITS          | FIELD    | TYPE | DESCRIPTION              | DECODE   |
| [7:1]         | RESERVED | R    | /                        | /  |
| [0]           | WDLOCK   | W/R  | Watchdog Lock Protection | 0 = Watchdog configuration registers are writeable<br>1 = Watchdog configuration registers are read-only |

| CONFIG_ENLP [7:0] |          |      |   |  |
|-------------------|----------|------|---|--|
| ADDRESS: 0x18     |          |      |   |  |
| BITS              | FIELD    | TYPE | DESCRIPTION   | DECODE   |
| [7:6]             | RESERVED | R    | /   | /  |
| [5]               | EN5_LP   | W/R  | Low power mode enable control for Load Switch OUT5. | 0 = Output enabled in low power mode<br>1 = Output disabled low power mode |
| [4]               | EN4_LP   | W/R  | Low power mode enable control for LV BOOST OUT4.    | 0 = Output enabled in low power mode<br>1 = Output disabled low power mode |
| [3]               | EN3_LP   | W/R  | Low power mode enable control for LV BUCK OUT3.     | 0 = Output enabled in low power mode<br>1 = Output disabled low power mode |

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|     |             |     |   |  |
|-----|-------------|-----|---|--|
|     |             |     |   | 1 = Output disabled low power mode   |
| [2] | EN2_LP      | W/R | Low power mode enable control for LV BUCK OUT2.                                     | 0 = Output enabled in low power mode<br>1 = Output disabled low power mode |
| [1] | RESERVED    | R   | /   | /  |
| [0] | LOWPOWER_EN | W/R | Low power mode Enable. This bit has self-clear function when state quit from SLEEP. | 0 = Disabled.<br>1 = Enabled.  |

## CONFIG\_PGSEL1 [7:0]

ADDRESS: 0x19

| BITS  | FIELD        | TYPE | DESCRIPTION                                    | DECODE                                       |
|-------|--------------|------|--|--|
| [7:6] | DEEP_OVP_SEL | W/R  | Deep OVP threshold selection for all channels. | 00 = +15%, others are reserved               |
| [5:4] | DEEP_UVP_SEL | W/R  | Deep UVP threshold selection for all channels. | 00 = -25%; 01 = -20%; 10 = -15%; 11 = -10%   |
| [3:2] | RESERVED     | R    | /  | /  |
| [1:0] | PG5_SEL      | W/R  | OUT5 OV/UV threshold selection.                | 00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10% |

## CONFIG\_PGSEL2 [7:0]

ADDRESS: 0x1A

| BITS  | FIELD   | TYPE | DESCRIPTION                     | DECODE                                       |
|-------|---------|------|---------------------------------|--|
| [7:6] | PG4_SEL | W/R  | OUT4 OV/UV threshold selection. | 00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10% |
| [5:4] | PG3_SEL | W/R  | OUT3 OV/UV threshold selection. | 00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10% |
| [3:2] | PG2_SEL | W/R  | OUT2 OV/UV threshold selection. | 00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10% |
| [1:0] | PG1_SEL | W/R  | OUT1 OV/UV threshold selection. | 00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10% |

## CONFIG\_SLEEPB [7:0]

ADDRESS: 0x1B

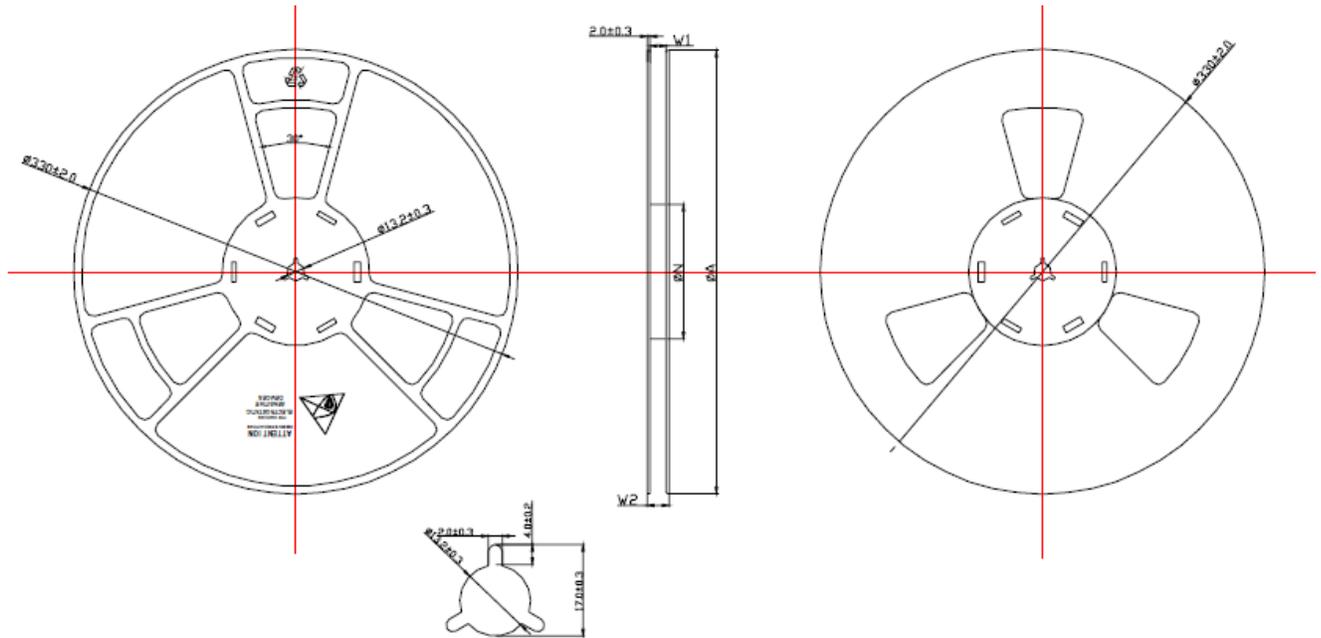
| BITS  | FIELD        | TYPE | DESCRIPTION   | DECODE                                      |
|-------|--------------|------|---|---|
| [7:6] | RESERVED     | W/R  | /   | /   |
| [5:4] | SLEEPB_BLANK | W/R  | SLEEPB Pin blanking time after RESETB change from low to high. During this time, SLEEPB pin need change high if do not need enter sleep mode. | 00 = 0ms; 01 = 2.5ms; 10 = 5ms; 11 = 10ms   |
| [3:2] | SLEEPB_DLYR  | W/R  | Select SLEEPB pin rising deglitch time, PMIC wake up after SLEEPB changes high for this time.   | 00 = 100us, 01 = 50us, 10 = 20us, 11 = 10us |
| [1:0] | SLEEPB_DLYF  | W/R  | Select SLEEPB pin falling deglitch time, PMIC enter low power mode after SLEEPB changes low for this time.                                    | 00 = 100us, 01 = 50us, 10 = 20us, 11 = 10us |

| I2C_LOCK [7:0] |          |      |   |   |
|----------------|----------|------|---|---|
| ADDRESS: 0x1C  |          |      |   |   |
| BITS           | FIELD    | TYPE | DESCRIPTION   | DECODE  |
| [7:1]          | RESERVED | R    | /   | /   |
| [0]            | I2C_LOCK | W/R  | Lock Protection. If 0 by default, then this bit can be changed through the I2C. | 0 = All registers can be written.<br>1 = Writes are ignored to protected registers. |

| SYS_STATE [7:0] |             |      |                                    |   |
|-----------------|-------------|------|------------------------------------|---|
| ADDRESS: 0x22   |             |      |                                    |   |
| BITS            | FIELD       | TYPE | DESCRIPTION                        | DECODE  |
| [7]             | OTP_CRC_ERR | R    | when OTP CRC has error, this bit=1 | 0 = pass<br>1 = fail  |
| [6]             | ABIST_ERR   | R    | when ABIST has error, this bit=1   | 0 = pass<br>1 = fail  |
| [5]             | LBIST_ERR   | R    | when LBIST has error, this bit=1   | 0 = pass<br>1 = fail  |
| [4]             | RESERVED    | R    | /                                  | /   |
| [3:0]           | SYS_STATE   | R    | System state machine.              | 0000 = IDLE, 0001 = LBIST, 0010 = DEEPSAFE, 0011 = LOADOTP, 0100 = SLEEP, 0101 = NORMAL, 0110 = ABIST, 0111 = POWERUP, 1000 = others, 1001 = others, 1010 = others, 1011 = others, 1100 = RECOVER, 1101 = RESET, 1110 = RCVRST, 1111 = others |

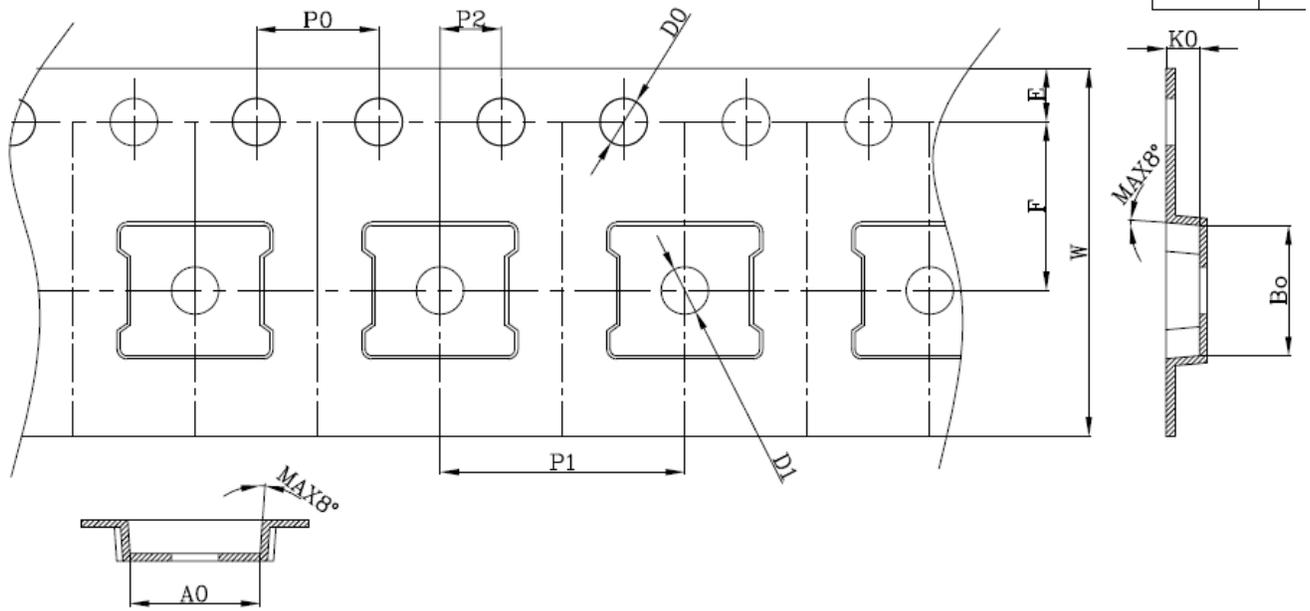


**TAPE AND REEL INFORMATION**



| PRODUCT SPECIFICATIONS |               |               |          |          |
|------------------------|---------------|---------------|----------|----------|
| TYPE WIDTH             | $\phi A$      | $\phi N$      | W1 (Min) | W2 (Max) |
| 12MM                   | $330 \pm 2.0$ | $100 \pm 1.0$ | 12.4     | 19.4     |
| 16mm                   | $330 \pm 2.0$ | $100 \pm 1.0$ | 16.4     | 23.4     |
| 24MM                   | $330 \pm 2.0$ | $100 \pm 1.0$ | 24.4     | 31.4     |
| 32MM                   | $330 \pm 2.0$ | $100 \pm 1.0$ | 32.4     | 39.4     |
| 44MM                   | $330 \pm 2.0$ | $100 \pm 1.0$ | 44.4     | 51.4     |

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|        |           |           |           |           |           |            |
|--------|-----------|-----------|-----------|-----------|-----------|------------|
| SYMBOL | A0        | B0        | K0        | P0        | P1        | P2         |
| SPEC   | 4.30±0.10 | 4.30±0.10 | 1.10±0.10 | 4.00±0.10 | 8.00±0.10 | 2.00±0.05  |
| SYMBOL | T         | E         | F         | D0        | D1        | W          |
| SPEC   | 0.30±0.05 | 1.75±0.10 | 5.50±0.05 | 1.55±0.05 | 1.55±0.10 | 12.00±0.30 |