19V Vin Quad Channel Power Management IC for Automotive Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range: 3.5-19V
- Three High-Efficiency Step-Down Converters:
  - HV Buck1: Vout1=2.7-5V with 100mV Steps, Up to 2A Continuous Output Current
  - LV Buck2/3: Vout2/3=0.6-2.15V with 50mV Steps, Up to 2A Continuous Output Current
- One Low-Dropout Regulator (LDO):
  - LDO4: Vout4=1.6-3.5V with 50mV Steps, Up to 300mA Continuous Output Current
  - High PSRR: 60dB@10kHz, 60dB@100kHz, 40dB@1MHz
  - Low noise: 30μV rms total integrated noise from 100Hz to 100kHz
- ±2% Output Voltage Accuracy
- 2.2MHz Fixed Switching Frequency
- Integrated Frequency Dither for EMI Mitigation
- Selectable Light-load Operation: FCCM/PSM
- Programmable Power Sequencer
- Selectable RESETB Output: Open-drain/Push-pull
- Two GPIOs for Flexible System Management
- Integrated Protection Features:
  - Output Over-voltage/Under-voltage Protection
  - Over Current Protection
  - Input Under-voltage Lockout
  - Input Over-voltage Protection
  - Thermal Shutdown Protection: 175°C
- QA & Simple Watchdog
- Up to 1MHz I2C Interface with Optional Packet Error Checking (PEC)
- Available in QFN-20L(2.5mm×3.5mm) Package with Wettable Flanks

APPLICATIONS

- Compact Camera Module
- Cabin Monitor

DESCRIPTION

The SCT61242Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2 and LV Buck3) and one high-PSRR, low noise LDO (LDO4) with OV/UV monitoring and flexible power sequence for all outputs.

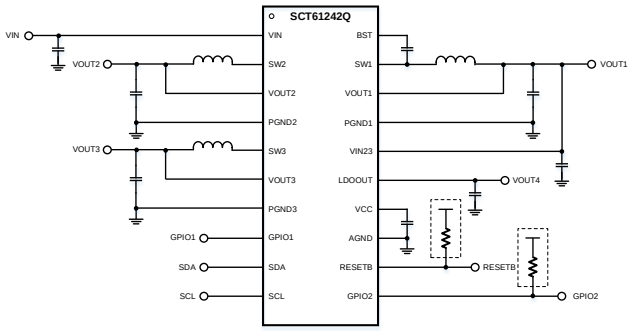
Buck1 has an input voltage range from 3.5 to 19V for connections to Power over Coax (PoC). Buck2 and Buck3 are identical and powered from the output of Buck1. All three buck converters can operate in either FCCM or PSM mode at light load, with 2.2MHz switching frequency and optional Frequency Spread Spectrum (FSS) function for EMI mitigation. LDO4 is a high PSRR, low noise LDO designed for analog power rail with a continuous output current of up to 300mA. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution.

The SCT61242Q is featured with two configurable GPIO pins for flexible system management. For instance, GPIO1 could be configured as external voltage monitor input while GPIO2 configured as external regulator enable output to monitor and control an external power rail.

The SCT61242Q integrated protection features including input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown at 175°C.

The SCT61242Q is available in a 2.5mm×3.5mm QFN-20L package with wettable flanks.

TYPICAL APPLICATION



REVISION HISTORY

Revision 0.8: Customer Sample.

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT61242Q-xxxxFHAR	Tape & Reel	5000	1242Q	20	FCTQFN2.5X3.5-20L	1

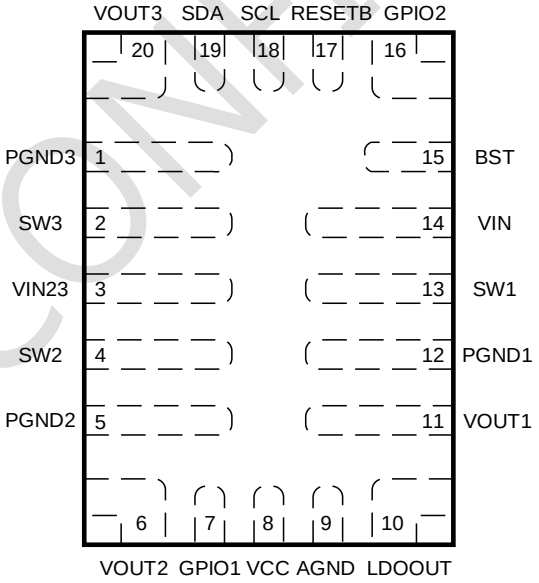
1) "xxxx" is the specific suffix code for different configuration. Contact SCT for details.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	21(23 in 100ms)	V
SW1	-0.3(-1 in 30ns)	21	V
BST-SW1	-0.3	6	V
Others	-0.3	6	V
Operation junction temperature T_J (2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 20-Lead FCTQFN 2.5mm×3.5mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 175°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	PIN	PIN FUNCTION
PGND3	1	**Power ground for Buck3.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW3	2	**Buck3 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN23	3	**Input supply voltage for Buck2 and Buck3.** VIN23 assumes to connect to the output of Buck1. Place a ceramic decoupling capacitor (10uF) from VIN23 to PGND2/3.
SW2	4	**Buck2 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
PGND2	5	**Power ground for Buck2.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT2	6	**Feedback for Buck2.** Connect VOUT2 pin to the Buck2 output directly.
GPIO1	7	**General Purpose Input/Output pin1.** GPIO1 can be configured as INTB or VMON.
VCC	8	**Internal VCC regulator output.** Power supply to the internal control circuit and gate drivers. A 1uF decoupling capacitor to ground close to this pin is required.
AGND	9	**Analog ground.** AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to Power Ground, make sure AGND connected to power ground in PCB.
LDOOUT	10	**LDO4 output.** Connect a 4.7uF or higher ceramic capacitor between this pin and ground.
VOUT1	11	**Feedback for Buck1 and power source for LDO4.** Connect VOUT1 pin to Buck1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 pin to minimize switching spikes.
PGND1	12	**Power ground for Buck1.** Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
SW1	13	**Buck1 switch node.** SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VIN	14	**Input supply for the device and Buck1.** A decoupling capacitor to ground is recommended to be placed close to VIN pin to minimize switching spikes.
BST	15	**Bootstrap capacitor connection pin for Buck1.** Connect a 0.1uF ceramic capacitor between this pin and SW1.
GPIO2	16	**General Purpose Input/Output pin2.** GPIO2 can be configured as SEQOUT, PG, GPO, INTB, ERRIN, WDI, SLEEPB or RSTIN.
RESETB	17	**Reset Output.** High state of this pin indicates all channels work properly and low state indicates power rails are not ready or a fault condition. RESETB could be configured as either open-drain or push-pull. Float this pin if not used.
SCL	18	**Serial clock line.** Connect this pin to ground if not used.
SDA	19	**Serial data line.** Open-Drain I/O, connect this pin to a high level via a pull-up resistor. Connect this pin to ground if not used.
VOUT3	20	**Feedback for Buck3.** Connect VOUT3 pin to the Buck3 output directly.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	VIN input voltage range	3.5	19	V
V_{IN23}	VIN23 input voltage range	2.7	5.5	V
V_{OUT1}	HV Buck1 output voltage range	2.7	5	V
V_{OUT2}	LV Buck2 output voltage range	0.6	2.15	V
V_{OUT3}	LV Buck3 output voltage range	0.6	2.15	V
V_{OUT4}	LDO4 output voltage range	1.6	3.5	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	46.25	°C/W
ψ_{JT}	Junction-to-top characterization parameter(1)	2.1	
ψ_{JB}	Junction-to-board characterization parameter(1)	3.85	
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	40.95	
$R_{\theta JB}$	Junction to board thermal resistance(1)	3.95	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61242Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61242Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN} = 10V, T_J = -40°C to 150°C, unless otherwise stated. Typical values are at T_J = 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Input voltage range		3.5		19	V
V_{IN_START}	Input rising threshold to initiate power up sequence	VIN_START[1:0]=00	3	3.2	3.4	V
		VIN_START[1:0]=01	3.8	4	4.2	V
		VIN_START[1:0]=10	4.8	5	5.2	V
		VIN_START[1:0]=11	5.8	6	6.2	V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN_STOP}	Input falling threshold to initiate power down sequence	VIN_STOP[1:0]=00	2.6	2.8	3	V
		VIN_STOP[1:0]=01	3.3	3.5	3.7	V
		VIN_STOP[1:0]=10	4.3	4.5	4.7	V
		VIN_STOP[1:0]=11	5.3	5.5	5.7	V
V_{IN_OVP}	Input OVP rising threshold		20	21	22	V
$V_{IN\_OVP\_HYS}$	Input OVP hysteresis			1.5		V
I_Q(1)	Quiescent current from VIN	No load, V_{OUT1}=3.3V, FCCM		16		mA
		Sleep Mode, Buck1 is on, Buck2/3 and LDO4 is off		0.6		mA
		All channels off via I2C		1		mA
VCC Power						
V_{CC}	Internal linear regulator		4.85	5	5.15	V
V_{CC_UVLO}	VCC UVLO rising threshold		2.6	2.8	3	V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis			200		mV
V_{CC_OVP}	VCC OVP rising threshold		5.2	5.5	5.8	V
$V_{CC\_OVP\_HYS}$	VCC OVP hysteresis			200		mV
Oscillator and Timing						
f_{DIG}	Digital clock frequency		3.6	4	4.4	MHz
f_{SW}	Switching frequency	Buck1/2/3	2	2.2	2.4	MHz
f_{FSS_RANGE}	Spread spectrum range	FSS_RANGE[0]=0		±8		%
		FSS_RANGE[0]=1		±4		%
f_{FSS}	Spread spectrum frequency	FSS_PERIOD[0]=0		4		kHz
		FSS_PERIOD[0]=1		8		kHz
t_{SS}	Soft start time	Buck1/2/3, LDO4	0.7	0.8	0.9	ms
t_{ON_SEQ}	Turn-on sequence delay time configuration	ON_DELAY_SCALE[1:0] =00, SEQx[3:0]=0000		0		ms
		ON_DELAY_SCALE[1:0] =00, SEQx[3:0]=0001	0.45	0.5	0.55	ms
		ON_DELAY_SCALE[1:0] =11, SEQx[3:0]=1111	54	60	66	ms
t_{OFF_SEQ}	Turn-off sequence delay time configuration	OFF_DELAY_SCALE[1:0] =00, SEQx[3:0]=0000		0		ms
		OFF_DELAY_SCALE[1:0] =00, SEQx[3:0]=0001	0.45	0.5	0.55	ms
		OFF_DELAY_SCALE[1:0] =11, SEQx[3:0]=1111	54	60	66	ms
t_{RSTB_DLYR}	RESETB rising delay time	RESETB_DLYR_SCALE[0] =0, RESETB_DLYR[1:0]=00	0.4	0.5	0.6	ms
		RESETB_DLYR_SCALE[0] =0, RESETB_DLYR[1:0]=01	0.8	1	1.2	ms
		RESETB_DLYR_SCALE[0] =1, RESETB_DLYR[1:0]=11	16	20	24	ms
t_{RSTB_HT}	RESETB assertion low-level hold time	RESETB_HT[1:0]=00		10		ms
		RESETB_HT[1:0]=01		20		ms
		RESETB_HT[1:0]=10		30		ms
		RESETB_HT[1:0]=11		40		ms

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
HV BUCK1						
V_{OUT1}	Output voltage configurable range		2.7		5	V
V_{OUT1_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-2		2	%
R_{DSON_HS1}	High-side MOSFET on-resistance	V_{BST}-V_{SW}=5V		175	350	mΩ
R_{DSON_LS1}	Low-side MOSFET on-resistance			75	150	mΩ
I_{LIM_HS1}	High-side peak current limit		2.4	3	3.8	A
I_{LIM_LSP1}	Low-side valley current limit		2.1	2.6	3.1	A
I_{LIM_LSN1}	Low-side reverse current limit		1.4	2	2.6	A
R_{DIS1}	Output discharge resistance	Output disabled		50	100	Ω
t_{ON_MIN1}	Minimum on-time			70		ns
θ_{Phase1}(1)	Switching phase			0		Deg
LV BUCK2						
V_{IN23}	Supply voltage range		2.7		5.5	V
V_{OUT2}	Output voltage configurable range		0.6		2.15	V
V_{OUT2_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-2		2	%
R_{DSON_HS2}	High-side MOSFET on-resistance			80	150	mΩ
R_{DSON_LS2}	Low-side MOSFET on-resistance			50	120	mΩ
I_{LIM_HS2}	High-side peak current limit		2.2	3.2	4	A
I_{LIM_LSP2}	Low-side valley current limit		2.1	2.6	3.1	A
I_{LIM_LSN2}	Low-side reverse current limit		1.4	2	2.6	A
R_{DIS2}	Output discharge resistance	Output disabled		50	100	Ω
t_{ON_MIN2}	Minimum on-time			80		ns
θ_{Phase2}(1)	Switching phase			180		Deg
LV BUCK3						
V_{IN23}	Supply voltage range		2.7		5.5	V
V_{OUT3}	Output voltage configurable range		0.6		2.15	V
V_{OUT3_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-2		2	%
R_{DSON_HS3}	High-side MOSFET on-resistance			80	150	mΩ
R_{DSON_LS3}	Low-side MOSFET on-resistance			50	120	mΩ
I_{LIM_HS3}	High-side peak current limit		2.2	3.2	4	A
I_{LIM_LSP3}	Low-side valley current limit		2.1	2.6	3.1	A
I_{LIM_LSN3}	Low-side reverse current limit		1.4	2	2.6	A
R_{DIS3}	Output discharge resistance	Output disabled		50	100	Ω
t_{ON_MIN3}	Minimum on-time			80		ns
θ_{Phase3}(1)	Switching phase			0		Deg

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
LDO4						
V_{LDO4}	Output voltage configurable range		1.6		3.5	V
V_{LDO4_ACC}	Output voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C to 150°C	-2		2	%
V_{LDO4_DROP}	Dropout voltage	V_{OUT1}=3.3V, V_{LDO4} set to 3.3V, I_{LDO4}=300mA		120	240	mV
L_{LINE_REG4}	Line Regulation	V_{OUT1}=3V to 5V, V_{LDO4} set to 2.7V, I_{LDO4}=100mA		0.02		%/V
L_{LOAD_REG4}	Load Regulation	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V, I_{LDO4}=10mA to 300mA		0.1		%
I_{LIM_OCP4}	Over-current limit	V_{OUT1}=3.3V, V_{LDO4} set to 2.8V	320	400	500	mA
I_{LIM_SCP4}	Short-circuit current limit	V_{OUT1}=3.3V, V_{LDO4}=0V	40	70	100	mA
PSRR(1)	Power supply rejection ratio	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 10kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 100kHz		60		dB
		V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, @ 1MHz		40		dB
N_{RMS}(1)	RMS Noise	V_{OUT1}=3.3V, V_{LDO4}=2.8V, C_{LDO4}=4.7uF, I_{LDO4}=100mA, from 10Hz to 100kHz		30		μV_{RMS}
R_{DIS4}	Output discharge resistance	Output disabled		50	100	Ω
Protection						
V_{OV_R}	Output over-voltage rising threshold		106	108	110	%
V_{OV_HYS}	Output over-voltage hysteresis			2		%
V_{UV_F}	Output under-voltage falling threshold		90	92	94	%
V_{UV_HYS}	Output under-voltage hysteresis			2		%
V_{DPOV_R}	Output deep over-voltage protection rising threshold	DEEP_OVP_SEL[1:0]=00		115		%
		DEEP_OVP_SEL[1:0]=01		112		%
		DEEP_OVP_SEL[1:0]=10		110		%
		DEEP_OVP_SEL[1:0]=11		108		%
V_{DPOV_HYS}	Output deep over-voltage protection hysteresis			2		%
V_{DPUV_F}	Output deep under-voltage protection falling threshold	DEEP_UVP_SEL[1:0]=00		75		%
		DEEP_UVP_SEL[1:0]=01		80		%
		DEEP_UVP_SEL[1:0]=10		85		%
		DEEP_UVP_SEL[1:0]=11		90		%
V_{DPUV_HYS}	Output deep under-voltage protection hysteresis			2		%
t_{HICCUP}	Hiccup time		72	80	88	ms
T_{WR}	Thermal warning rising threshold		140	155	170	°C
T_{WR_HYS}	Thermal warning hysteresis			20		°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
T_{SD}	Thermal shutdown rising threshold		160	175	190	°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C
RESETB						
$V_{OL\_RSTB\_OD}$	Open-drain output low level voltage	I_{SINK}=1mA			0.1	V
$I_{LKG\_RSTB\_OD}$	Open-drain output high leakage current		-1		1	uA
$V_{OL\_RSTB\_PP}$	Push-pull output low level voltage	I_{SINK}=1mA			0.1	V
$V_{OH\_RSTB\_PP}$	Push-pull output high level voltage	VIO[0]=0	3	3.3	3.6	V
		VIO[0]=1	1.6	1.8	2	V
GPIO1						
$V_{OL\_GPIO1\_OD}$	Open-drain output low level voltage	I_{SINK}=1mA			0.1	V
$I_{LKG\_GPIO1\_OD}$	Open-drain output high leakage current		-1		1	uA
$V_{OL\_GPIO1\_PP}$	Push-pull output low level voltage	I_{SINK}=1mA			0.1	V
$V_{OH\_GPIO1\_PP}$	Push-pull output high level voltage	VIO[0]=0	3	3.3	3.6	V
		VIO[0]=1	1.6	1.8	2	V
V_{MON}	VMON voltage configurable range	GPIO1_SEL[0]=1	0.6		2.15	V
V_{MON_ACC}	VMON voltage accuracy	GPIO1_SEL[0]=1	-2		2	%
GPIO2						
$V_{OL\_GPIO2\_OD}$	Open-drain output low level voltage	I_{SINK}=1mA			0.1	V
$I_{LKG\_GPIO2\_OD}$	Open-drain output high leakage current		-1		1	uA
$V_{OL\_GPIO2\_PP}$	Push-pull output low level voltage	I_{SINK}=1mA			0.1	V
$V_{OH\_GPIO2\_PP}$	Push-pull output high level voltage	VIO[0]=0	3	3.3	3.6	V
		VIO[0]=1	1.6	1.8	2	V
V_{IH_GPIO2}	High level input voltage		1.2			V
V_{IL_GPIO2}	Low level input voltage				0.4	V
R_{PD_GPIO2}	Input pull-down resistance			2		MΩ
t_{GPIO2_BLK}	Input blanking time after RESETB pulled high	GPIO2_BLANK[1:0]=00		0		ms
		GPIO2_BLANK[1:0]=01	2.25	2.5	2.75	ms
		GPIO2_BLANK[1:0]=10	4.5	5	5.5	ms
		GPIO2_BLANK[1:0]=11	9	10	11	ms
t_{GPIO2_DLYR}	Input rising deglitch time	GPIO2_DLYR[1:0]=00	50	80	110	us
		GPIO2_DLYR[1:0]=01	25	40	55	us
		GPIO2_DLYR[1:0]=10	12.5	20	27.5	us
		GPIO2_DLYR[1:0]=11	6.25	10	13.75	us
t_{GPIO2_DLYF}	Input falling deglitch time	GPIO2_DLYF[1:0]=00	50	80	110	us
		GPIO2_DLYF[1:0]=01	25	40	55	us
		GPIO2_DLYF[1:0]=10	12.5	20	27.5	us
		GPIO2_DLYF[1:0]=11	6.25	10	13.75	us

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I2C Interface(1)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.4	V
V_{OL}	Low level output voltage	I_{SINK}=4mA			0.4	V
f_{SCL}	SCL clock frequency				1	MHz
t_{LOW}	Low period of the SCL clock		500			ns
t_{HIGH}	High period of the SCL clock		260			ns
t_{HD_STA}	Hold time (repeated) START condition		260			ns
t_{SU_STA}	Set-up time for a repeated START condition		260			ns
t_{HD_DAT}	Data hold time		0			ns
t_{SU_DAT}	Data set-up time		50			ns
t_{SU_STO}	Set-up time for STOP condition		260			ns
t_r	Rise time of both SCL and SDA signals				120	ns
t_f	Fall time of both SCL and SDA signals				120	ns
C_B	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample characterization, not tested in production.

TYPICAL CHARACTERISTICS

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

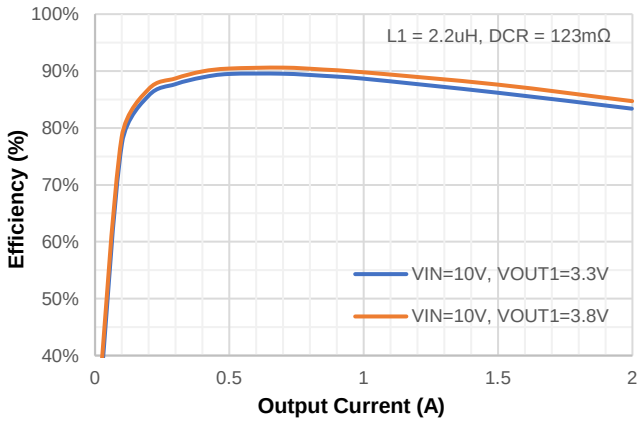


Figure 1. Buck1 Efficiency vs. Load Current

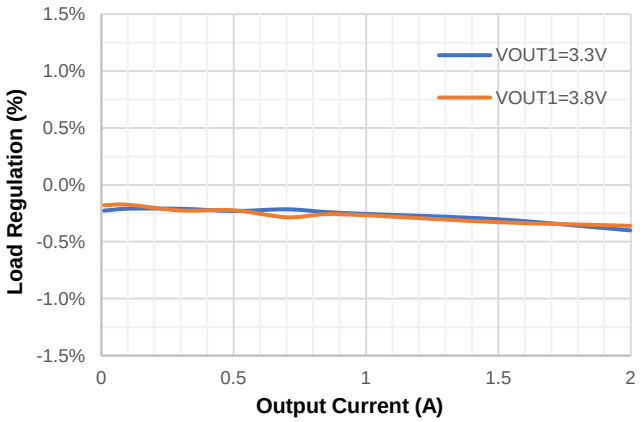


Figure 2. Buck1 Load Regulation

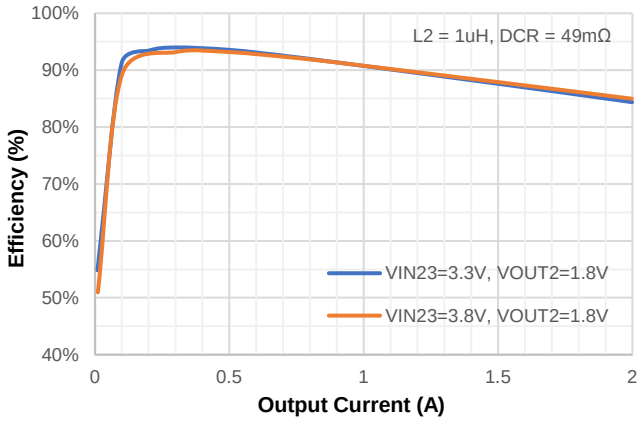


Figure 3. Buck2 Efficiency vs. Load Current

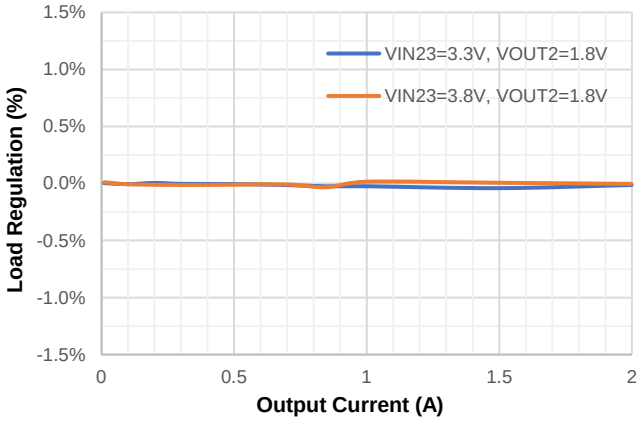


Figure 4. Buck2 Load Regulation

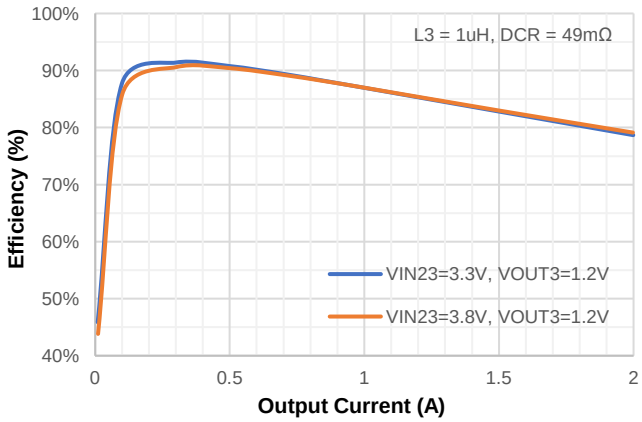


Figure 5. Buck3 Efficiency vs. Load Current

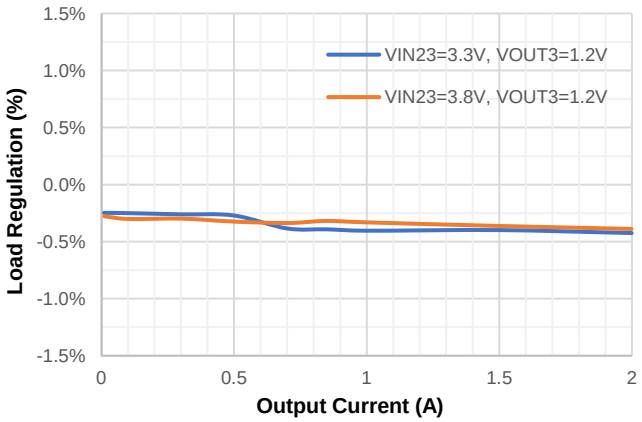


Figure 6. Buck3 Load Regulation

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

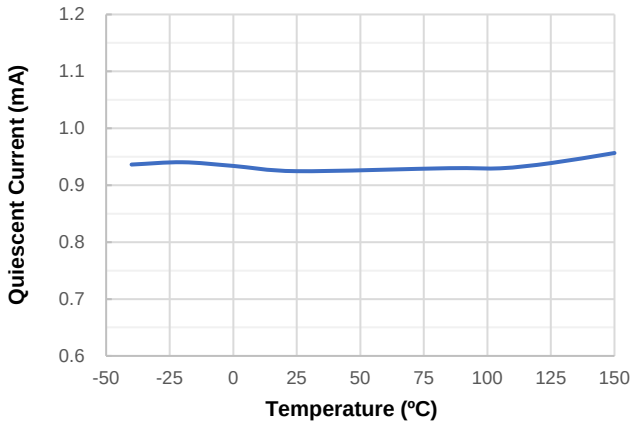


Figure 7. Quiescent Current (rails off) vs. Temperature

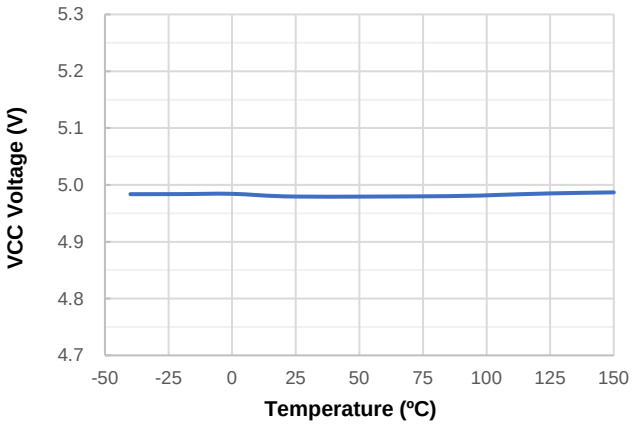


Figure 8. VCC Voltage vs. Temperature

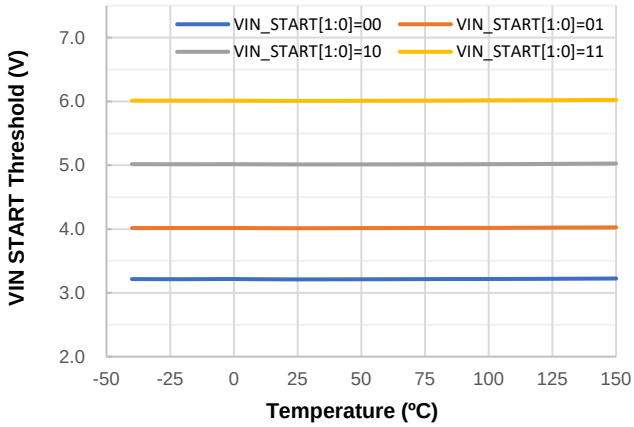


Figure 9. VIN START Threshold vs. Temperature

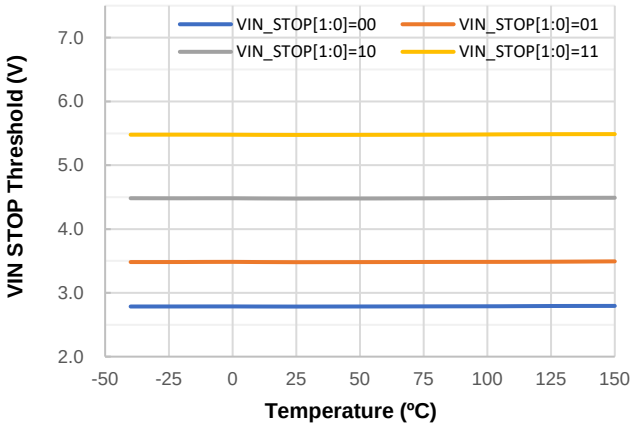


Figure 10. VIN STOP Threshold vs. Temperature

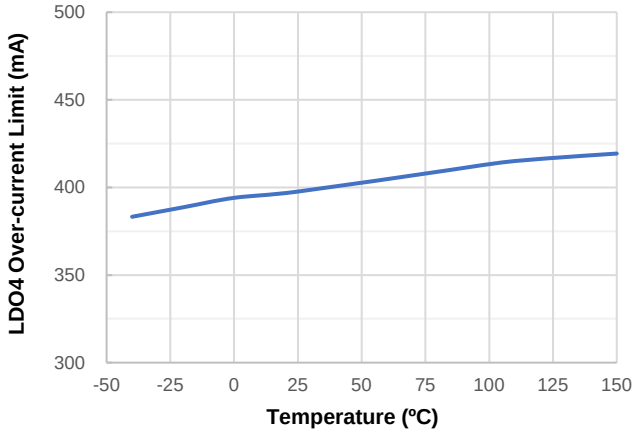


Figure 11. LDO4 Over-current Limit vs. Temperature

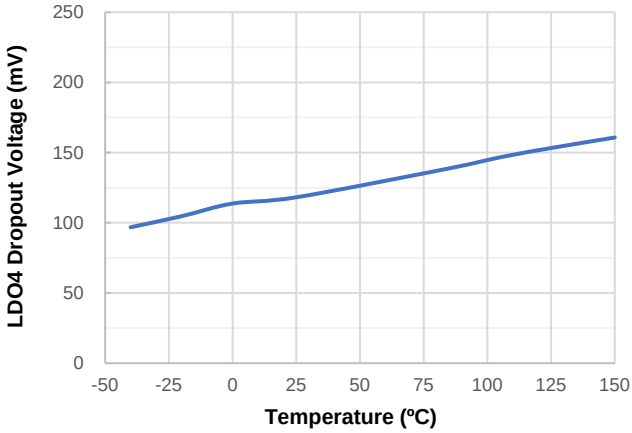


Figure 12. LDO4 Dropout Voltage vs. Temperature

FUNCTIONAL BLOCK DIAGRAM

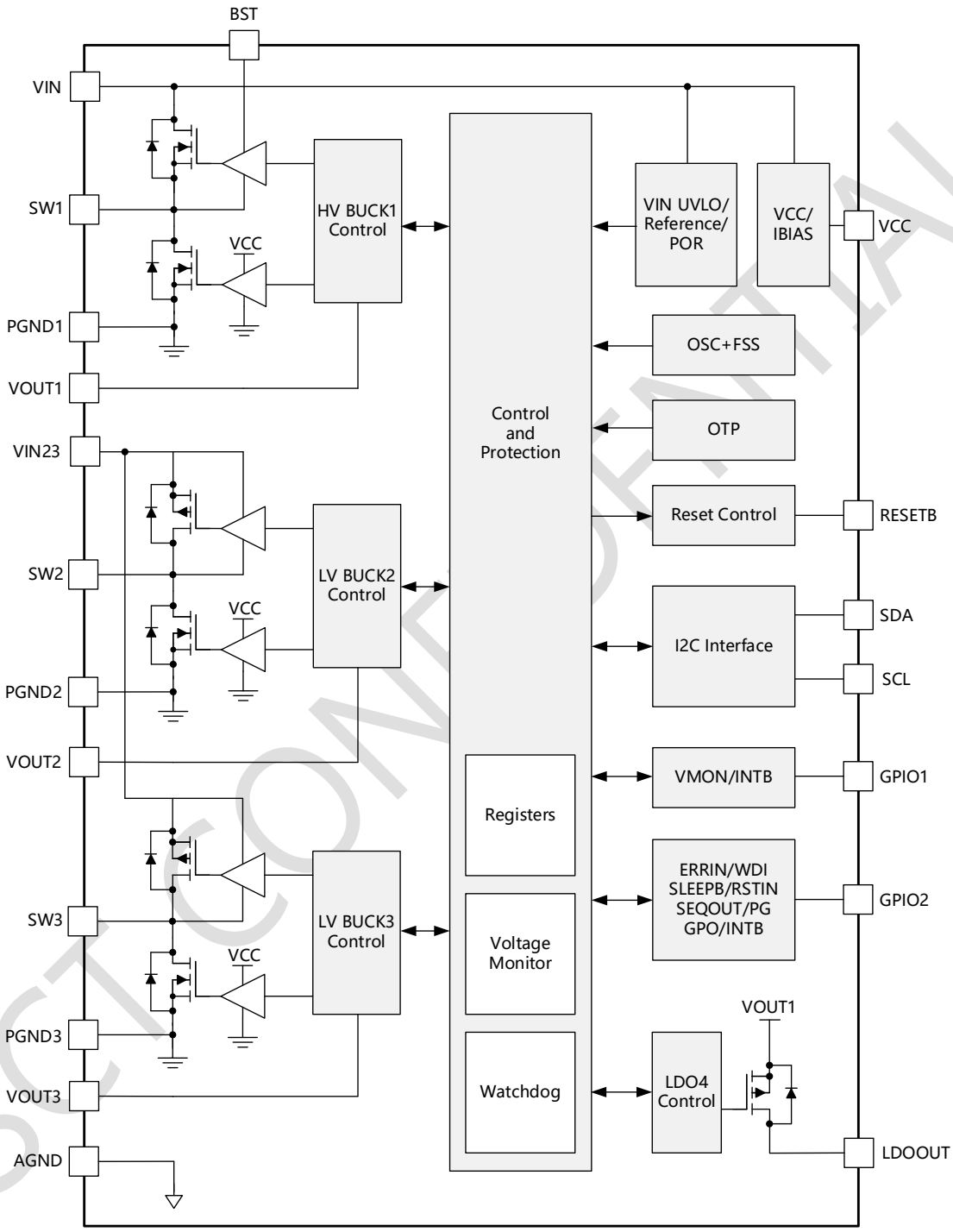


Figure 13. Functional Block Diagram

OPERATION

Overview

The SCT61242Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high-efficiency synchronous buck converters (HV Buck1, LV Buck2 and LV Buck3) and one high-PSRR, low noise LDO (LDO4) with OV/UV monitoring and flexible power sequence for all outputs.

Buck1 has an input voltage range from 3.5 to 19V for connection to Power over Coax (PoC). Buck2 and Buck3 are identical and powered from the output of Buck1. All three buck converters can operate in either FCCM or PSM mode at light load, with 2.2MHz switching frequency and optional Frequency Spread Spectrum (FSS) function for EMI mitigation. LDO4 is a high PSRR, low noise LDO designed for analog power rail with a continuous output current of up to 300mA. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution.

The SCT61242Q is featured with two configurable GPIO pins for flexible system management. GPIO1 can be configured to INTB (interrupt output) or VMON (external voltage monitor input). GPIO2 can be configured to SEQOUT (sequential output for external enable), PG (power good output), GPO (register-based output), INTB, ERRIN (logic input for power cycle), WDI (watchdog input), SLEEPB (sleep mode input) and RSTIN (logic input for reset). For instance, GPIO1 could be configured as VMON while GPIO2 configured as SEQOUT, in which case an external power rail is used, monitored and controlled. The two GPIO pins supports open-drain output and push-pull output of either 1.8V or 3.3V level. Fail-safe feature is also integrated to avoid any unexpected current sinking.

The SCT61242Q integrated protection features including input under-voltage protection, input over-voltage protection, output over-voltage/under-voltage protection, over-current protection and thermal shutdown.

Operating State Machine

The operation state machine of SCT61242Q is shown in Figure 14. The power rail action and system function in each state are listed in Table 1.

Table 1. PMIC Operation in Each State

<table>
<tr><th rowspan="2">State</th><th colspan="4">Power Rail</th><th colspan="5">Function</th></tr>
<tr><th>Buck1</th><th>Buck2</th><th>Buck3</th><th>LDO4</th><th>RESETB</th><th>I2C</th><th>Watchdog</th><th>TSD</th><th>Register</th></tr>
<tr><td>IDLE</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td rowspan="3">OFF</td><td>Hi-Z</td><td rowspan="2">OFF</td><td rowspan="3">OFF</td><td rowspan="2">OFF</td><td>Reset</td></tr>
<tr><td>LOADOTP</td><td rowspan="2">Low</td><td rowspan="5">\</td></tr>
<tr><td>STANDBY</td><td rowspan="5">ON</td><td rowspan="8">ON</td></tr>
<tr><td>POWERUP</td><td rowspan="5">ON</td><td rowspan="3">ON</td><td rowspan="3">ON</td><td rowspan="3">ON</td></tr>
<tr><td>NORMAL</td><td>High</td><td>ON</td></tr>
<tr><td>RESET</td><td>Low</td><td>OFF</td></tr>
<tr><td>SLEEP</td><td>ON/OFF</td><td>ON/OFF</td><td>ON/OFF</td><td rowspan="2">High</td><td>OFF</td><td rowspan="2">ON</td></tr>
<tr><td>RECOVER</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="2">ON</td><td rowspan="3">ON</td></tr>
<tr><td>RCVRST</td><td rowspan="3">Low</td><td rowspan="3">OFF</td></tr>
<tr><td>DEEPSAFE</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td><td rowspan="2">OFF</td></tr>
<tr><td>TURNOFF</td></tr>
</table>

IDLE State

The device enters IDLE state whenever VCC is below VCC UVLO threshold. All functional blocks are disabled and all registers are reset. VCC is powered from VIN through internal linear regulator after power-on. The device will exit IDLE state and jump to LOADOTP state when VCC reached its rising UVLO threshold.

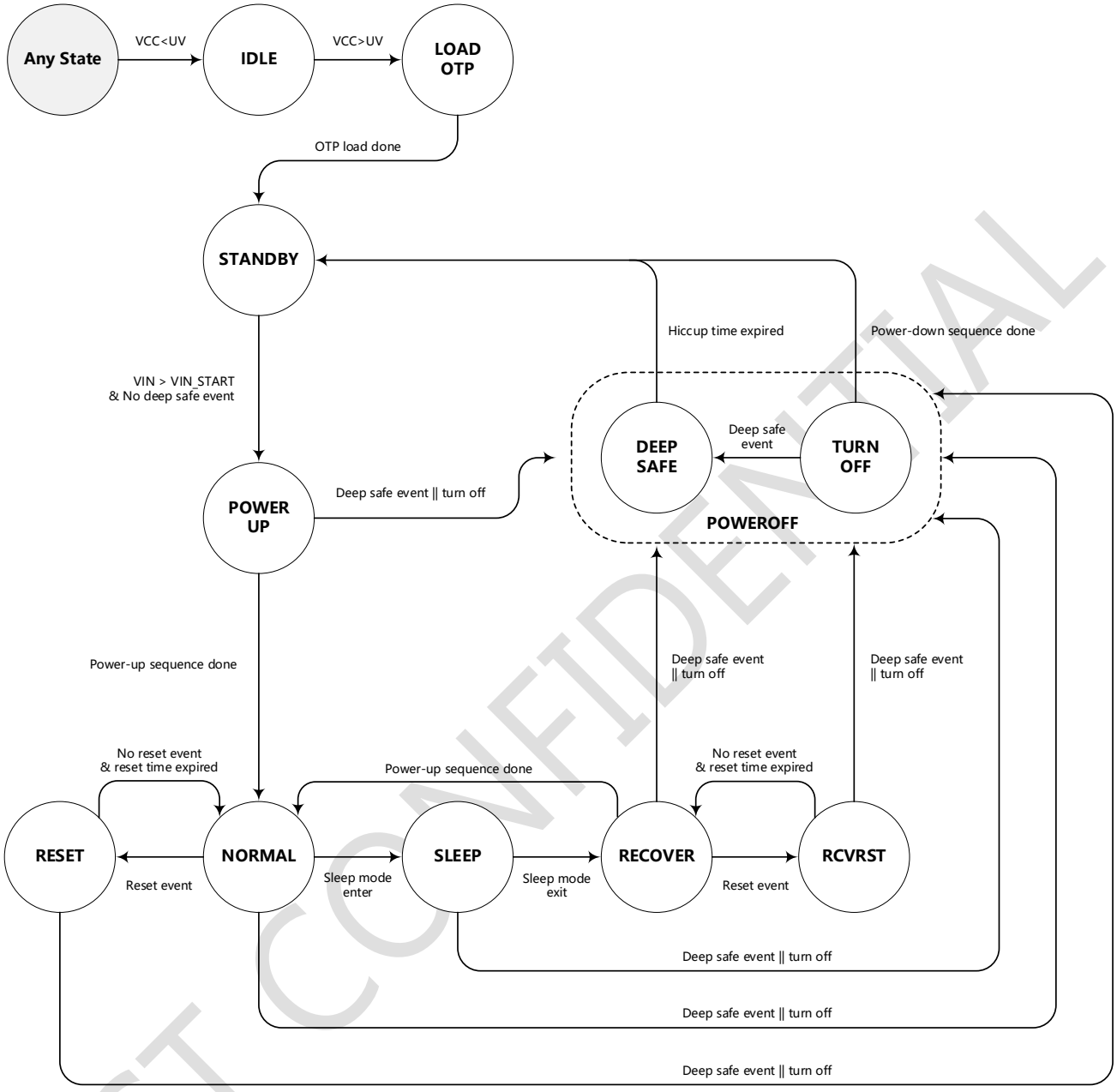


Figure 14. Operating State Machine and Transitions

LOADOTP State

Once the device enters LOADOTP state, OTP data will be loaded into corresponding registers, then STANDBY state is entered.

STANDBY State

STANDBY state is where the device could be held on to check and wait for all conditions met to power up. To exit STANDBY state, VIN shall be higher than V_{IN_START} threshold, output rails shall be discharged and no other critical fault like thermal shutdown is triggered. The device will transit to POWERUP state almost immediately if all conditions are met when entering STANDBY state.

POWERUP State

In POWERUP state, all power rails will be built up following a dedicated OTP-programmed sequence. Since HV Buck1 is usually the power supply for the other channels, Buck1 is always set to start up first. The other channels then will start up with their own turn-on delay time configuration respectively, which is configured in register **CONFIG_SEQ45** and **CONFIG_SEQ23**. See Figure 20 for a detailed power up sequence. If all channels finish soft-start within power good range, the RESETB rising delay timer starts. Once the timer is expired, the device will enter NORMAL state and RESETB pin will be pulled high. If any deep safe event occurs, the device will transit to DEEPSAFE state directly.

NORMAL State

NORMAL state is the normal operation state of the device with all enabled channels on. RESETB pin is pulled high upon entering this state. If watchdog is enabled in register **CONFIG_WD3**, the watchdog window cycle will be initiated and watchdog shall be fed by periodic trigger pulse through GPIO2 as WDI or specific I2C write operation at correct timing. SLEEP state could be entered if **EN_LP[0]**=1 and SLEEPB is pulled low when GPIO2 configured as SLEEPB, where low power mode is activated and a very low standby current is achieved. When operating in NORMAL state, the device will transit to RESET state once any reset event occurs.

RESET State

All power rails keep on with just RESETB pin pulled low in RESET state. The device transits from NORMAL state to RESET state when any of the reset events shown in Table 2 occurs. When the device enters RESET state, RESETB pin will be pulled low for a hold time configured in **RESETB_HT[1:0]**. The device will go back to NORMAL state once the hold time expired and the reset event discontinued. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET to NORMAL state. If some reset events are not needed or undesired, the device provides corresponding mask options in register **CTRL_FLTMAP1** and **CTRL_FLTMAP2**.

Table 2. Reset Event

Category	Reset Event	Map/Mask Bit	Status Bit
Analog	Buck1 output is out of OV/UV range	RSTMAP_VO1[0]	OV1[0], UV1[0]
	Buck2 output is out of OV/UV range	RSTMAP_VO2[0]	OV2[0], UV2[0]
	Buck3 output is out of OV/UV range	RSTMAP_VO3[0]	OV3[0], UV3[0]
	LDO4 output is out of OV/UV range	RSTMAP_VO4[0]	OV4[0], UV4[0]
	VMON input is out of OV/UV range (when GPIO1 configured as VMON)	RSTMAP_VMON[0]	OV5[0], UV5[0]
	VMON deep OVP/UVP (when VMON_DEEPSAFE_CTRL[0]=1)	RSTMAP_VMONDP[0]	DEEPOVP5[0], DEEPUVP5[0]
	VIN OVP (when VINOVP_DEEPSAFE_CTRL[0]=1)	RSTMAP_VINOVP[0]	VIN_OVP[0]
Digital	Watchdog failure	RSTMAP_WD[0]	WD_ERR[0]
	I2C PEC error	RSTMAP_I2C[0]	I2C_PEC_ERR[0]
	RSTIN input high (when GPIO2 configured as RSTIN)	RSTMAP_RSTIN[0]	RSTIN[0]

SLEEP State

The device provides a low-power sleep mode where each channel could be configured to turn off or operate in PSM to reduce power consumption. The device transits from NORMAL state to SLEEP state when **EN_LP[0]** is set to 1 and SLEEPB is pulled low (GPIO2 configured as SLEEPB). RESETB pin remains high and I2C operation is disabled in SLEEP state. Once SLEEPB is pulled high, the device will be awakened, going through RECOVER state and back to NORMAL state with **EN_LP[0]** self-cleared to 0.

RECOVER State

RECOVER state is an intermediate state when the device is awakened from SLEEP state. The channels disabled in SLEEP state will start up with the turn-on delay time same as in POWERUP state, and other channels will resume to FCCM operation. After all outputs are built up successfully, the device will enter NORMAL state. If any reset event triggered in RECOVER state, the device goes to RCVRST state.

RCVRST State

RCVRST state is an extra reset state to assert RESETB pin with output rails keep starting up in programmed sequence. This state aims to allow possible reset events to be triggered for those continuously enabled rails, like an output OV/UV. The device will go back to RECOVER state automatically once the hold time expired and the reset event discontinued.

TURNOFF State

If the device is manually turned off (e.g., writing **EN_ALL[0]**=0 online), or VIN drops to lower than V_{IN_STOP} threshold after start-up, TURNOFF state will be entered. All channels will be shut down with their turn-off delay time configuration in register **CONFIG_SEQ45** and **CONFIG_SEQ23**. See Figure 21 for a detailed power down sequence. After power down sequence is finished, the device will go back to STANDBY state waiting for reboot. If any deep safe event triggered in TURNOFF state, the device transits to DEEPSAFE state.

DEEPSAFE State

In DEEPSAFE state, all channels are shut off and RESETB pin is pulled low. Regardless of current state, the device can always jump to DEEPSAFE state when any of the deep safe events shown in Table 3 occurs after start-up. All power rails are shut down immediately and simultaneously while I2C interface keeps alive in DEEPSAFE state, allowing user to communicate with the device and read the status registers to locate the specific fault. The device will go back to STANDBY state once the hiccup timer expired and the deep safe event discontinued.

Table 3. Deep Safe Event

Category	Deep Safe Event	Status Bit
Analog	Buck1 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP1[0], DEEPUVP1[0], UV1[0], OC1[0]
	Buck2 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP2[0], DEEPUVP2[0], UV2[0], OC2[0]
	Buck3 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP3[0], DEEPUVP3[0], UV3[0], OC3[0]
	LDO4 output is out of deep OVP/UVP range or UV along with OC	DEEPOVP4[0], DEEPUVP4[0], UV4[0], OC4[0]
	VMON deep OVP/UVP (when VMON_DEEPSAFE_CTRL[0]=0)	DEEPOVP5[0], DEEPUVP5[0],
	VIN OVP (when VINOVP_DEEPSAFE_CTRL[0]=0)	VIN_OVP[0]
	VCC OVP	VCC_OVP[0]
	Thermal shutdown	THSD[0]
Digital	ERRIN input high (when GPIO2 configured as ERRIN)	ERRIN[0]

High Efficiency Regulators

All three buck converters employ 2.2MHz fixed frequency peak current mode control. Optional Forced Continuous Conduction Mode (FCCM) ensures good output performance at light-load, or Pulse Skip Mode (PSM) to provide excellent light-load efficiency. HV Buck1 is always the first one to power up, LV Buck2 and LV Buck3 then will start up with corresponding turn-on delay time configuration. The soft-start time is fixed at 0.8ms for all three buck converters.

Buck1 is a high-voltage synchronous buck converter directly powered from VIN pin. Buck1 output can be regulated at 2.7V to 5V with down to 100mV steps, providing a continuous output current of up to 2A. An external 100nF ceramic capacitor between BST and SW1 pins is required to power high-side power MOSFET gate driver, which is charged from VCC when low-side power MOSFET is on. Buck1 output is the power supply for other channels.

Buck2 and Buck3 are two identical low-voltage synchronous buck converter powered by Buck1. Both Buck2 and Buck3 output can be regulated at 0.6V to 2.15V with 50mV steps, providing up to 2A continuous output current. To further improve the EMI performance, Buck2 and Buck3 will operate in 180° phase shift.

LDO4 is a high PSRR, low noise LDO designed for analog power rail, also powered from Buck1. LDO4 output can be regulated at 1.6V to 3.5V with 50mV steps, providing a continuous output current of up to 300mA.

All output voltages are pre-programmed without any external feedback divider, and continuously monitored during operation. There is a two-stage OV/UV protection strategy. Any output OV/UV condition will trigger a reset event to pull RESETB pin low. For worse OV/UV cases, deep over-voltage protection or deep under-voltage protection will kick in to shut down all channels, as a deep safe event.

Deep Over-voltage Protection

If any output voltage exceeds the deep over-voltage protection threshold configured in **DEEP_OVP_SEL[1:0]** during operation, a deep safe event is triggered and all outputs will be shut down for the hiccup time. In this hiccup time, all output rails will be discharged by internal circuit. When the hiccup timer expired and the deep over-voltage condition discontinued, the device will start up again with configured power up sequence.

Deep Under-voltage Protection

If any output voltage falls below the deep under-voltage protection threshold configured in **DEEP_UVP_SEL[1:0]** during operation, a deep safe event is triggered and all outputs will be shut down for the hiccup time. In this hiccup time, all output rails will be discharged by internal circuit. When the hiccup timer expired and the deep under-voltage condition discontinued, the device will start up again with configured power up sequence.

Over Current Protection

The buck converters implement over current protection with cycle-by-cycle limit for both high-side power MOSFET peak current and low-side power MOSFET valley current to avoid inductor current running away during unexpected overload or output short-circuit. When the converter is not able to provide enough output current to meet loading requirement with the inductor current already clamped at the over current limit, the output voltage drops below the regulation target. If the peak current limit is kicked for continuous 32 times and the output voltage is below its UV threshold, the converter will stop switching and the device will transit to DEEPSAFE state. After a hiccup time, the device will try to restart again, but transit to DEEPSAFE state again if over-load condition not removed. The hiccup protection mode greatly reduces the average short-circuit current to alleviate thermal issues and protect the device. Once over-load condition removed, the device would recover to normal operation in NORMAL state.

For LDO4, if the load current is higher than its current limit, the output voltage will start to drop and the input current will be clamped at the current limit. Then the output under-voltage or deep under-voltage protection would be triggered if the over-load condition continued.

Thermal Shutdown

The thermal shutdown protects the device from damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 155°C, the status bit **THWR[0]** will be set as a high temperature warning flag while the device keeps in normal operation. If the junction temperature continues to rise and exceeds 175°C,

thermal shutdown as a deep safe event will be triggered and the status bit **THSD[0]** will be set. The device will shut down all channels immediately and transit to DEEPSAFE state. After the hiccup timer expired, the device will try to restart if the over-temperature condition discontinued.

Status Bits

The SCT61242Q provides 6 status registers, **STATUS1~6**, to record all kinds of warnings, errors or faults during operation. Once being set, these status bits will not be reset until VCC under-voltage (e.g., VIN power off), or manually writing '1' to clear corresponding status bit via I2C. When GPIO2 is configured as INTB, any status bits being set will pull INTB low as an indicator to notify other devices. INTB level keeps latched after pulled low and only reset to high until all status bits are cleared. Some fault conditions could be masked for INTB through register **CTRL_FLTMAP2**.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliance, the SCT61242Q implements optional Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency in ±4/±8% range and 4k/8kHz period, with triangle, pseudorandom or hybrid modulation, which are configured in **FSS_PERIOD[0]**, **FSS_RANGE[0]** and **FSS_MODE[1:0]**. The FSS feature guarantees the switching frequency does not drop into 1.8MHz AM band limit.

Active Output Discharge

If any channel is disabled or shut off due to a deep safe event, there will be an active output discharge path at its output. To ensure all outputs are initiated before next power-up sequence, the discharge path will not be turned off until the output voltage drops below typical 250mV.

RESETB Indicator

The RESETB pin will assert when any reset event or deep safe event occurs. The RESETB output could be configured to be either open-drain or push-pull by **RESETB_OUT[0]**, and the high level of push-pull mode could be set to either 1.8V or 3.3V by **VIO[0]**, with an internal resistance of around 1kΩ. To avoid some reset events triggering RESETB, the device provides mask options in register **CTRL_FLTMAP1** and **CTRL_FLTMAP2**. A deep safe event will always pull RESETB low.

General Purpose I/O

The SCT61242Q is featured with two configurable GPIO pins for flexible system management. Each GPIO could be configured to a dedicated function pin as either input or output for different applications. GPIO1 can be configured to INTB or VMON. GPIO2 can be configured to SEQOUT, PG, GPO, INTB, ERRIN, WDI, SLEEPB and RSTIN. See Table 4 for a detailed description.

When configured as output, the two GPIOs could be set to be either open-drain or push-pull by **GPIO1_OUT[0]** and **GPIO2_OUT[0]**. The high level of push-pull mode could be set to either 1.8V or 3.3V by **VIO[0]**, with an internal resistance of around 1kΩ. The device could monitor the real-time output state of two GPIOs and report in register **STATUS5** if output gets stuck. When configured as input, GPIO2 has adjustable blanking time and deglitch time for both rising and falling edge. Fail-safe feature is also integrated to avoid any unexpected current sinking.

Table 4. GPIO Configuration

Pin	I/O	Function	Description
GPIO1	Input	VMON	External voltage monitor input. VMON can be used to monitor the external regulator output voltage with configurable activation timing. Any VMON OV/UV condition will trigger a reset event and VMON deep OVP/UVP will trigger a deep safe event. When used, VMON pin shall be connected directly to the external regulator without any resistor in between.
	Output	INTB	Interrupt output. INTB can be used as a fault indicator and pulled low when any fault condition in status registers triggered. INTB level keeps latched after pulled low and only reset to high until all status register bits are cleared. Some fault conditions could be masked for INTB through register **CTRL_FLTMAP2**.
GPIO2	Input	ERRIN	Logic input for power cycle. ERRIN can be used as an error injection pin. The device will be forced to transit to DEEPSAFE state and shut down all power rails once ERRIN pulled high.
		WDI	Watchdog input. WDI is used to feed the watchdog in simple mode and ignored in QA mode.
		SLEEPB	Sleep mode input. SLEEPB is used to enable the low-power sleep mode. The device will enter SLEEP state when **EN_LP[0]** set to 1 and SLEEPB pulled low, and exit SLEEP state once SLEEPB pulled high.
		RSTIN	Logic input for reset. RSTIN can be used as a reset event injection pin. The device will be forced to transit to RESET state and pulled RESETB pin low for the hold time once RSTIN pulled high.
	Output	SEQOUT	Sequential output for external enable. SEQOUT can be used to enable the external regulator with programmable power sequence and shut it down during deep safe event. SEQOUT function is only activated when GPIO1 is set to VMON.
		PG	Power good output. PG is the real-time power good indicator for all power rails. PG will be pulled high after power-up sequence done and pulled low once any UV/OV condition triggered.
		GPO	Register-based output. GPO output state is directly controlled by the register bit **CTRL_GPIO[0]**. GPO can be used as a logic output to interact with other device.
		INTB	Interrupt output. INTB can be used as a fault indicator and pulled low when any fault condition in status registers triggered. INTB level keeps latched after pulled low and only reset to high until all status register bits are cleared. Some fault conditions could be masked for INTB through register **CTRL_FLTMAP2**.

Watchdog

The SCT61242Q provides two kinds of watchdog operation mode, simple watchdog and Question and Answer (QA) watchdog.

In simple watchdog mode, watchdog is fed by trigger pulse to WDI(GPIO2) pin, or writing any byte to register **WD_KEY**. Once the device enters NORMAL state, the watchdog will be activated starting by close window and followed by open window, with extension cycles configured by **WD_1UD[0]**. The duration of close window and open window in each cycle could be configured by **WD_TCLOSE[3:0]** and **WD_TOPEN[3:0]**, and watchdog shall be fed only within open window. A correct watchdog feed action will restart the whole window cycle immediately. If watchdog fed during close window, status bit **WD_UV[0]** will be set, the watchdog error counter will be incremented and the window cycle will also be refreshed. Any feed action during the first close window after NORMAL state entered will be blanked. If watchdog not fed before open window expired, status bit **WD_EXP[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. When watchdog error counter reaches the times configured in **WD_FAIL_CNT[1:0]**, a reset event will be triggered and status bit **WD_ERR[0]** will be set. The device transits to RESET state and goes back to NORMAL state after a hold time. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET back to NORMAL state.

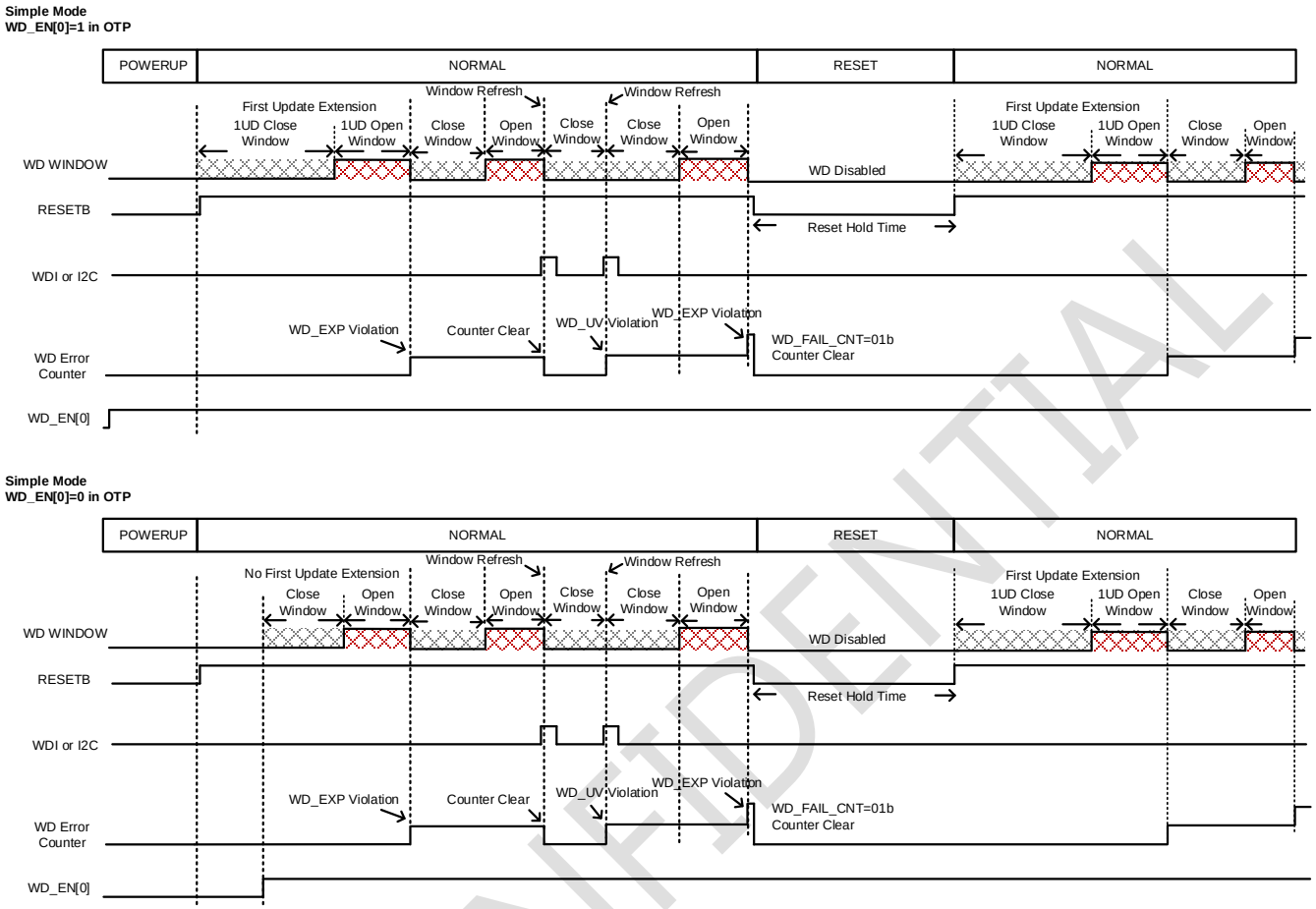


Figure 15. Simple Watchdog Operation and Timing

In QA watchdog mode, watchdog is fed by writing specific value to register **WD_KEY** and the operation is similar to simple watchdog mode. Once the device enters NORMAL state, the watchdog will be activated starting by close window and followed by open window, with extension cycles configured by **WD_1UD[0]**. The duration of close window and open window in each cycle could be configured by **WD_TCLOSE[3:0]** and **WD_TOPEN[3:0]**, and watchdog shall be fed only within open window. The correct value written to register **WD_KEY** shall be the same as the current value in **WD_KEY**, which can also be calculated with the previous value in **WD_KEY** by a LFSR polynomial of x8 + x6 + x5 + x4 + 1. A correct watchdog feed action will restart the whole window cycle immediately. If an incorrect value is written, status bit **WD_LFSR[0]** will be set, the watchdog error counter will be incremented and the window cycle will also be refreshed. If watchdog fed during close window, status bit **WD_UV[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. Any feed action during the first close window after NORMAL state entered will be blanked. If watchdog not fed before open window expired, status bit **WD_EXP[0]** will be set, the watchdog error counter will be incremented and the window cycle will be refreshed. When watchdog error counter reaches the times configured in **WD_FAIL_CNT[1:0]**, a reset event will be triggered and status bit **WD_ERR[0]** will be set. The device transits to RESET state and goes back to NORMAL state after a hold time. The watchdog error counter is reset and watchdog window cycle is initiated when transiting from RESET back to NORMAL state.

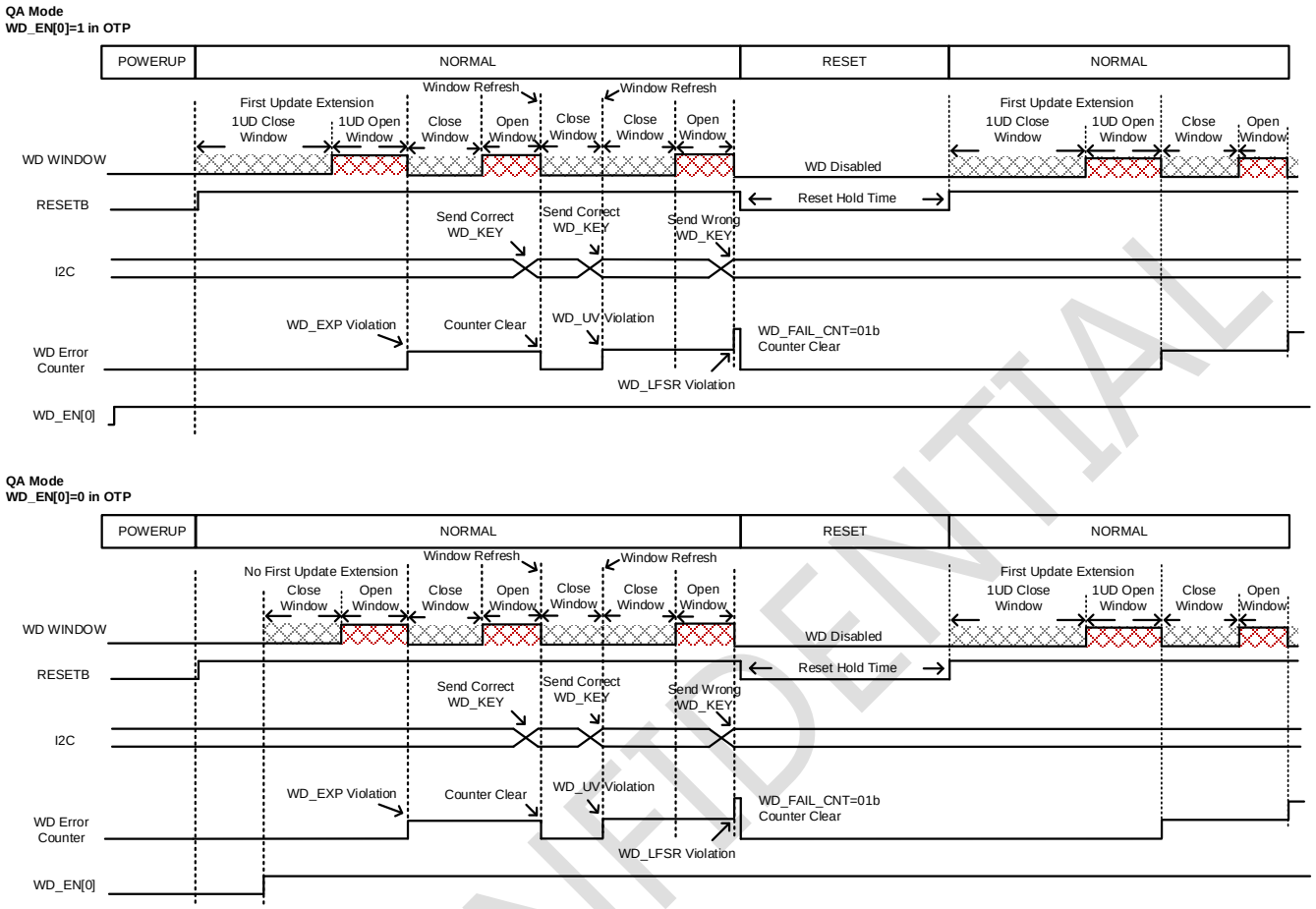


Figure 16. QA Watchdog Operation and Timing

Table 5. Watchdog Feed Response

Mode	Feed Action	Feed Timing	Window Refresh	Error Counter	Status Bit
Simple	WDI pulse or any writing to **WD_KEY** register	1st close window	No	No change	\
		Other close window	Yes	+1	**WD_UV[0]** is set
		Open window	Yes	Clear	\
QA	Writing correct key to **WD_KEY** register	1st close window	No	No change	\
		Other close window	Yes	+1	**WD_UV[0]** is set
		Open window	Yes	Clear	\
	Writing incorrect key to **WD_KEY** register	1st close window	No	No change	\
		Other close window	Yes	+1	**WD_LFSR[0]** and **WD_UV[0]** are set
		Open window	Yes	+1	**WD_LFSR[0]** is set

I2C Interface

The SCT61242Q integrates a two-wire serial interface for bidirectional communications between the device and the master through the bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61242Q is assigned with a unique chip address 0x38 by default and operates as a slaver. The master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and the SDA lines need a pull-up resistor connected to bus voltage since high state is the default state when bus is idle. The SCT61242Q supports Standard mode (up to 100kHz), Fast-mode (up to 400kHz) and Fast-mode Plus (up to 1MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of Interfaces is limited.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

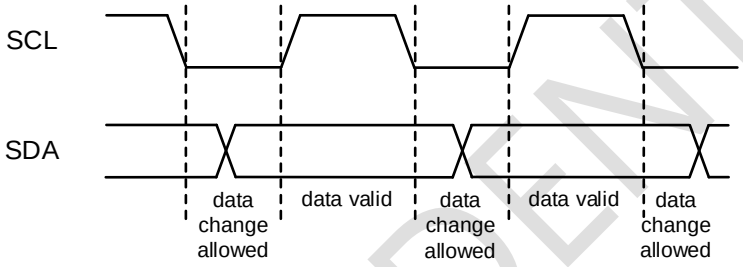


Figure 17. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A high to low transition on the SDA line while SCL is high defines a START condition. A low to high transition on the SDA line while SCL is high defines a STOP condition. Both the START and STOP conditions are generated by the master on the bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

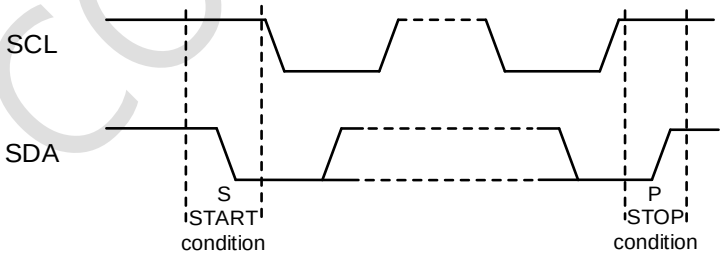


Figure 18. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61242Q will pull the SDA line low during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled low. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command.

Packet Error Checking (PEC)

The SCT61242Q supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated with the register address and data byte over the entire message from the first START condition. Note that the slave address is not involved in the calculation both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. PEC function can be enabled or disabled by **PEC_EN[0]**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 19 illustrates the proper format for one frame.

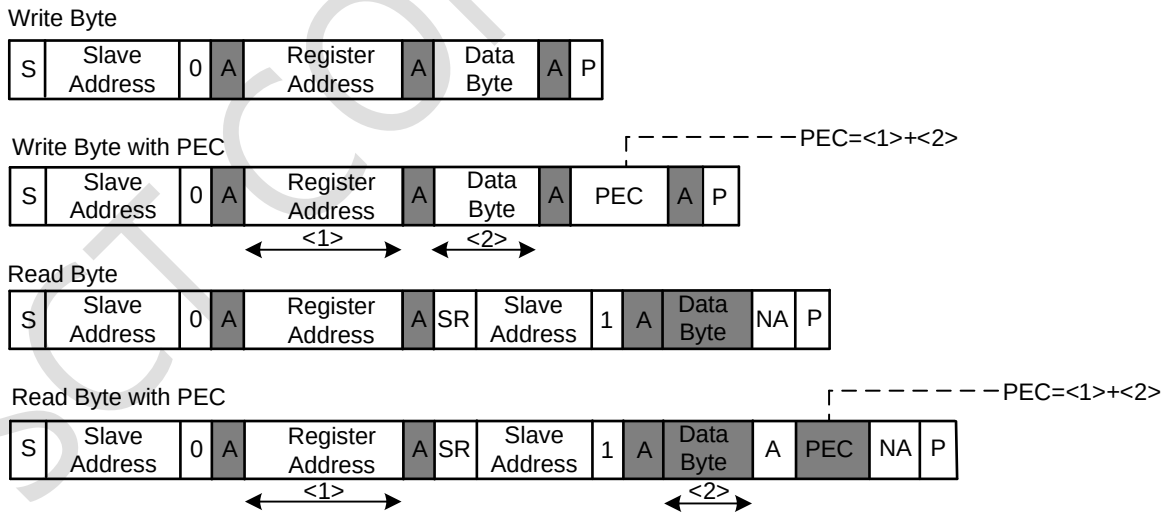


Figure 19. Transmission Data Format

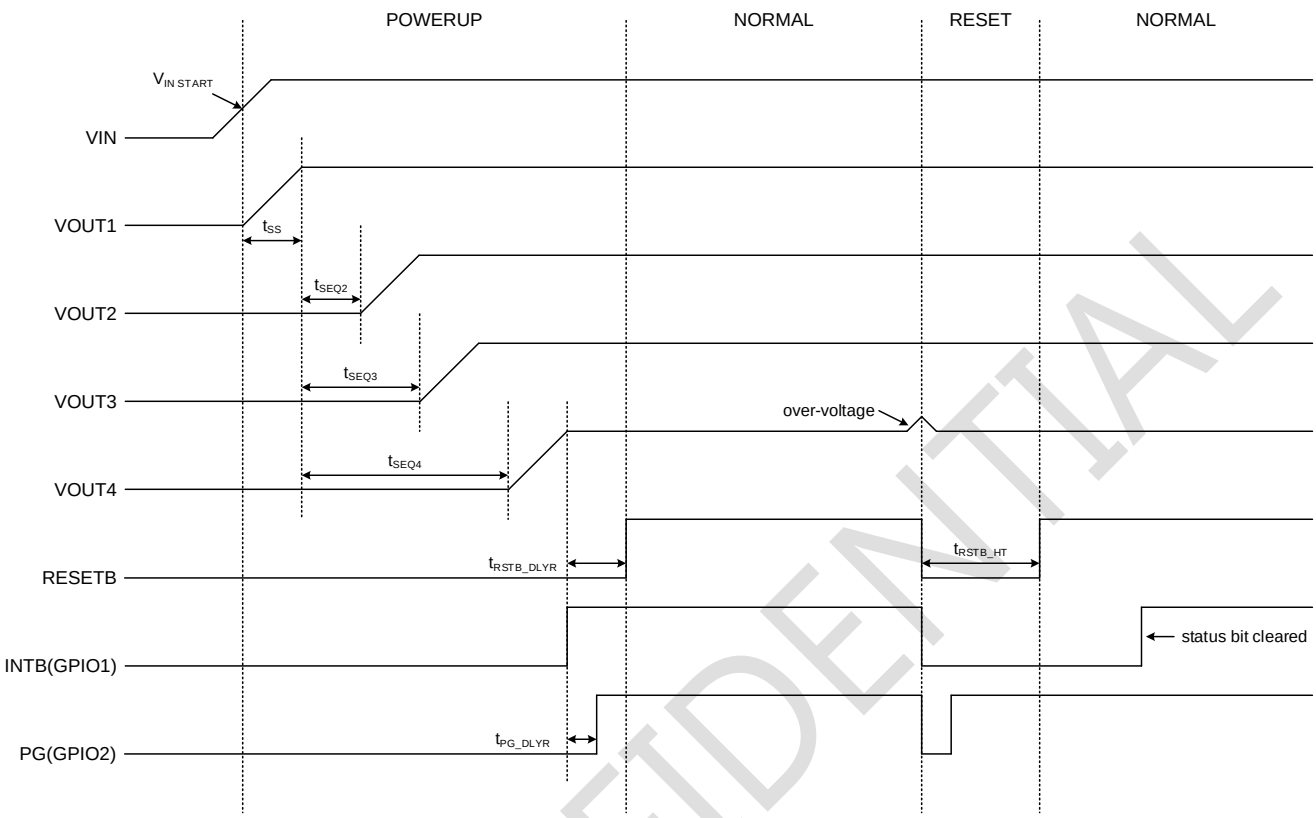


Figure 20. Power Up Sequence

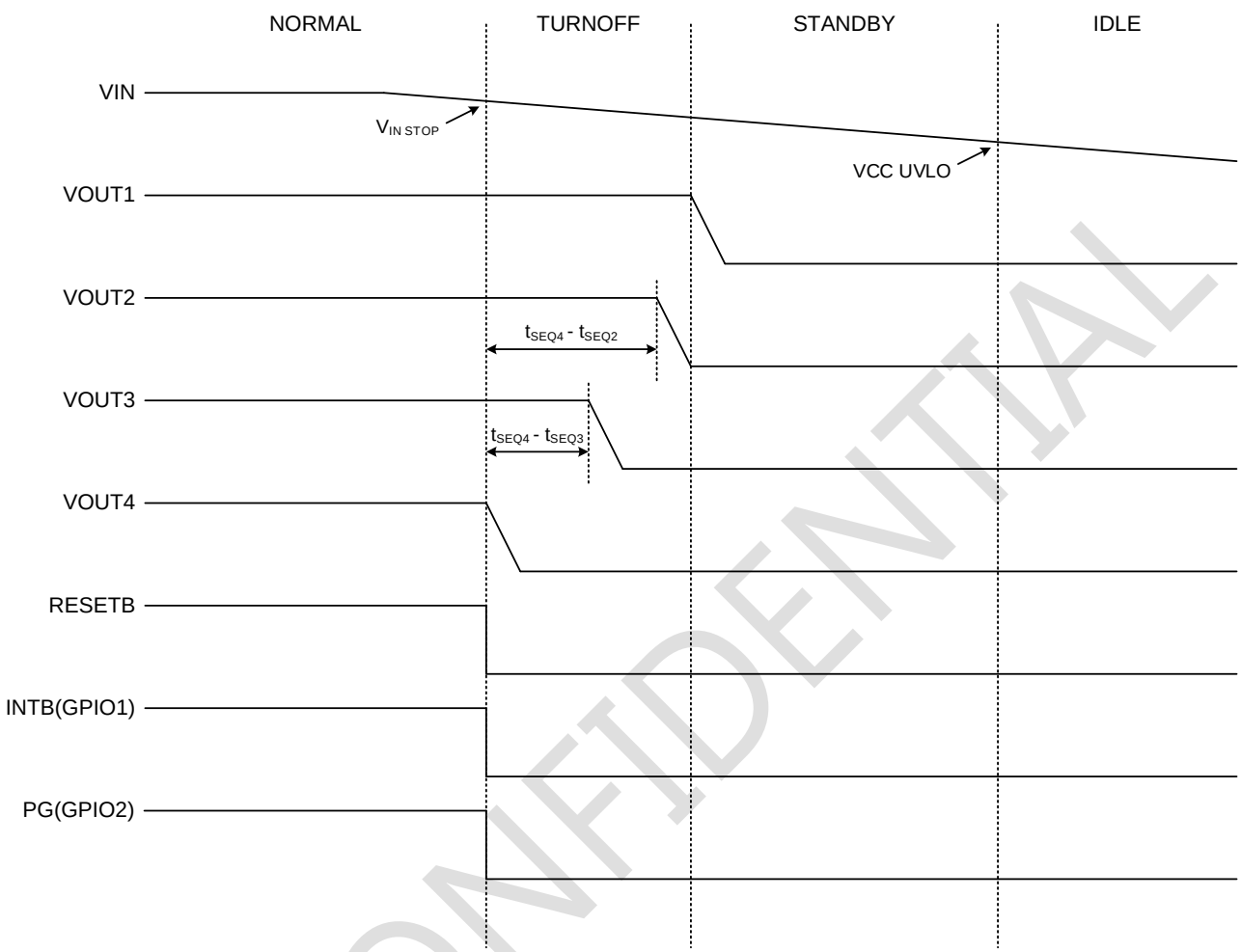


Figure 21. Power Down Sequence

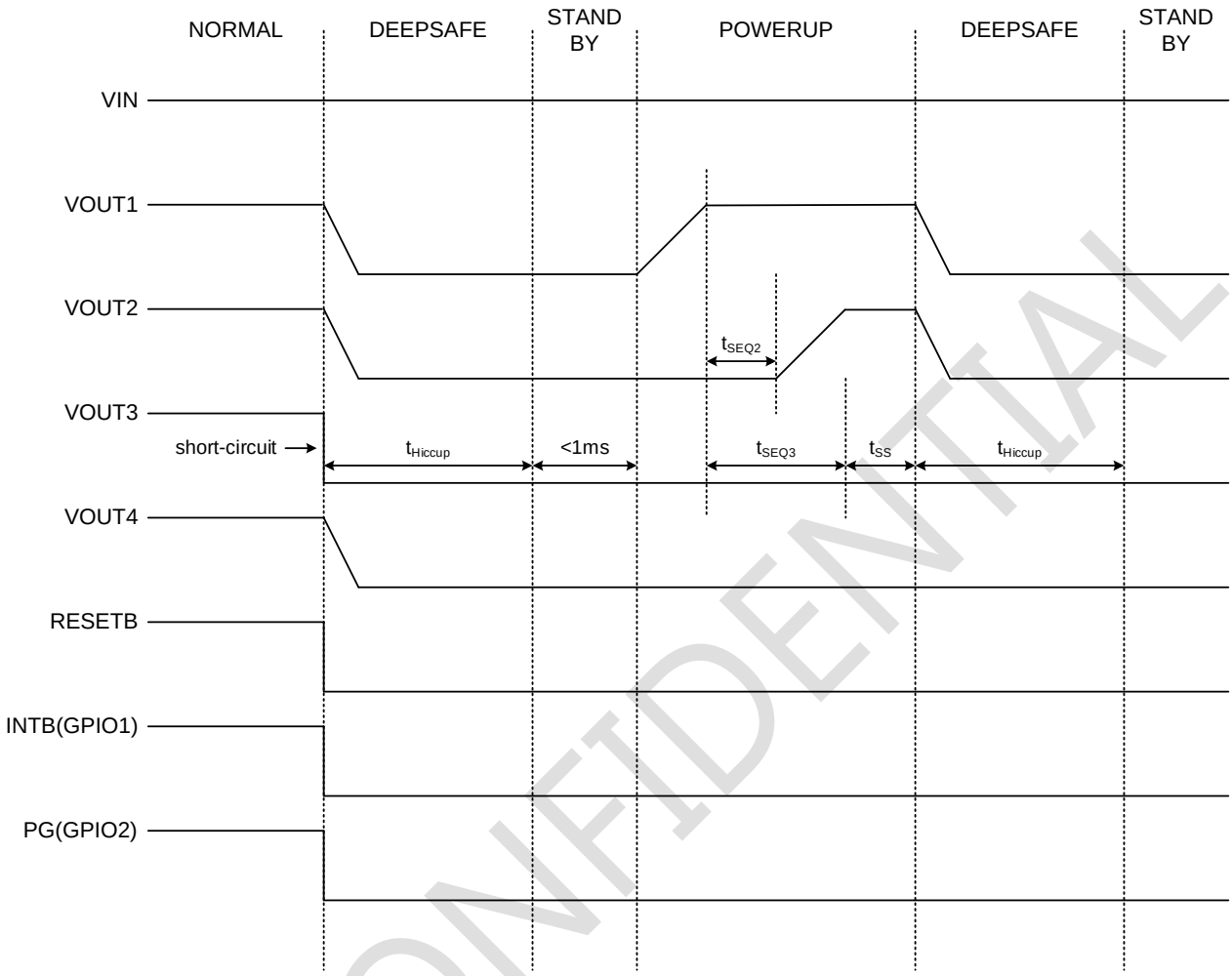


Figure 22. Deep Safe Event

APPLICATION INFORMATION

Typical Application

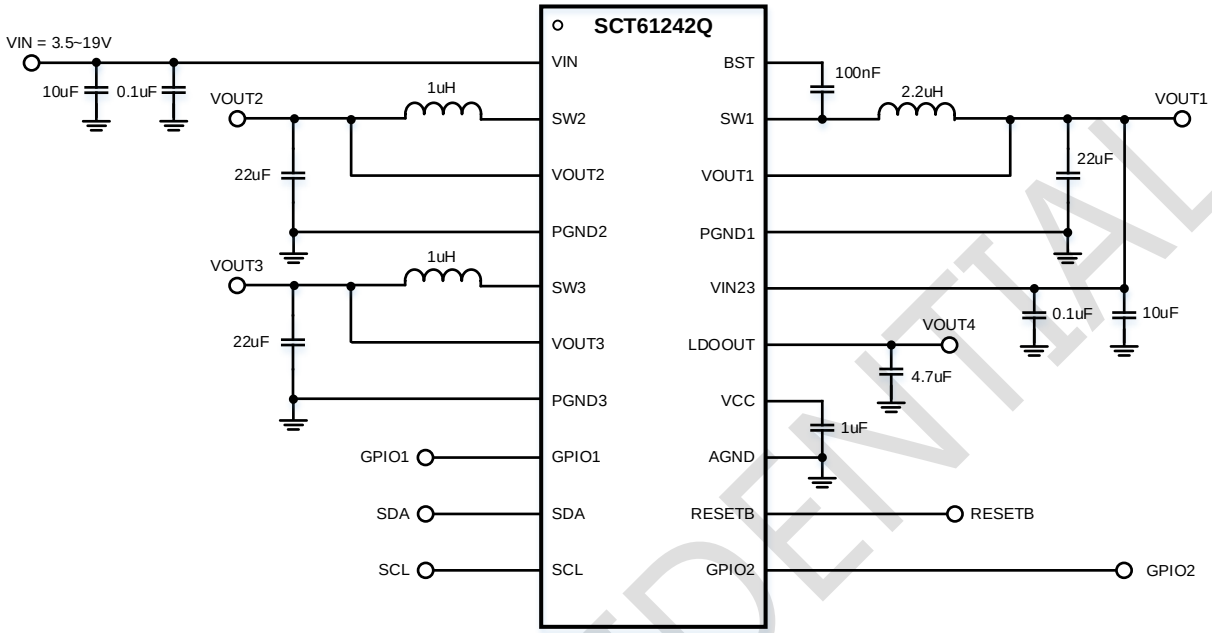


Figure 23. Application Schematic, 3.5V to 19V Input

Design Parameters	Example Value
Input Voltage	Nominal 10V
Output Voltage	Buck1: 3.3V Buck2: 1.8V Buck3: 1.2V LDO4: 2.8V
Maximum Output Current	Buck1: 2A Buck2: 2A Buck3: 2A LDO4: 300mA
Switching Frequency	2.2MHz
Output Voltage Ripple (Peak-to-Peak)	Buck1: <10mV Buck2: <5mV Buck3: <5mV

The SCT61242Q is featured with minimized external components and all feedback divider, pull-up or configuration resistor could be saved. For typical application, the recommended inductance and capacitance for each power rail are listed in Table 6. Higher inductance and capacitance for lower output ripple are also acceptable.

Table 6. Recommended BOM for Typical Application

Output Rail	Switching Frequency	Inductor	Output Capacitor
Buck1	2.2MHz	2.2uH	10uF or 22uF
Buck2	2.2MHz	1uH	10uF or 22uF
Buck3	2.2MHz	1uH	10uF or 22uF
LDO4	-	-	4.7uF

Application Waveforms

V_{IN} = 10V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{OUT4} = 2.8V, L1 = 2.2uH, L2 = L3 = 1uH, FCCM, T_A = 25°C, unless otherwise noted.

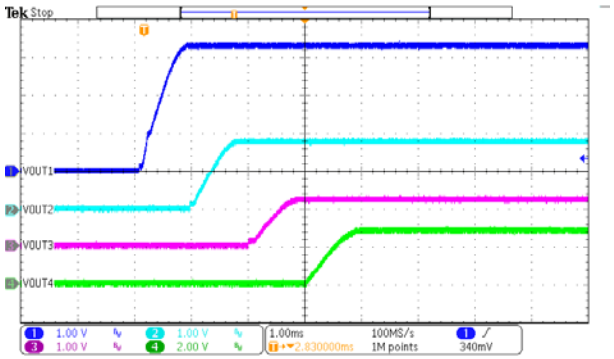


Figure 24. Power Up Sequence

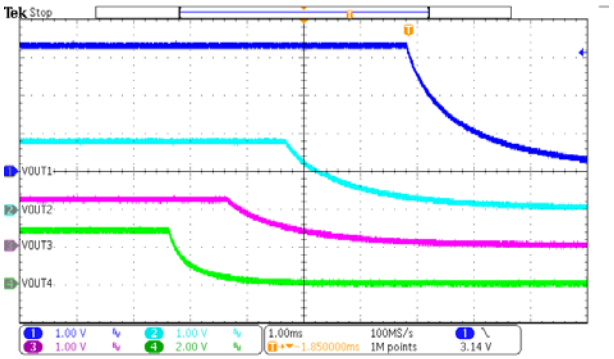


Figure 25. Power Down Sequence

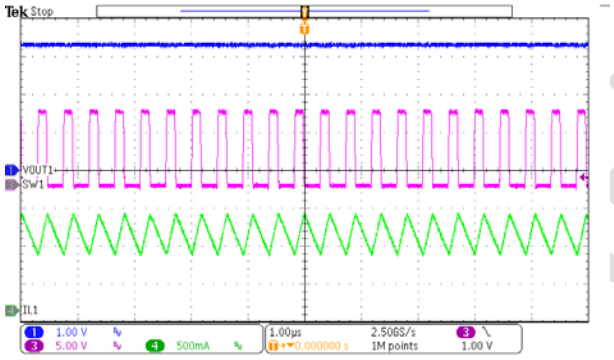


Figure 26. Buck1 Steady State, Load=1A

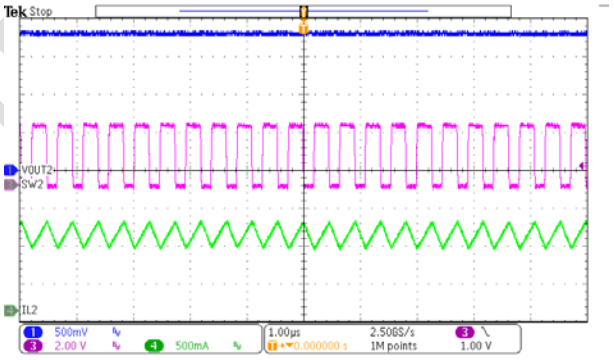


Figure 27. Buck2 Steady State, Load=1A

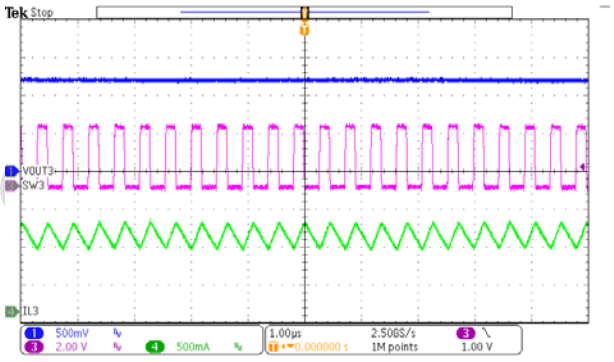


Figure 28. Buck3 Steady State, Load=1A

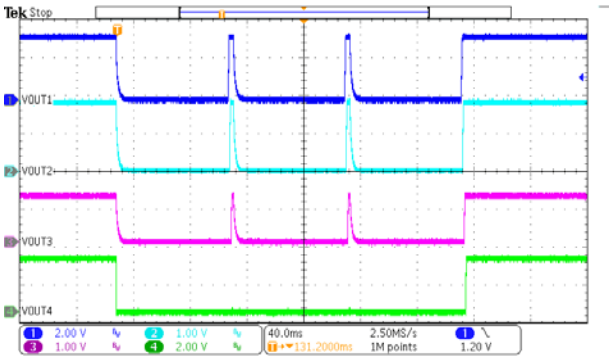


Figure 29. LDO4 Short-circuit and Recovery

Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over-heat area.
2. Place a low ESR ceramic capacitor as close to VIN and VIN23 pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. Connect AGND to PGND plane at a single point.

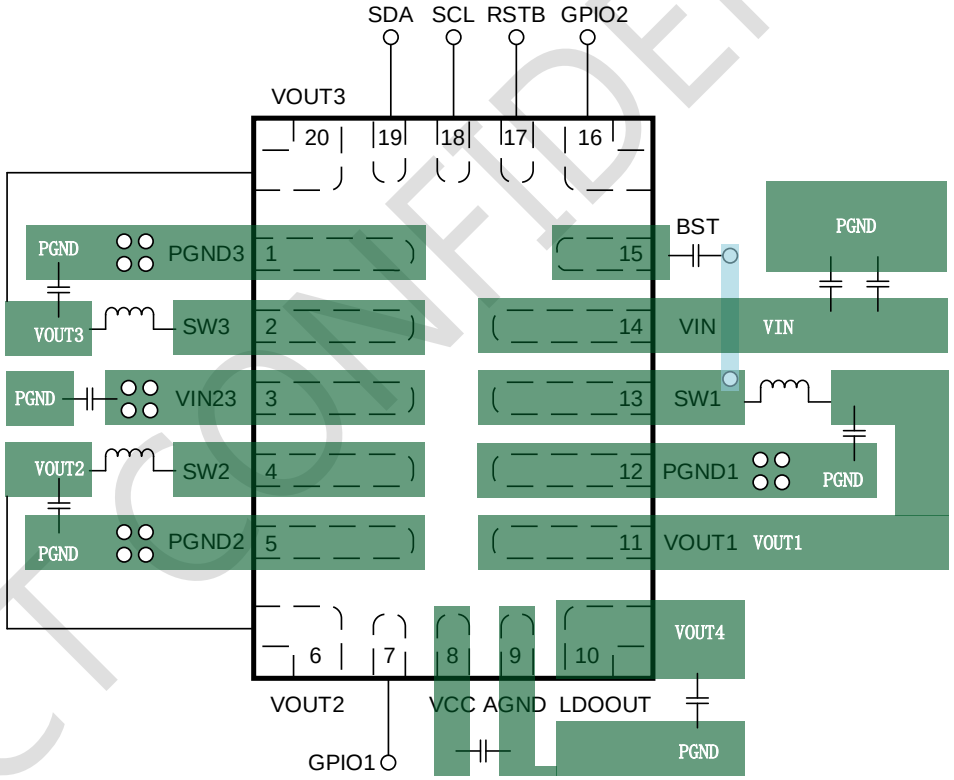


Figure 30. PCB Layout Example

REGISTER MAP

ADDRESS	REGISTER	DEFAULT VALUE	OTP ACCESS	I2C WRITE LOCK
0x00	CHIPID	-	Y	-
0x01	CTRL_EN	-	Y	Y
0x02	CTRL_ENLP	-	Y	Y
0x03	CONFIG_SYSTEM	-	Y	-
0x04	CONFIG_BUCK1	-	Y	-
0x05	CONFIG_BUCK2	-	Y	-
0x06	CONFIG_BUCK3	-	Y	-
0x07	CONFIG_LDO4	-	Y	-
0x08	CONFIG_VMON	-	Y	-
0x09	CONFIG_MISC	-	Y	-
0x0A	CONFIG_T1	-	Y	-
0x0B	CONFIG_T2	-	Y	-
0x0C	CONFIG_SEQ45	-	Y	-
0x0D	CONFIG_SEQ23	-	Y	-
0x0E	CONFIG_WD1	-	Y	N
0x0F	CONFIG_WD2	-	Y	N
0x10	CONFIG_WD3	-	Y	N
0x11	WD_KEY	-	N	N
0x12	WD_LOCK	-	N	N
0x13	CONFIG_GPIO0	-	Y	-
0x14	CONFIG_GPIO1	-	Y	-
0x15	CTRL_GPO	-	N	Y
0x16	CONFIG_FLTMAP1	-	Y	Y
0x17	CONFIG_FLTMAP2	-	Y	Y
0x18	STATUS1	-	N	N
0x19	STATUS2	-	N	N
0x1A	STATUS3	-	N	N
0x1B	STATUS4	-	N	N
0x1C	STATUS5	-	N	N
0x1D	STATUS6	-	N	N
0x1E	STATE	-	N	N
0xE0	I2C_LOCK	-	N	N
0xE1	CTRL_RESTART	-	N	Y

REGISTER DESCRIPTION

CHIPID [7:0]			
ADDRESS: 0x00			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	CONFIG_ID	R	Chip Configuration Identification. This is a unique number identifying the factory configuration of the device. This helps identify/verify the configuration without having to look at all configuration registers.

CTRL_EN [7:0]			
ADDRESS: 0x01			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PEC_EN	W/R	Packet Error Checking Enable. Set this bit to 1 to enable PEC or 0 to disable PEC. 0: Disabled 1: Enabled
[6:5]	RESERVED	R	/
[4]	EN5	W/R	Enable for external channel when GPIO2 is set to SEQOUT. This bit is only activated when GPIO1 set to VMON. 0: Disabled 1: Enabled
[3]	EN4	W/R	Enable for LDO4. 0: Disabled 1: Enabled
[2]	EN3	W/R	Enable for LV Buck3. 0: Disabled 1: Enabled
[1]	EN2	W/R	Enable for LV Buck2. 0: Disabled 1: Enabled
[0]	EN_ALL	W/R	Enable for all channels. 0: Disabled 1: Enabled

CTRL_ENLP [7:0]			
ADDRESS: 0x02			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	RESERVED	R	/
[3]	OFF4_LP	W/R	LDO4 control for low power mode. 0: LDO4 will stay alive in low power mode. 1: LDO4 will be turned off in low power mode.
[2]	OFF3_LP	W/R	LV Buck3 control for low power mode. 0: LV Buck3 will stay alive in low power mode. 1: LV Buck3 will be turned off in low power mode.
[1]	OFF2_LP	W/R	LV Buck2 control for low power mode. 0: LV Buck2 will stay alive in low power mode. 1: LV Buck2 will be turned off in low power mode.
[0]	EN_LP	W/R	Enable for low power mode. This bit will be self-cleared when exiting SLEEP state and is only activated when GPIO2 set to SLEEPB. 0: Disabled 1: Enabled

CONFIG_SYSTEM [7:0]			
ADDRESS: 0x03			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	FSS_PERIOD	R	Frequency spread spectrum period. 0: 4kHz 1: 8kHz
[6]	FSS_RANGE	R	Frequency spread spectrum range. 0: ±8% 1: ±4%
[5:4]	FSS_MODE	R	Frequency spread spectrum mode/enable. 00: Disable 01: Triangle Modulation 10: Pseudorandom Modulation 11: Triangle and Pseudorandom Modulation
[3:2]	VIN_START	R	VIN rising threshold to initiate power up sequence. 00: 3.2V 01: 4V 10: 5V 11: 6V
[1:0]	VIN_STOP	R	VIN falling threshold to initiate power down sequence. 00: 2.8V 01: 3.5V 10: 4.5V 11: 5.5V

CONFIG_BUCK1 [7:0]			
ADDRESS: 0x04			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM1	R	Buck1 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:4]	RESERVED	R	/
[3:0]	VOUT1	R	Buck1 output voltage setting. 0000: 2.7V 0001: 2.8V 0010: 2.9V 0011: 3.0V 0100: 3.1V 0101: 3.2V 0110: 3.3V 0111: 3.4V 1000: 3.5V 1001: 3.6V 1010: 3.7V 1011: 3.8V 1100: 3.9V 1101: 4V 1110: 4.5V 1111: 5V

CONFIG_BUCK2 [7:0]			
ADDRESS: 0x05			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM2	R	Buck2 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:5]	RESERVED	R	/
[4:0]	VOUT2	R	Buck2 output voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 01100: 1.2V … 11000: 1.8V … 11110: 2.1V 11111: 2.15V (V_{OUT2} = 0.6V + VOUT2[4:0] × 0.05V)

CONFIG_BUCK3 [7:0]			
ADDRESS: 0x06			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	PSM3	R	Buck3 FCCM/PSM mode selection in NORMAL state. 0: FCCM 1: PSM
[6:5]	RESERVED	R	/
[4:0]	VOUT3	R	Buck3 output voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 01100: 1.2V … 11000: 1.8V … 11110: 2.1V 11111: 2.15V (V_{OUT3} = 0.6V + VOUT3[4:0] × 0.05V)

CONFIG_LDO4 [7:0]			
ADDRESS: 0x07			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:5]	RESERVED	R	/
[4:0]	VOUT4	R	LDO4 output voltage setting. 00000: 1.6V 00001: 1.65V 00010: 1.7V … 01001: 2.05V 01010: 2.1V (50mV step from 1.6V to 2.1V, V_{OUT4} = 1.6V + VOUT4[4:0] × 0.05V) 01011: 2.5V 01100: 2.55V … 10001: 2.8V … 11011: 3.3V … 11110: 3.45V 11111: 3.5V (50mV step from 2.5V to 3.5V, V_{OUT4} = 2.5V + VOUT4[4:0] × 0.05V)

CONFIG_VMON [7:0]			
ADDRESS: 0x08			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:5]	RESERVED	R	/
[4:0]	VMON	R	VMON monitor voltage setting. 00000: 0.6V 00001: 0.65V 00010: 0.7V … 11110: 2.1V 11111: 2.15V (V_{MON} = 0.6V + VMON[4:0] × 0.05V)

CONFIG_MISC [7:0]			
ADDRESS: 0x09			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	DEEP_OVP_SEL	R	Deep OVP threshold selection for all channels. 00: 115% 01: 112% 10: 110% 11: 108%
[5:4]	DEEP_UVP_SEL	R	Deep UVP threshold selection for all channels. 00: 75% 01: 80% 10: 85% 11: 90%
[3]	VINOVP_DEEPSAFE_CTRL	R	VIN OVP action selection. 0: Enter DEEPSAFE state 1: Enter RESET state
[2]	VMON_DEEPSAFE_CTRL	R	VMON deep OVP/UVP action selection. 0: Enter DEEPSAFE state 1: Enter RESET state
[1:0]	VMON_BLANK	R	VMON monitor blanking time. VMON pin will be monitored after this blanking time since SEQOUT pulled high. If SEQOUT is not used, the blanking time starts from SEQ5[3:0] configured timing. 00: 1ms 01: 2ms 10: 4ms 11: 8ms

CONFIG_T1 [7:0]			
ADDRESS: 0x0A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESETB_HT	R	RESETB assertion low-level hold time. The RESETB pin is pulled low at least for this duration when any reset event triggered. After the hold time expired, NORMAL state will be entered if the reset event discontinued. 00: 10ms 01: 20ms 10: 30ms 11: 40ms
[5:4]	RESETB_DLYR	R	RESETB rising delay time after all channels are built up in POWERUP state. When RESETB_DLYR_SCALE[0]=0: 00: 0.5ms 01: 1ms 10: 2ms 11: 4ms When RESETB_DLYR_SCALE[0]=1: 00: 2.5ms 01: 5ms 10: 10ms 11: 20ms
[3:2]	PG_DLYR	R	PG rising delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us
[1:0]	PG_DLYF	R	PG falling delay time when GPIO2 is set to PG. 00: 50us 01: 100us 10: 150us 11: 200us

CONFIG_T2 [7:0]			
ADDRESS: 0x0B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	ON_DELAY_SCALE	R	Power up sequence on delay time scale selection. 00: t_{ON_SCALE} = 0.5ms (0~7.5ms range) 01: t_{ON_SCALE} = 1ms (0~15ms range) 10: t_{ON_SCALE} = 2ms (0~30ms range) 11: t_{ON_SCALE} = 4ms (0~60ms range)
[5:4]	OFF_DELAY_SCALE	R	Power down sequence off delay time scale selection. 00: t_{OFF_SCALE} = 0.5ms (0~7.5ms range) 01: t_{OFF_SCALE} = 1ms (0~15ms range) 10: t_{OFF_SCALE} = 2ms (0~30ms range) 11: t_{OFF_SCALE} = 4ms (0~60ms range)
[3:0]	OVUV_FILTER_TIME	R	OV rising/UV falling filter time for all output comparators. t_{FILT} = (OVUV_FILTER_TIME[3:0] + 1) × 10us

CONFIG_SEQ45 [7:0]			
ADDRESS: 0x0C			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	SEQ5	R	SEQOUT rising delay time configuration after Buck1 output built in power up sequence. VMON blanking time is initiated after this delay time. It also configures SEQOUT falling delay time. t_{ON_SEQ5} = SEQ5[3:0] × t_{ON_SCALE} t_{OFF_SEQ5} = SEQ5[3:0] × t_{OFF_SCALE}
[3:0]	SEQ4	R	LDO4 turn-on delay time configuration after Buck1 output built in power up sequence. It also configures LDO4 turn-off delay time. See Figure 20 and Figure 21 for details. t_{ON_SEQ4} = SEQ4[3:0] × t_{ON_SCALE} t_{OFF_SEQ4} = SEQ4[3:0] × t_{OFF_SCALE}

CONFIG_SEQ23 [7:0]			
ADDRESS: 0x0D			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	SEQ3	R	Buck3 turn-on delay time configuration after Buck1 output built in power up sequence. It also configures Buck3 turn-off delay time. See Figure 20 and Figure 21 for details. t_{ON_SEQ3} = SEQ3[3:0] × t_{ON_SCALE} t_{OFF_SEQ3} = SEQ3[3:0] × t_{OFF_SCALE}
[3:0]	SEQ2	R	Buck2 turn-on delay time configuration after Buck1 output built in power up sequence. It also configures Buck2 turn-off delay time. See Figure 20 and Figure 21 for details. t_{ON_SEQ2} = SEQ2[3:0] × t_{ON_SCALE} t_{OFF_SEQ2} = SEQ2[3:0] × t_{OFF_SCALE}

CONFIG_WD1 [7:0]			
ADDRESS: 0x0E			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	WD_MODE	W/R	Watchdog mode selection. 0: QA watchdog 1: Simple watchdog
[6]	WD_SCALE	W/R	Watchdog clock divider scale. 0: t_{WDCLK_SCALE} = 128us 1: t_{WDCLK_SCALE} = 8192us
[5:0]	WD_CLK	W/R	Watchdog clock divider. t_{WDCLK} = (WD_CLK[5:0] + 1) × t_{WDCLK_SCALE}

CONFIG_WD2 [7:0]			
ADDRESS: 0x0F			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:4]	WD_TCLOSE	W/R	Watchdog close window duration time configuration. Feeding watchdog in close window will trigger a WD_UV violation and increase watchdog error counter by 1. t_{WD_CLOSE} = (WD_TCLOSE[3:0] + 1) × 8 × t_{WDCLK}
[3:0]	WD_TOPEN	W/R	Watchdog open window duration time configuration. Feeding watchdog correctly in open window will restart the whole window cycle immediately. t_{WD_OPEN} = (WD_TOPEN[3:0] + 1) × 8 × t_{WDCLK}

CONFIG_WD3 [7:0]			
ADDRESS: 0x10			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:6]	RESERVED	R	/
[5:4]	WD_FAIL_CNT	W/R	Watchdog error counting times configuration. When watchdog error counter reaches this number, a RESET event will be triggered. 00: 1 time 01: 2 times 10: 3 times 11: 4 times
[3]	WD_EN	W/R	Watchdog enable. 0: Disabled 1: Enabled
[2:0]	WD_1UD	W/R	Watchdog first update extension. This configures the extra length of the first open/close window after entering NORMAL state. $t_{WD\_CLOSE\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_CLOSE} $t_{WD\_OPEN\_1st}$ = (WD_1UD[2:0] + 1) × t_{WD_OPEN}

WD_KEY [7:0]			
ADDRESS: 0x11			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_KEY	W/R	Watchdog key. The current key can be read from this register and the next key will be updated after the current key written to this register by user. For simple watchdog, writing any value to the WD_KEY register will refresh the watchdog and the value written will be ignored. For QA watchdog, writing the correct value to the WD_KEY register during an open window will result in a window refresh and the WD_KEY register being updated. Writing the incorrect value to the WD_KEY register during an open window will result in a WD_LFSR violation. Writing any value during a closed window will result in a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]			
ADDRESS: 0x12			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	WD_LOCK	W/R	Watchdog configuration lock protection. AAh: Watchdog configuration registers (CONFIG_WD1/2/3) are writeable. Others: Watchdog configuration registers (CONFIG_WD1/2/3) are read-only.

CONFIG_GPIO0 [7:0]			
ADDRESS: 0x13			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESETB_DLYR_SCALE	R	RESETB rising delay time scale selection. 0: t_{RST_SCALE} = 0.5ms (0.5~4ms range) 1: t_{RST_SCALE} = 2.5ms (2.5~20ms range)
[6]	RESERVED	R	/
[5:4]	GPIO2_BLANK	R	GPIO2 input signal blanking time after RESETB pulled high. 00: 0ms 01: 2.5ms 10: 5ms 11: 10ms
[3:2]	GPIO2_DLYR	R	GPIO2 input signal rising deglitch time. 00: 80us 01: 40us 10: 20us 11: 10us
[1:0]	GPIO2_DLYF	R	GPIO2 input signal falling deglitch time. 00: 80us 01: 40us 10: 20us 11: 10us

CONFIG_GPIO1 [7:0]			
ADDRESS: 0x14			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	VIO	R	High level voltage selection when RESETB/GPIO1/GPIO2 configured as push-pull output. 0: 3.3V 1: 1.8V
[6]	RESETB_OUT	R	RESETB output configuration. 0: Open-drain 1: Push-pull
[5]	GPIO1_OUT	R	GPIO1 output configuration. 0: Open-drain 1: Push-pull
[4]	GPIO2_OUT	R	GPIO2 output configuration. 0: Open-drain 1: Push-pull
[3]	GPIO1_SEL	R	GPIO1 function selection. 0: INTB (output) 1: VMON (analog input)
[2:0]	GPIO2_SEL	R	GPIO2 function selection. 000: SEQOUT (output) 001: PG (output) 010: GPO (output) 011: INTB (output) 100: ERRIN (digital input) 101: WDI (digital input) 110: SLEEPB (digital input) 111: RSTIN (digital input)

CTRL_GPO [7:0]			
ADDRESS: 0x15			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:1]	RESERVED	R	/
[0]	CTRL_GPIO	W/R	GPIO2 output state when GPIO2 configured as GPO. 0: Low 1: High

CTRL_FLTMAP1 [7:0]			
ADDRESS: 0x16			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RSTMAP_I2C	W/R	Reset event and RESETB pin mapping for I2C PEC error. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[6]	RSTMAP_VINOVP	W/R	Reset event and RESETB pin mapping for VIN OVP. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[5]	RSTMAP_VMON	W/R	Reset event and RESETB pin mapping for VMON OV and UV. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[4]	RSTMAP_VO4	W/R	Reset event and RESETB pin mapping for VOUT4 OV and UV. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[3]	RSTMAP_VO3	W/R	Reset event and RESETB pin mapping for VOUT3 OV and UV. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[2]	RSTMAP_VO2	W/R	Reset event and RESETB pin mapping for VOUT2 OV and UV. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[1]	RSTMAP_VO1	W/R	Reset event and RESETB pin mapping for VOUT1 OV and UV. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[0]	RSTMAP_WD	W/R	Reset event and RESETB pin mapping for watchdog error. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin

CTRL_FLTMAP2 [7:0]			
ADDRESS: 0x17			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RSTMAP_RSTIN	W/R	Reset event and RESETB pin mapping for RSTIN. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[6]	RSTMAP_VMONDP	W/R	Reset event and RESETB pin mapping for VMON deep OVP/UVP when VMON_DEEPSAFE_CTRL[0]=1. 0: Not mapped to reset event and RESETB pin 1: Mapped to reset event and RESETB pin
[5]	RESERVED	R	/
[4]	INTBMAP_I2C	W/R	INTB pin mapping for I2C PEC error. 0: Not mapped to INTB pin 1: Mapped to INTB pin
[3]	INTBMAP_THWR	W/R	INTB pin mapping for thermal warning. 0: Not mapped to INTB pin 1: Mapped to INTB pin
[2]	RESERVED	R	/
[1]	INTBMAP_WD	W/R	INTB pin mapping for watchdog error (WD_ERR, WD_LFSR, WD_UV, WD_EXP). 0: Not mapped to INTB pin 1: Mapped to INTB pin
[0]	STATEMAP_ERRIN	W/R	State machine mapping for ERRIN. 0: Not mapped to state machine 1: Mapped to state machine

STATUS1 [7:0]			
ADDRESS: 0x18			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	UV5	W1C/R	VMON under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	UV4	W1C/R	LDO4 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	UV3	W1C/R	Buck3 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	UV2	W1C/R	Buck2 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	UV1	W1C/R	Buck1 output under-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OV5	W1C/R	VMON over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	OV4	W1C/R	LDO4 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	OV3	W1C/R	Buck3 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS2 [7:0]			
ADDRESS: 0x19			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	OV2	W1C/R	Buck2 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	OV1	W1C/R	Buck1 output over-voltage status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	OC4	W1C/R	LDO4 over-current status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	OC3	W1C/R	Buck3 over-current status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	OC2	W1C/R	Buck2 over-current status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	OC1	W1C/R	Buck1 over-current status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	DEEPUVP5	W1C/R	VMON deep under-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	DEEPUVP4	W1C/R	LDO4 deep under-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS3 [7:0]			
ADDRESS: 0x1A			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	DEEPUVP3	W1C/R	Buck3 deep under-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	DEEPUVP2	W1C/R	Buck2 deep under-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	DEEPUVP1	W1C/R	Buck1 deep under-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	DEEPOVP5	W1C/R	VMON deep over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	DEEPOVP4	W1C/R	LDO4 deep over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	DEEPOVP3	W1C/R	Buck3 deep over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	DEEPOVP2	W1C/R	Buck2 deep over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	DEEPOVP1	W1C/R	Buck1 deep over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATUS4 [7:0]			
ADDRESS: 0x1B			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESERVED	R	/
[6]	VCC_OVP	W1C/R	VCC over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5:0]	RESERVED	R	/

STATUS5 [7:0]			
ADDRESS: 0x1C			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:3]	RESERVED	R	/
[2]	THSD	W1C/R	Thermal shutdown status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	THWR	W1C/R	Thermal warning status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	RESERVED	R	/

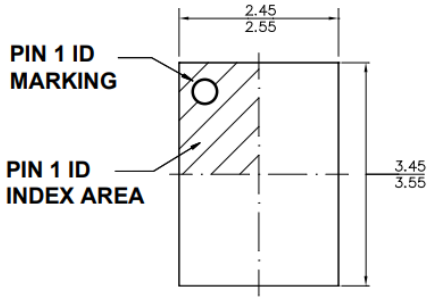
STATUS6 [7:0]			
ADDRESS: 0x1D			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	WD_ERR	W1C/R	Watchdog error (counter reached) status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[6]	WD_LFSR	W1C/R	Watchdog LFSR write mismatch status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[5]	WD_UV	W1C/R	Watchdog update violation status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[4]	WD_EXP	W1C/R	Watchdog open window expired status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[3]	ERRIN	W1C/R	ERRIN input status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[2]	RSTIN	W1C/R	RSTIN input status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[1]	I2C_PEC_ERR	W1C/R	I2C PEC error status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.
[0]	VIN_OVP	W1C/R	VIN over-voltage protection status. Write “1” to clear this bit. 0: No fault detected. 1: Fault detected.

STATE [7:0]			
ADDRESS: 0x1E			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7]	RESERVED	R	/
[6]	RESETB_STATE	R	RESETB pin real-time state. 0: Low 1: High
[5]	WD_OPEN	R	Watchdog open window real-time indicator. 0: Watchdog not open. 1: Watchdog open to feed.
[4]	RESERVED	R	/
[3:0]	SYS_STATE	R	System state machine real-time status. 0000: IDLE 0001: LOADOTP 0010: STANDBY 0100: TURNOFF 0101: NORMAL 0111: POWERUP 1010: DEEPSAFE 1100: SLEEP 1101: RECOVER 1110: RCVRST 1111: RESET Others: Reserved

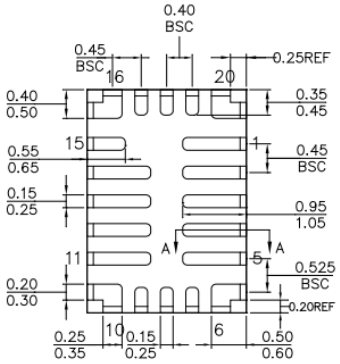
I2C_LOCK [7:0]			
ADDRESS: 0xE0			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	I2C_LOCK	W/R	Write correct password (DDh) to this register to unlock I2C write operation for registers under protection (see Register Map), or write anything else to lock it off. DDh: Protected registers are writeable. Others: Protected registers are read-only.

CTRL_RESTART [7:0]			
ADDRESS: 0xE1			
BITS	**FIELD**	**TYPE**	**DESCRIPTION**
[7:0]	PASSWORD_RESTART	W/R	Write correct password (write 65h, 3Eh continuously) to initiate a Power-On Reset. This register is self-clear.

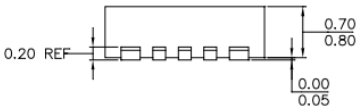
PACKAGE INFORMATION



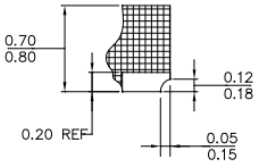
TOP VIEW



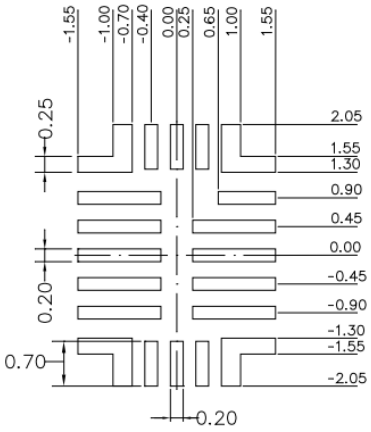
BOTTOM VIEW



SIDE VIEW



SECTION A-A

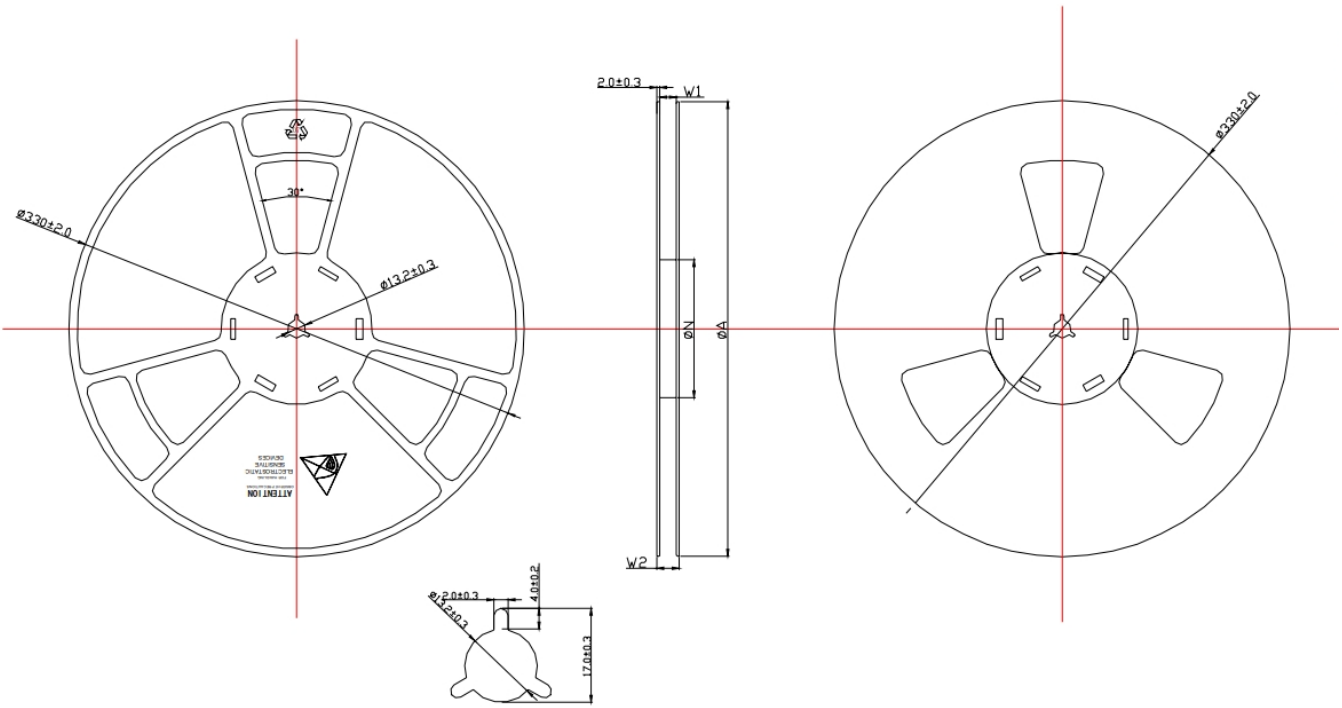


RECOMMENDED LAND PATTERN

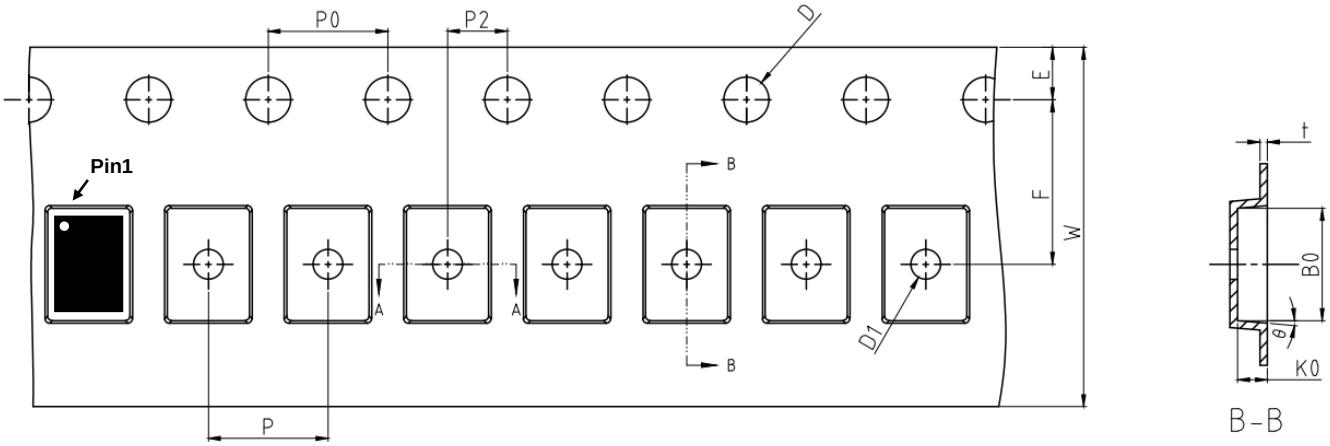
NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3)EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4



E	1.75±0.10
F	5.50±0.05
P_2	2.00±0.05
D	$1.50_{0}^{+0.10}$
D_1	1.00±0.10
P_0	4.00±0.10
$10P_0$	40.0±0.20

W	$12.00_{-0.10}^{+0.30}$
P	4.00±0.10
A_0	2.75±0.10
B_0	3.75±0.10
K_0	1.00±0.10
t	0.25±0.03
θ	5°max

