3.6V-36V Vin, 3A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Range: 3.6V-36V
- Up to 3A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 60mΩ High-Side and 36mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode (PSM) with 30uA Quiescent Current in Sleep Mode
- 60ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Switching Frequency: 200k~2.2MHz
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for adjustable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Parallel input path to minimize switch node ringing
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in 2mm*3mm QFN-12L Package

APPLICATIONS

- Battery Pack Powered System
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

DESCRIPTION

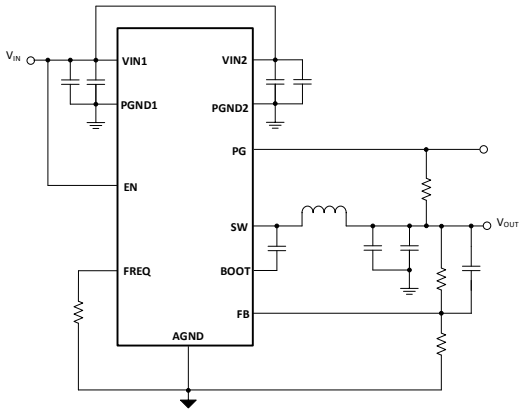
The SCT2434D is 3A synchronous buck converters with wide input voltage, ranging from 3.6V to 36V, which integrates a 60mΩ high-side MOSFET and a 36mΩ low-side MOSFET. The SCT2434D, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 30uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2434D features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency can be set between 200kHz and 2.1MHz through a resistor. The SCT2434D allows power conversion from high input voltage to low output voltage with a minimum 60ns on-time of high-side MOSFET.

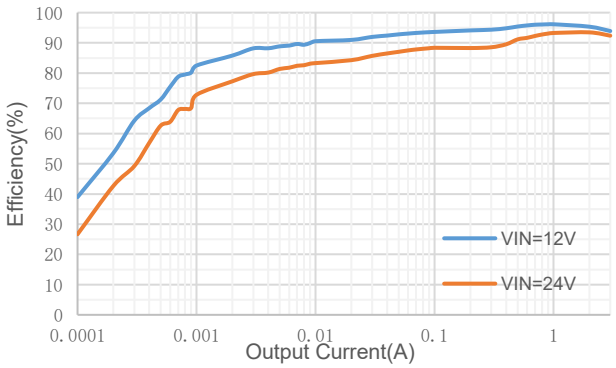
The SCT2434D is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2434D features Frequency Spread Spectrum FSS with ±10% jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2434D offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in 2mm*3mm QFN-12L package with wettable flanks.

TYPICAL APPLICATION



3.6V-36V, Synchronous Buck Converter



Efficiency, V_{OUT}=5V, F_{SW}=400kHz

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Released to Market

.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2434DFPAR	Tape & Reel	5000	434D	12	FCQFN2x3-12L	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	42	V
EN	-0.3	42	V
BOOT	-0.3	48	V
SW	-1	42	V
BOOT-SW	-0.3	6	V
PG	-0.3	24	V
FB	-0.3	6	V
Operating junction temperature TJ(3)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

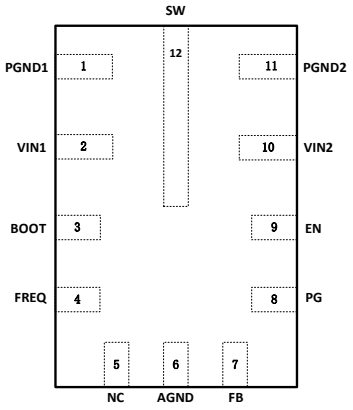


Figure 1. 12-Lead QFN 2mm×3mm

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PGND	1,11	Power ground to internal low side MOSFET. Connect to system ground. Low impedance connection should be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
VIN	2,10	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
BOOT	3	High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and BOOT. An internal diode connects to VCC and allows BOOT to charge while SW node is low.
FREQ	4	Frequency setting pin. Connect a resistor from this pin to ground to set the switching frequency.
NC	5	This pin has no internal connection to the regulator.
AGND	6	Analog ground for internal circuitry. Feedback are measured with respect to this pin. Must connect AGND to both PGND1 and PGND2 on PCB.
FB	7	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage. Do not float or connect to ground.

PG	8	Open-drain power-good status output. Pull this pin up to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. PG output goes low when EN =low, VIN > 1V.
EN	9	Enable pin to regulator with internal pull-up current source. Pull below 1.12V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
SW	12	Switching node of the buck converter.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.6	36	V
V_{OUT}	Output voltage range	1	16	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM)	-2	+2	kV
	Charged Device Model(CDM)	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-12L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	63.02	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.33	
Ψ_{JB}	Junction-to-board characterization parameter(1)	7.74	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	63.93	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	7.95	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2434D is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2434D. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.6		36	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		3.4	3.6	V
	Hysteresis			300		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0		1.2	10	μA
I_Q	Quiescent current from VIN pin	EN floating, non-switching, BOOT-SW=5V		30	55	μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=4.2V		60	100	mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			36	65	mΩ
Reference						
V_{REF}	Reference voltage of FB		0.788	0.8	0.812	V
						V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		4	5	6	A
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold		3.25	4.5	5.5	A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold		1.13	1.24	1.31	V
V_{EN_L}	Enable low threshold		1	1.12	1.19	V
I_{EN_L}	Enable pin pull-up current	EN=1V	0.4	1	1.5	μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V	3.5	4.8	6.5	uA
T_{ss}	Internal soft start time		2	4	7.2	ms
Switching Frequency and External Clock Synchronization						
F_{RANGE_CLK}	Frequency range using CLK mode		200		2200	kHz
F_{SW}	Switching frequency	R_{RT}=88.7 kΩ(1%)	320	400	480	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw	T_J=-40°C~125°C		±10%		Hz
t_{ON_MIN}	Minimum on-time	V_{IN}=36V		70		ns
Power Good						
V_{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		95		%
		POWER BAD (% of FB voltage)		90		%
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		110		%
		POWER GOOD (% of FB voltage)		105		%
I_{PG}	PWRGD leakage current at high level output	VPull-Up = 5V			200	nA
V_{PG_LOW}	PWRGD low level output voltage	IPull-Up = 1 mA		50		mV

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{PGDFLT(rise)}$	Delay time to PGOOD high signal			2	3.5	ms
$t_{PGDFLT(fall)}$	Glitch filter time constant for PGOOD function			130		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}		BOOT-SW falling		2.7		V
		Hysteresis		400		mV
T_{SD}	Thermal shutdown threshold*	T_J rising		160		°C
		Hysteresis		20		°C

*Derived from bench characterization

TYPICAL CHARACTERISTICS

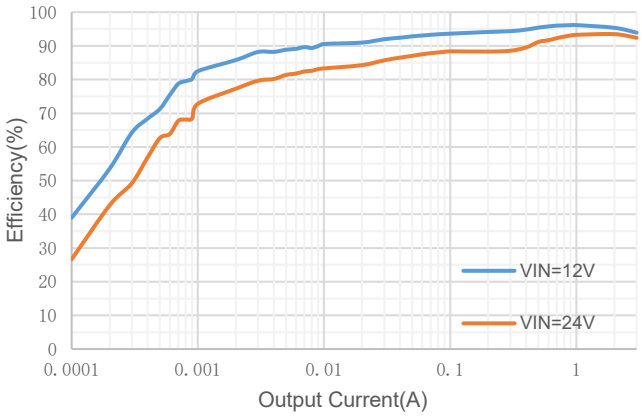


Figure 2. Efficiency, F_{SW}=400kHz, V_{OUT}=5V

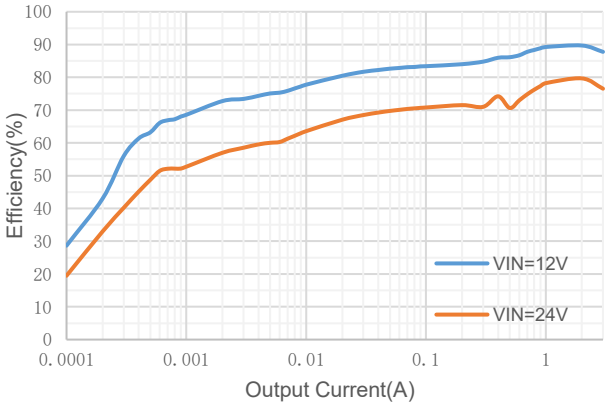


Figure 3. Efficiency, F_{SW}=2.2MHz, V_{OUT}=5V

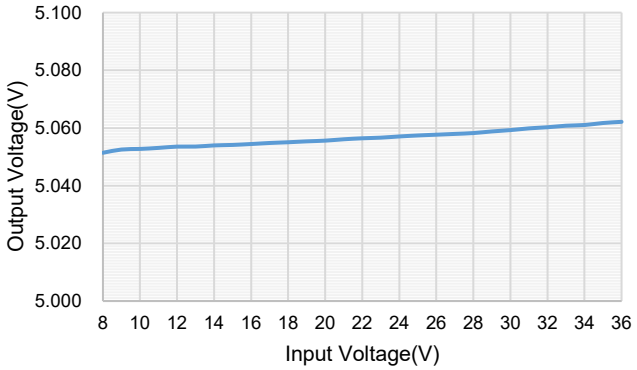


Figure 4. Line Regulation (FSW=400kHz,V_{OUT}=5V)

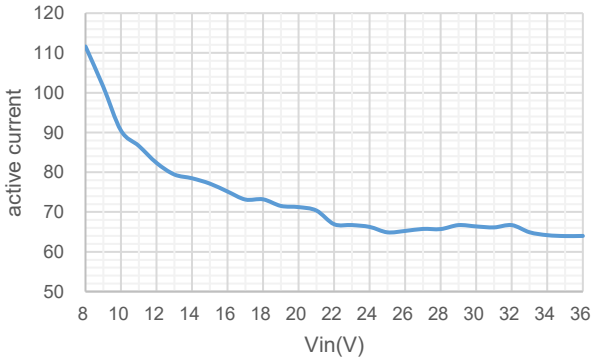


Figure 5. Input Current (V_{OUT}=5V, I_{LOAD}=0A)

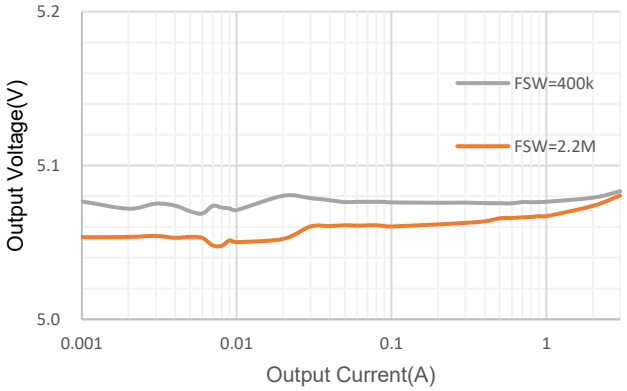


Figure 6. Load Regulation (V_{IN}=12V, V_{OUT}=5V)

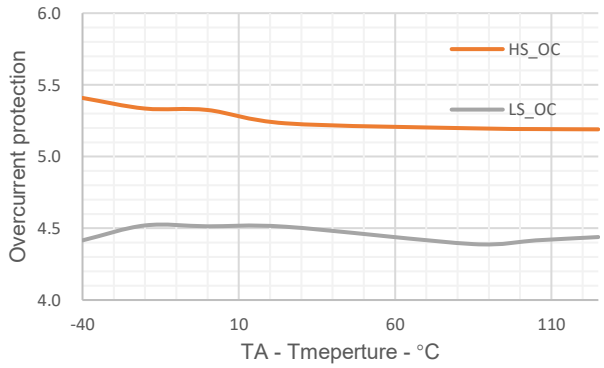


Figure 7. Current Limit vs Temperature

FUNCTIONAL BLOCK DIAGRAM

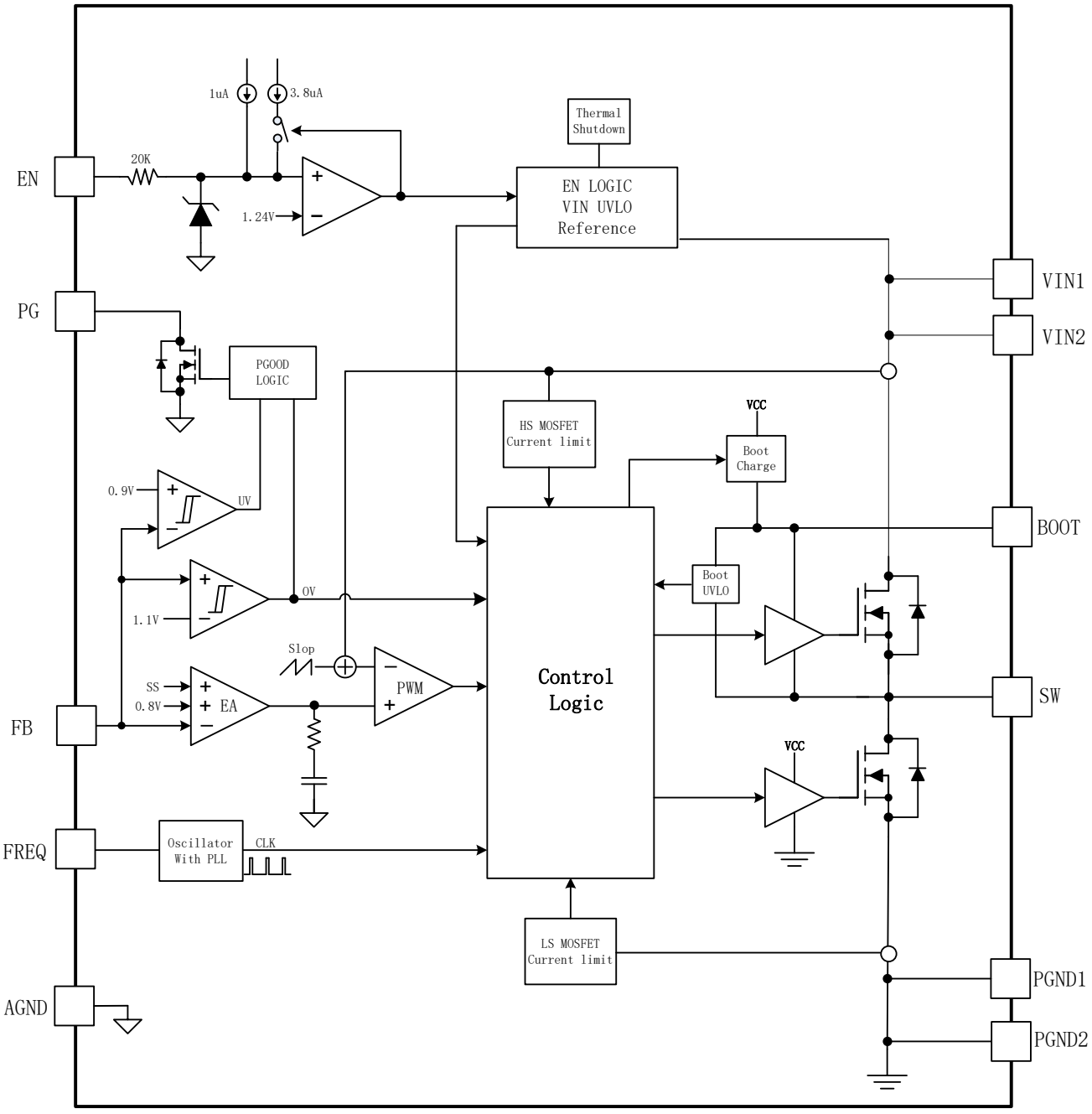


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2434D is a 3.6V-36V input, 3A output, EMI friendly synchronous buck converter with built-in 60mΩ Rdson high-side and 36mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 1.8MHz. The SCT2434D features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 30uA under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2434D implements the Frequency Spread Spectrum FSS modulation spreading of ±10% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2434D full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2434D employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2434D operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 0.8A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 30uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2434D is enabled when the VIN pin voltage rises about 3.4V and the EN pin voltage exceeds the enable threshold of 1.24V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.12V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R1 = \frac{V_{rise}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{fall}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (1)$$

$$R2 = \frac{R_1 \times V_{ENF}}{V_{fall} - V_{ENF} + R_1(I_1 + I_2)} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- I_1=1uA, I_2=3.8uA, V_{ENR}=1.24V, V_{ENF}=1.12V

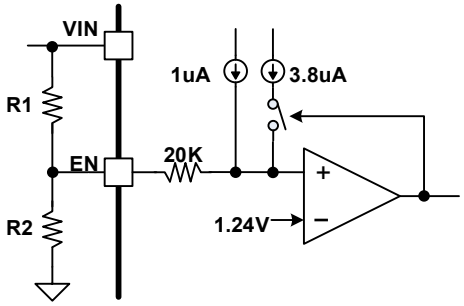


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2434D regulates the internal reference voltage at 1.0V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2434D integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.0V reference voltage in 4mS. If the EN pin is pulled below 1.12V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Frequency Spread Spectrum

The switching frequency of the SCT2434D is set by placing a resistor between FREQ pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between FREQ pin to the ground sets the switching frequency over a wide range from 200KHz to 2.2MHz. The FREQ pin voltage is typical 0.5V. FREQ pin is not allowed to be left floating or shorted to the ground. Use the plot in Table 1. to determine the resistance for a switching frequency needed.

Table 3. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_6 (R_{FSW})	Fsw	R_6 (R_{FSW})
200 KHz	182 KΩ	850 KHz	40.2 KΩ
300 KHz	120 KΩ	1000 KHz	34.8 KΩ
355 KHz	100 KΩ	1150 KHz	30.1 KΩ
400 KHz	88.7 KΩ	1450 KHz	22.6 KΩ
450 KHz	80.6 KΩ	1700 KHz	19.6 KΩ
520 KHz	68.1 KΩ	1900 KHz	17.8 KΩ
600 KHz	59 KΩ	2050 KHz	16.2 KΩ
700 KHz	51.1 KΩ	2200 KHz	15 KΩ

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 3.1V and hysteresis of 400mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.7V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, SCT2434D operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 3.1V. When the voltage from BOOT to SW drops below 2.7V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 3.1V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 98%.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2434D LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

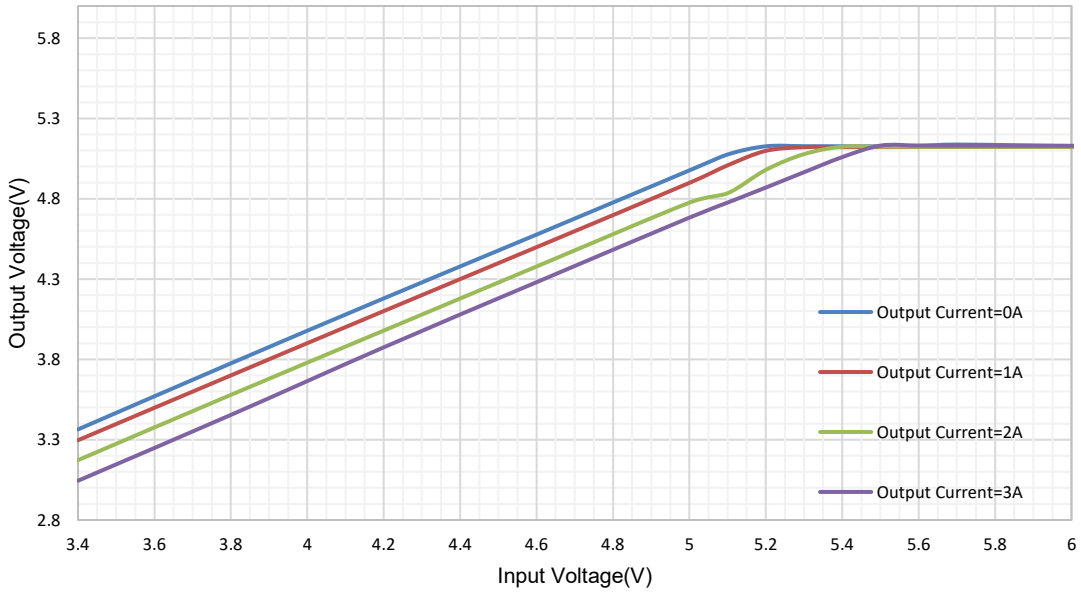


Figure 10. LDO Operation Characteristic (V_{OUT}=5V)

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2434D implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage 1.7V typical. When COMP voltage is clamped for 16 cycles of low side OC, the converter stops switching. After remaining OFF for 33.6ms，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high ， after soft start time and COMP still keep high for 16 cycles of low side OC，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2434D implements the Over-Voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 1.0V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 1.0V reference voltage, the high-side MOSFET can turn on again.

Power Good

The PG pin is an open-drain output. A pull up resistor between the values of 10KΩ and 100KΩ to a voltage source that is 5V or less is recommended.

Once the FB pin is between 95% and 105% of the internal voltage reference the PG pin is de-asserted and the pin floats with 2ms delay. The PG pin is pulled low when the FB is lower than 90% or greater than 110% of the nominal internal reference voltage with 130us deglitching time. Also, the PG is pulled low if Vin UVLO or thermal shutdown

are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 130us deglitching time do not trip the PG flag.

Thermal Shutdown

The SCT2434D protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 160°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 140°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

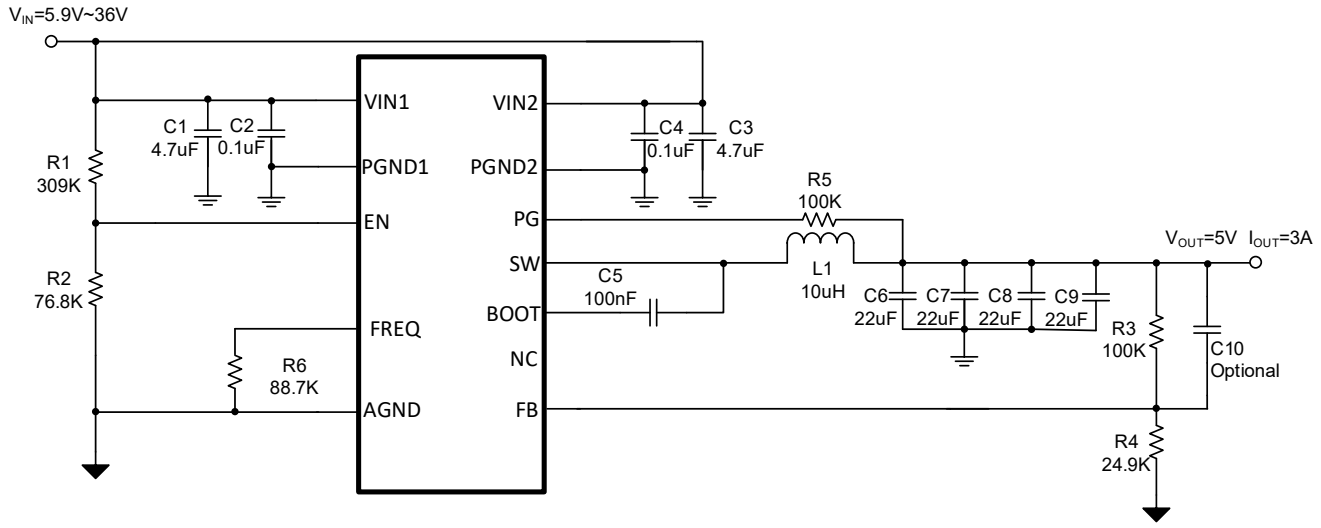


Figure 11. SCT2434D Design Example, 5V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 5.9V to 36V
Output Voltage	5V
Maximum Output Current	3A
Switching Frequency	400kHz
Output voltage ripple (peak to peak)	5mV
Transient Response 0.75A to 2.25A load step	ΔVout = 268mV
Start Input Voltage (rising VIN)	5.9V
Stop Input Voltage (falling VIN)	4.1V

Output Voltage

The output voltage is set by an external resistor divider R_3 and R_4 in typical application schematic. When the output voltage is greater than 3V, recommended R_4 resistance is 24.9KΩ. Use Equation 4 to calculate R_3.

$$R_3 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_4 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

If the output voltage is less than 3V, R_4 cannot exceed 24 KΩ.

Table 2. R_3, R_4Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_3	R_4
3.3 V	76.8 KΩ	24.9 KΩ
5 V	130 KΩ	24.9 KΩ
12 V	348 KΩ	24.9 KΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The 80ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 400 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from FREQ to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using table 2.

Table 3. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_6 (R_{FSW})	Fsw	R_6 (R_{FSW})
200 KHz	182 KΩ	850 KHz	40.2 KΩ
300 KHz	120 KΩ	1000 KHz	34.8 KΩ
355 KHz	100 KΩ	1150 KHz	30.1 KΩ
400 KHz	88.7 KΩ	1450 KHz	22.6 KΩ
450 KHz	80.6 KΩ	1700 KHz	19.6 KΩ
520 KHz	68.1 KΩ	1900 KHz	17.8 KΩ
600 KHz	59 KΩ	2050 KHz	16.2 KΩ
700 KHz	51.1 KΩ	2200 KHz	15 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.9V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.1V (stop or disable). Use Equation 5 and Equation 6 to calculate the values 309 kΩ and 76.8 kΩ of R_1 and R_2 resistors.

$$R_1 = \frac{V_{rise}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{fall}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (5)$$

$$R_2 = \frac{R_1 \times V_{ENF}}{V_{fall} - V_{ENF} + R_1(I_1 + I_2)} \quad (6)$$

where:

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- I_1=1uA, I_2=3.8uA, V_{ENR}=1.24V, V_{ENF}=1.12V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 7.

$$I_{LPP} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*f_{SW}} \quad (7)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 8 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW}*LIR*I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (8)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 9 and Equation 10.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (9)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (10)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current

- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 4.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 4.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2434D can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.3 to 0.5, and the inductor value is calculated to be 1.7uH, the RMS inductor current is 3A and the peak inductor current is 3.6A. The chosen inductor is a WE 74439358022, which has a saturation current rating of 12.55A. This also has a typical inductance of 2.2μH at no load and 2.19 μH at 3A load. The inductor DCR is 3.7mΩ.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 11.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (12)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For this example, two 4.7μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$\Delta V_{OUT} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{8*f_{SW}{}^2*L*C_{OUT}*V_{IN}} \quad (14)$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications.

Table 4: Typical External Component Values

V_{OUT}	R_3	R_4	R_6	L_1	C_{OUT}	C_{10}
3.3V	76.8 KΩ	24.9 KΩ	88.7 KΩ	6.8uH	4*22uF	22pF
5V	130 KΩ	24.9 KΩ	88.7 KΩ	10uH	4*22uF	Optional
3.3V	76.8 KΩ	24.9 KΩ	15 KΩ	1.5uH	4*22uF	22pF
5V	130 KΩ	24.9 KΩ	15 KΩ	2.2uH	4*22uF	Optional

Application Waveforms

V_{IN}=12V, V_{OUT}=5V, unless otherwise noted

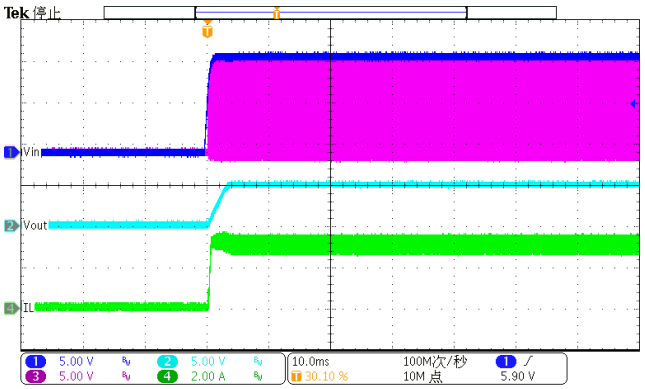


Figure 12. Power up(I_{LOAD}=3A)

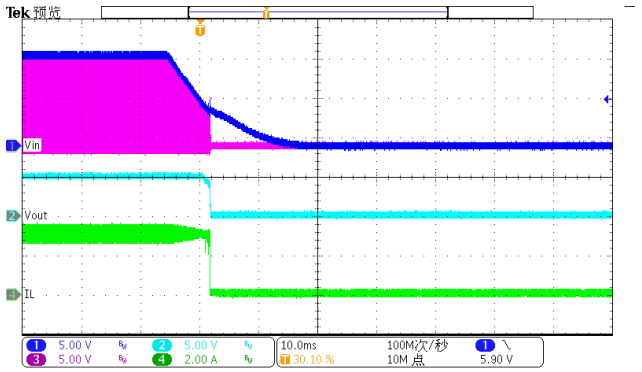


Figure 13. Power down(I_{LOAD}=3A)

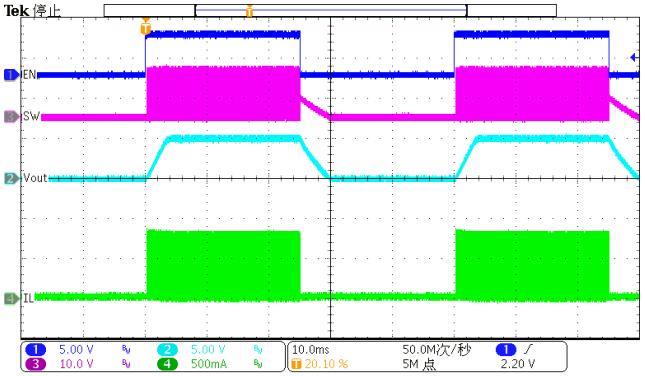


Figure 14. EN toggle (I_{LOAD}=0.1A)

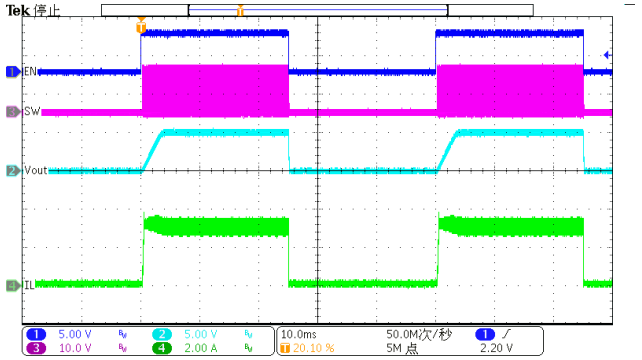


Figure 15. EN toggle (I_{LOAD}=3A)

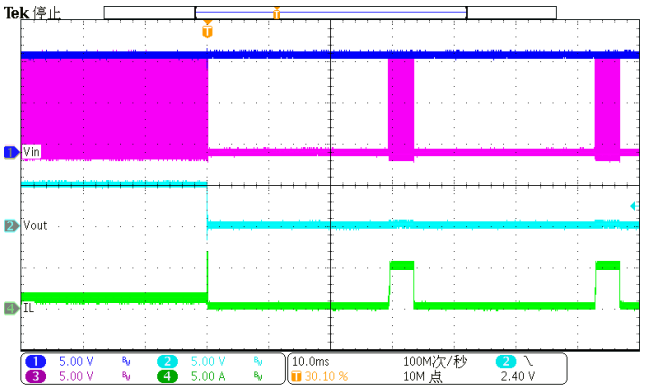


Figure 16. Over Current Protection(1A to hard short)

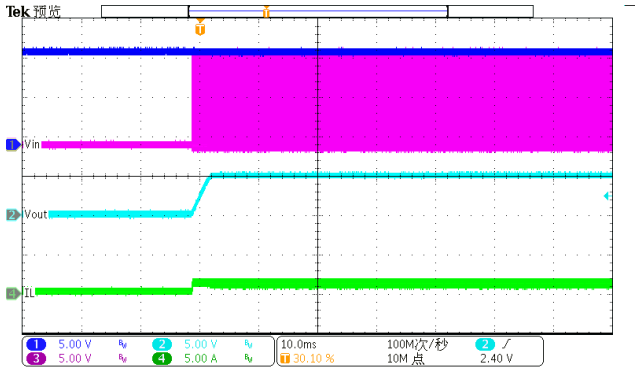


Figure 17. Over Current Release (hard short to 1A)

Application Waveforms

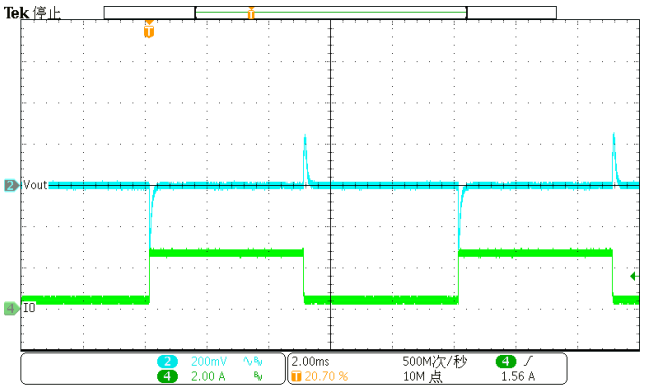


Figure 18. Load Transient (0.3A-2.7A, 1.6A/us)

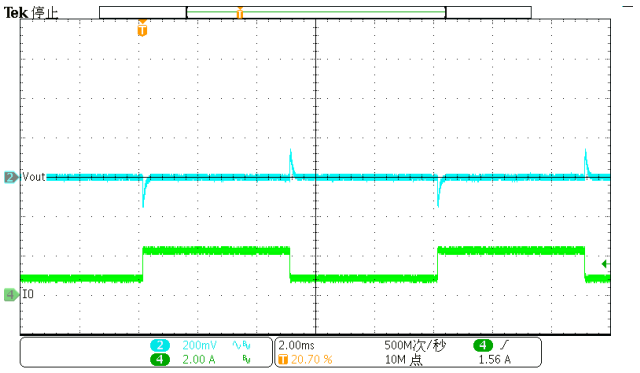


Figure 19. Load Transient (0.75A-2.25A, 1.6A/us)

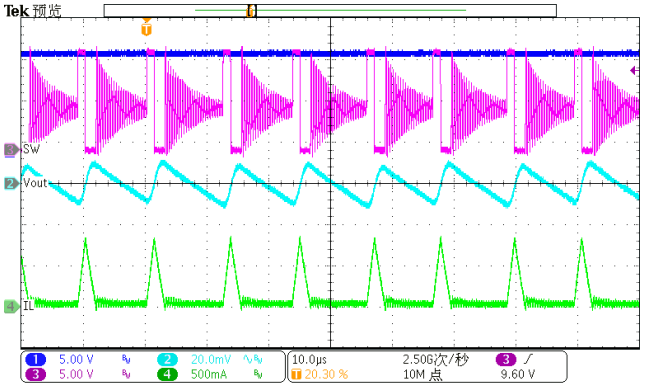


Figure 20. Output Ripple (I_{LOAD}=100mA)

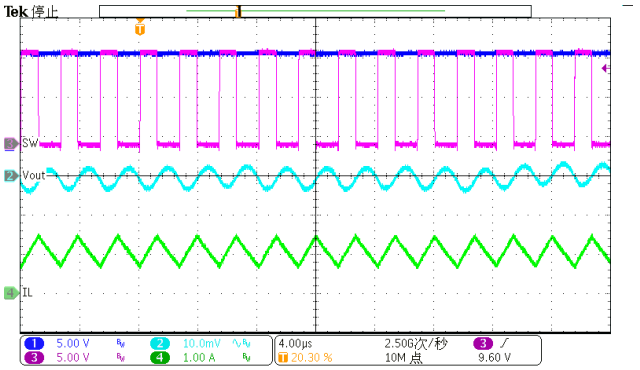


Figure 21. Output Ripple (I_{LOAD}=1A)

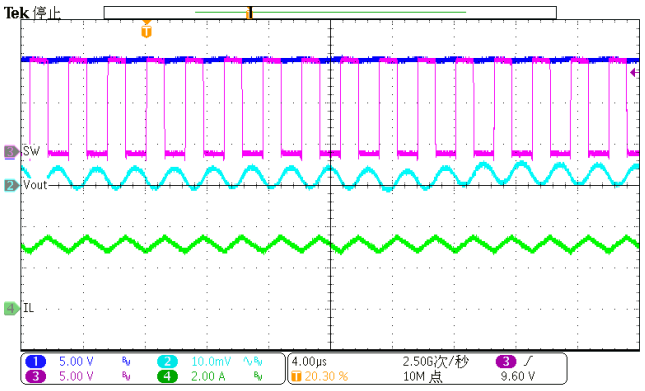


Figure 22. Output Ripple (I_{LOAD}=3A)

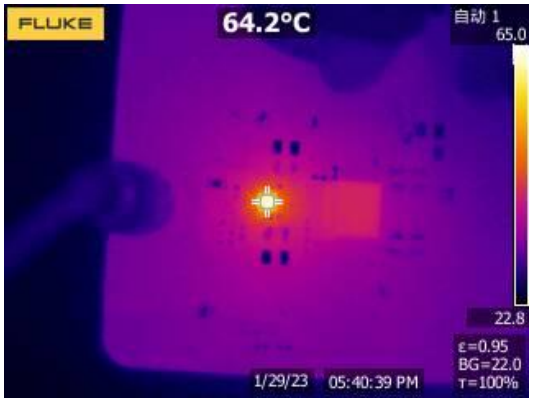


Figure 23. Thermal, 12V_{IN}, 5V_{OUT}, 3A

Layout Guideline

Proper PCB layout is a critical for SCT2434D's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. UVLO adjust and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
5. For achieving better thermal performance, a four-layer layout is strongly recommended.

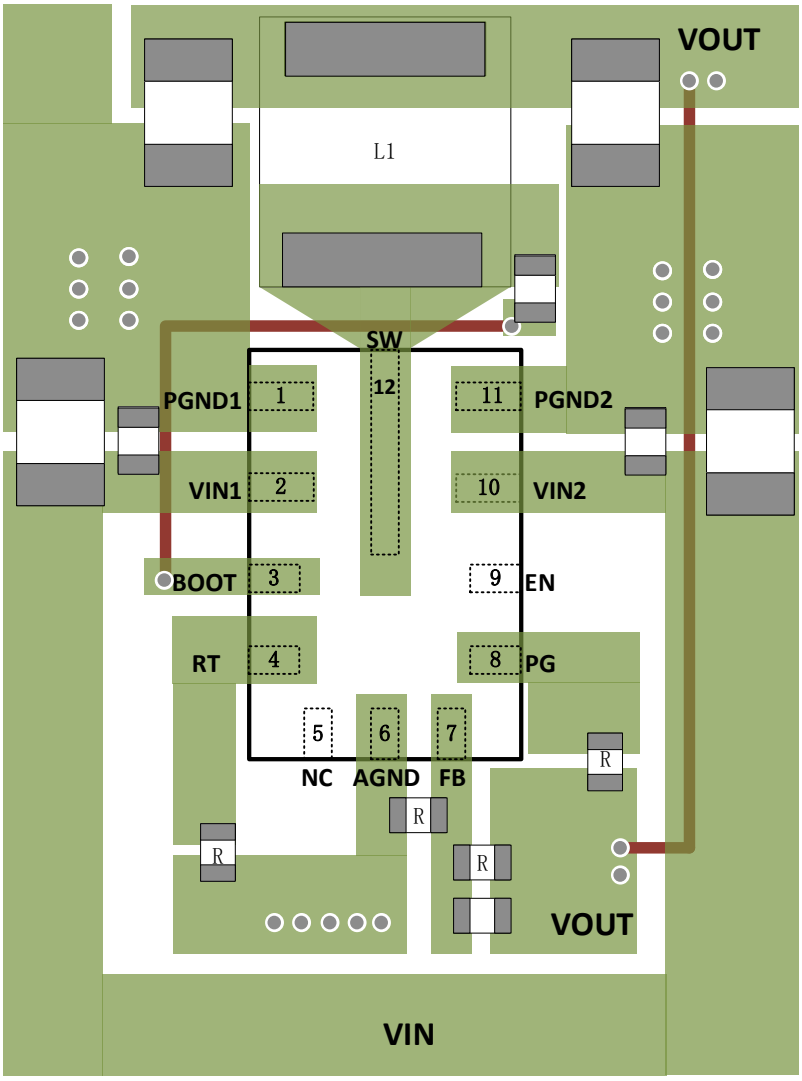
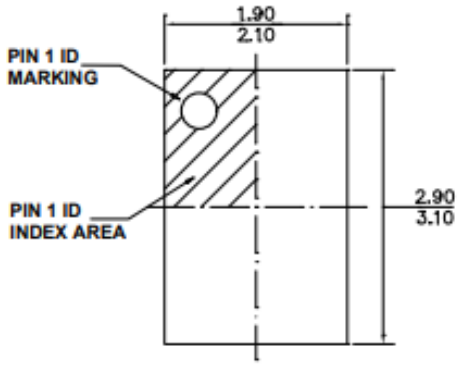
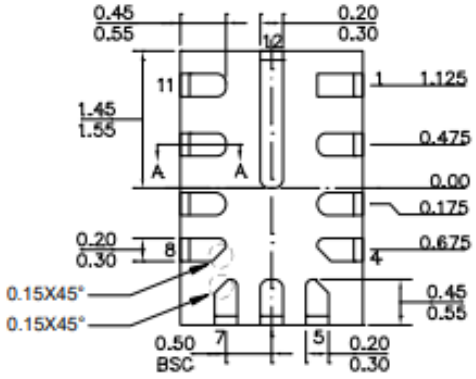


Figure 24. PCB Layout Example

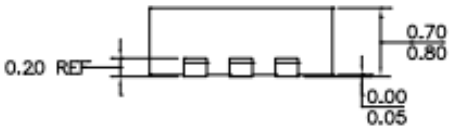
PACKAGE INFORMATION



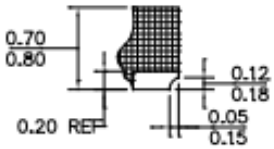
TOP VIEW



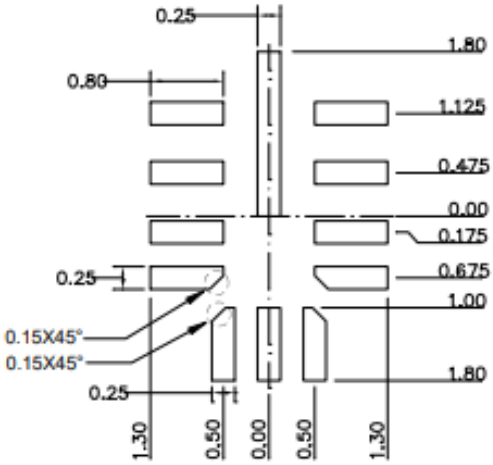
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION