

60V Input, 100mA Output Current, Low Quiescent Current LDO

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
 - - Device Temperature Grade 1: -40°C to 125°C
- Wide Input Range: 3V-60V
- Maximum Output Current: 100mA
- Adjustable Voltage: 1.2V-30V
- Output Voltage Accuracy:
 - $T_J = 25^\circ\text{C} : \pm 1\%$
 - $T_J = -40^\circ\text{C} \sim 125^\circ\text{C} : \pm 2\%$
- Low Quiescent Current: 4 μA
- Ultra-Low Shutdown Current: 0.35 μA
- Low Dropout Voltage :
 - 60mV at 20mA load current
 - 340mV at 100mA load current
- 770us Internal Soft-start Time
- Integrated Short-Circuit Protection with OCFB (Over Current Fold-back) Feature
- Enable pin is available
- Over-Temperature Protection
- Active Output Discharge
- Available Package: EMSOP-8L/ SOT223-4L

APPLICATIONS

- Emergency Call (eCall)
- Battery Management System (BMS)
- On-Board Charger (OBC) and wireless charger
- DC/DC converter

DESCRIPTION

The SCT71601Q product is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 60 V and 100mA output current with Enable control(EN) and an integrated open-drain, active-high, power-good output (PG) with a user programmable delay.

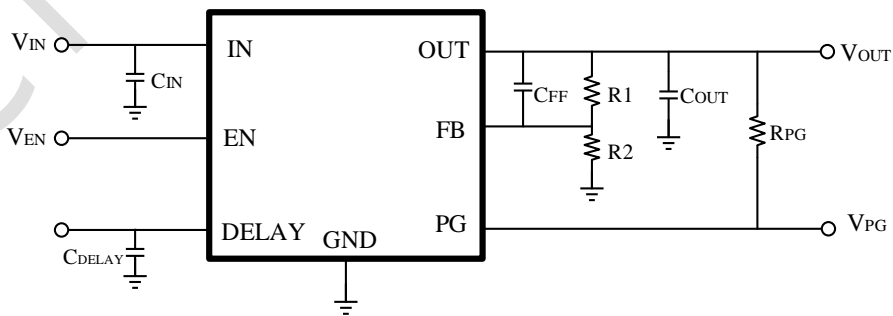
Only 4- μA typical quiescent current at light load makes the SCT71601Q product ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

The SCT71601Q product integrated short-circuit and overcurrent protection with OCFB (Over Current Fold-back) feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71601Q product could adjust output voltage version with 1.2V feedback voltage and have active output discharge.

The SCT71601Q product is available in EMSOP-8L and SOT223-4L packages, for other package options, please contact SCT sales.

TYPICAL APPLICATION



SCT71601Q Series

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Sampling.

Revision 0.81: Update electrical characteristic and typical characteristic.

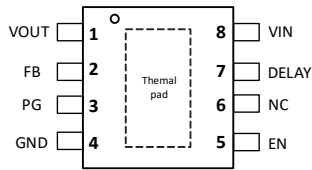
Revision 0.82: Update package information.

Revision 0.83: Add new package type and update relevant information.

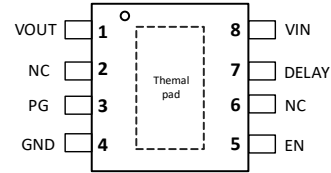
DEVICE ORDER INFORMATION

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
SCT71601A00QMTER	Adjust	EMSOP-8L	1A00Q	8	TBD	Tape & Reel, 4000
SCT71601F50QMTER	Fixed 5.0V	EMSOP-8L	1F50Q	8	TBD	Tape & Reel, 4000
SCT71601F33QMTER	Fixed 3.3V	EMSOP-8L	1F33Q	8	TBD	Tape & Reel, 4000
SCT71601F50QTXER	Fixed 5.0V	SOT223-4L	1F50Q	4	TBD	Tape & Reel, 2500

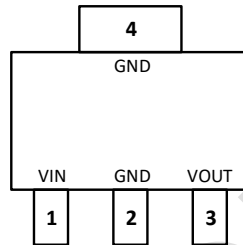
PIN CONFIGURATION



SCT71601A00QMTER
EMSOP-8L Package



SCT71601FxxQMTER
EMSOP-8L Package



SCT71601F50QTXER
SOT223-4L Package

PIN FUNCTIONS

EMSOP-8L/SCT71601A00Q/ SCT71601FxxQ:

NAME	NAME	PIN FUNCTION
1	VOUT	Regulated output voltage pin, A cap \geq 2.2uF must be tied from this pin to ground to assure stability.
2	FB/NC	For adjustable version, this is Feedback pin. For fixed versions, this is NC, must be left open.
3	PG	Power-good pin; Open-collector output; leave open or connect to GND if the power-good function is not needed.
4	GND	Ground reference pin.
5	EN	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_H}$, or EN is floating, the regulator is enabled. If $V_{EN} < V_{EN_L}$, the regulator is disabled. EN pin can be connected to VIN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
6	NC	No connection.
7	DELAY	Power-Good Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
8	VIN	Input voltage pin.
9	Thermal Pad	Connect the thermal pad to a large area GND plane for improved thermal performance.

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SOT223-4L/SCT71601F50Q:

NAME	NAME	PIN FUNCTION
1	VIN	Input voltage pin.
2、4	GND	Ground reference pin.
3	VOOUT	Regulated output voltage pin, A cap \geq 2.2uF must be tied from this pin to ground to assure stability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	3	60	V
V _{OUT}	Output voltage range	1.2	30	V
V _{EN}	Enable input voltage	0	V _{IN}	V
V _{PG}	Power-good pin voltage	0	5.5	V
DELAY	Programmable Power-Good Delay Time.	0	5	V
C _{IN}	Input capacitor	2.2	--	uF
C _{OUT}	Output capacitor	2.2	220	uF
ESR	Output capacitor ESR requirements	0.001	5	Ω
T _J	Operating junction temperature	-40	125	°C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted ⁽¹⁾

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Maximum input voltage range	-0.3	70	V
V _{OUT}	Maximum output voltage range	-0.3	35	V
V _{FB}	Maximum feedback pin voltage	-0.3	6.6	V
V _{EN}	Maximum enable input voltage	-0.3	V _{IN}	V
V _{PG} ⁽²⁾	Maximum power-good pin voltage	-0.3	6.6	V
V _{PGDL}	Maximum power-good delay pin voltage	-0.3	5.5	V
T _J ⁽³⁾	Junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) A current limit resistor should be connected between PG and the pulled-up power (eg. VOOUT or other power supply), When the pulled-up power is higher than 6V, the maximum Current Limit is better lower than 100uA to protect the Zener.
- (3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins ⁽¹⁾	-3	+3	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins ⁽²⁾	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. Because they were simulated in accordance with JESD 51-7. They do not represent the performance obtained in an actual application. For design information see Power Dissipation and Thermal Performance section.

The value of $R_{\theta JA_EVM}$ is the tested results based on our EVM, and is more useful for thermal design. Even if it still do not represent the thermal performance of customer's PCB design, but it was a good starting point for thermal performance design.

The PCB information of our EVM: 4-layer, 1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

The values given in this table are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB), thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the device. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual values of the below table.

PARAMETER	THERMAL METRIC	EMSOP-8L	UNIT
$R_{\theta JA}^{(1)}$	Junction to ambient thermal resistance	54.14	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.57	
Ψ_{JB}	Junction-to-board characterization parameter	19.28	
$R_{\theta JCtop}^{(2)}$	Junction to case thermal resistance	31.57	
$R_{\theta JA_EVM}^{(3)}$	junction to ambient thermal resistance	36.08	
PARAMETER	THERMAL METRIC	SOT223-4L	UNIT
$R_{\theta JA}^{(1)}$	Junction to ambient thermal resistance	60.71	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.85	
Ψ_{JB}	Junction-to-board characterization parameter	23.5	
$R_{\theta JCtop}^{(2)}$	Junction to case thermal resistance	57.99	
$R_{\theta JA_EVM}^{(3)}$	junction to ambient thermal resistance	27.24	

(1) $R_{\theta JA}$ is junction to ambient thermal resistance, based on JESD51-7.

(2) $R_{\theta JC}$ is junction to case thermal resistance, based on JESD51-7.

(3) $R_{\theta JA_EVM}$ is junction to ambient thermal resistance, which is tested on SCT EVM.

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ELECTRICAL CHARACTERISTICS

$V_{IN}=V_{OUT}+1V$, $C_{OUT}=10\mu F$, $T_J=-40^{\circ}C\sim 125^{\circ}C$, typical value is tested under $25^{\circ}C$.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3		60	V
V_{UVLO}	V_{IN} UVLO Threshold Hysteresis	V_{IN} rising		2.65 145		V mV
I_{SHDN}	Shutdown current from V_{IN} pin	EN=0, $V_{IN}=4.3V$		0.35	0.65	μA
		EN=0, $V_{IN}=48V$		2.4	5	μA
I_Q	Quiescent current from GND pin	EN float, no load, $V_{IN}=4.3V$, $T_J=25^{\circ}C$		4	6	μA
		EN float, no load, $V_{IN}=4.3V$, $T_J=-40^{\circ}C\sim 125^{\circ}C$			8.5	μA
		EN float, no load, $V_{IN}=60V$, $T_J=25^{\circ}C$		7.2	10	μA
		EN float, no load, $V_{IN}=60V$, $T_J=-40^{\circ}C\sim 125^{\circ}C$			14	μA
		EN float, no load, $V_{IN}=4.3V$, $T_J=25^{\circ}C$, (Fixed Output Version)		4.5		μA
		EN float, no load, $V_{IN}=60V$, $T_J=25^{\circ}C$, (Fixed Output Version)		7.7		μA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	$T_J=25^{\circ}C$		-1%	1%	
		$T_J=-40^{\circ}C\sim 125^{\circ}C$		-2%	2%	
VFB	Feedback voltage accuracy	$T_J=25^{\circ}C$	1.188	1.2	1.212	V
		$T_J=-40^{\circ}C\sim 125^{\circ}C$	1.176		1.224	V
ΔV_{OUT}	Line regulation	$V_{IN}=V_{OUT}+1V$ to 60V		1	55	mV
	Load regulation	$I_{OUT}=10\mu A$ to 100mA		9	25	mV
V_{DROP}	Dropout voltage ⁽¹⁾	$V_{IN}=V_{OUT}-0.1V$, $I_{OUT}=20mA$		60		mV
		$V_{IN}=V_{OUT}-0.1V$, $I_{OUT}=100mA$		340		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		100	mA
I_{OC}	Output current limit			200		mA
I_{OCFB}	Over Current Fold-back	$T_J=25^{\circ}C$		100		mA
PSRR	Power supply rejection ratio ⁽²⁾	$V_{OUT}=1.8V$, $I_{OUT}=10mA$, $f=1kHz$, $C_{OUT}=10\mu F$		73		dB
		$V_{OUT}=1.8V$, $I_{OUT}=10mA$, $f=10kHz$, $C_{OUT}=10\mu F$		59		dB
		$V_{OUT}=1.8V$, $I_{OUT}=10mA$, $f=100kHz$, $C_{OUT}=10\mu F$		51		dB
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.0		V
V_{EN_Hys}	Enable threshold hysteresis			200		mV
I_{EN_0V}	Enable pin pull-up current	EN=0V		0.2		μA
T_{SS}	Soft-start time			770		us
Over Voltage Protection						
OVP_H	overshoot of V_{out} when discharge occur			115%		

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
OVP _L	overshoot of V _{out} when discharge disappear			110%		
OVP _{Hys}	overshoot of V _{out} hysteresis			5%		
Power Good						
V _{PG_R}	PG rising threshold percentage	V _{OUT} /V _{OUT(NOM)} , when V _{OUT} rising		90%		
V _{PG_F}	PG falling threshold percentage	V _{OUT} /V _{OUT(NOM)} , when V _{OUT} falling		87%		
V _{HYS}	PG trip hysteresis			3%		
V _{PG_LOW}	PG output low voltage	V _{OUT} =0.8xV _{OUT(NOM)} , PG sink 100uA		76		mV
R _{GR}	PG pull down resistor	R _{GR} = V _{PG_LOW} / 0.1mA		150		Ω
I _{PG_LKG}	PG leakage current	V _{OUT(NOM)} , V _{OUT} in regulation			0.2	uA
I _{PGDL}	PGDL charging current ⁽³⁾	T _J = 25°C		1	2	uA
Thermal Protection						
T _{SD}	Thermal shutdown threshold ⁽⁴⁾	T _J rising Hysteresis		170 15		°C °C

- (1) The dropout voltage is defined as V_{IN}-V_{OUT}, when force V_{IN} is 100mV below the value of V_{OUT} for V_{IN}=V_{OUT(NOM)}+1V.
- (2) PSRR is derived from bench characterization, not production test.
- (3) I_{PGDL} will have updated to 1uA when this product has released to production.
- (4) Thermal shutdown threshold is derived from bench characterization, not production test.

TYPICAL CHARACTERISTICS

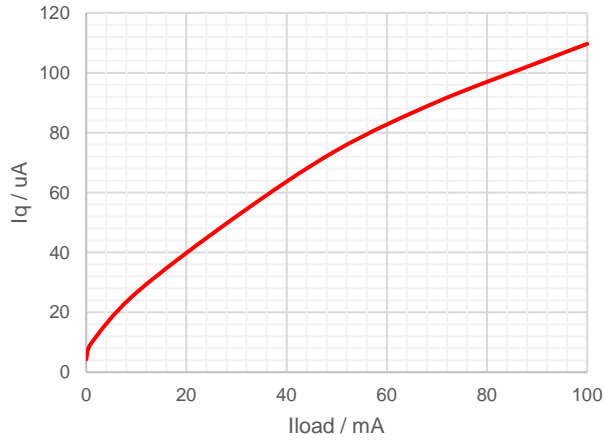


Figure 1. Quiescent Current vs Output Current

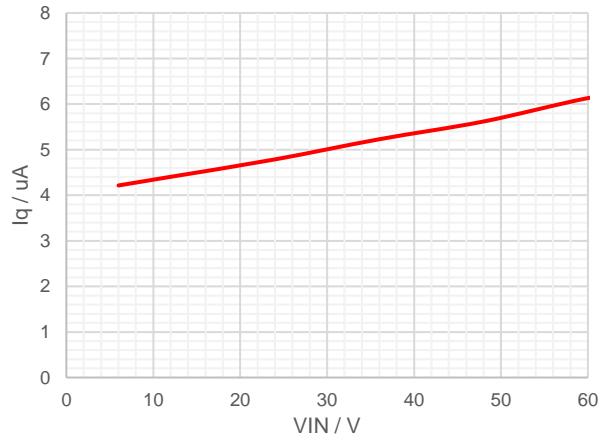


Figure 2. Quiescent Current vs Input Voltage, No load

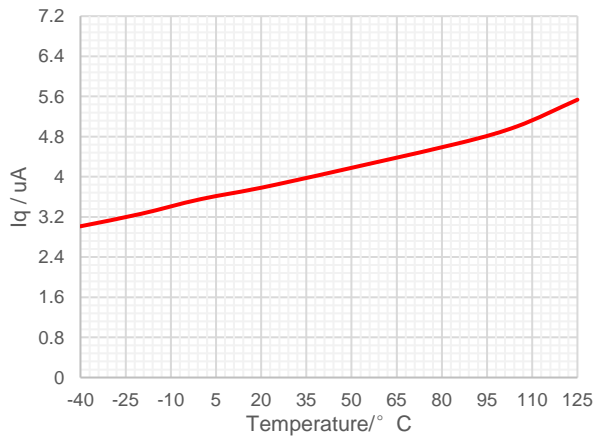


Figure 3. Quiescent Current vs Ambient Temperature

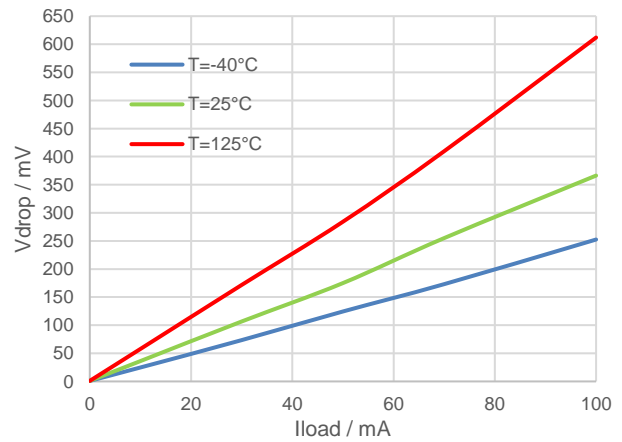


Figure 4. Dropout Voltage vs Output Current

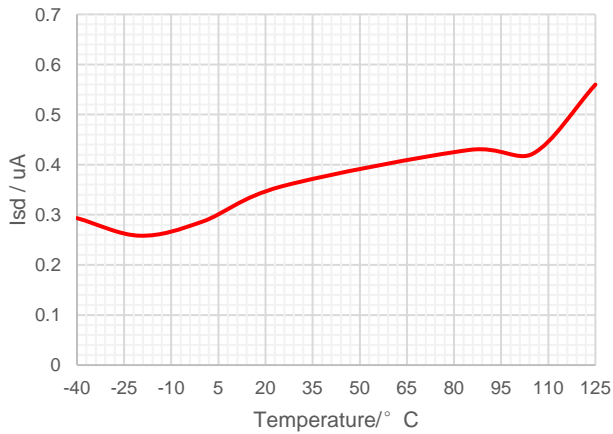


Figure 5. Shutdown Current vs Ambient Temperature

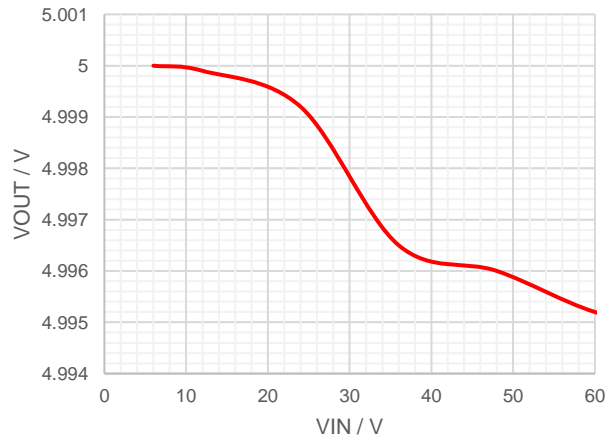


Figure 6. Output Voltage vs Input Voltage

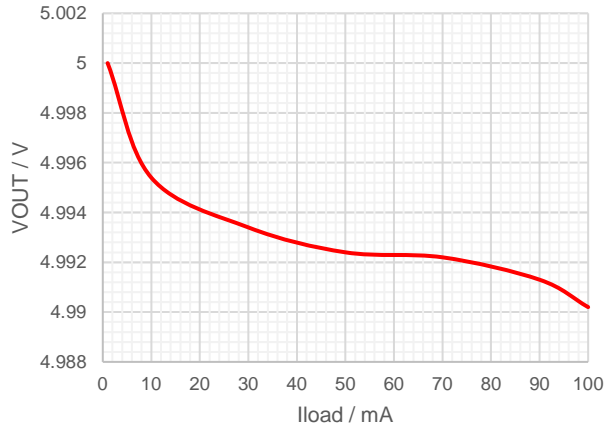


Figure 7. Output Voltage vs Output Current

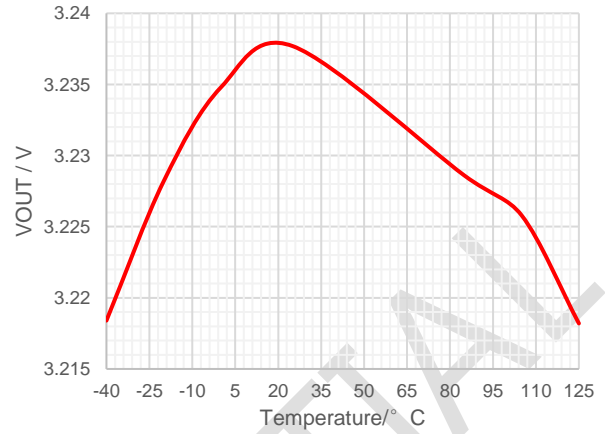


Figure 8. Output Voltage vs Ambient Temperature at VOUT=3.3V

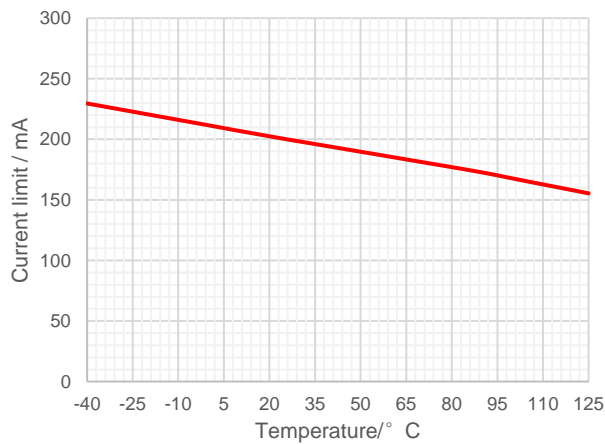


Figure 9. Output Current Limit vs Ambient Temperature at VIN<55V

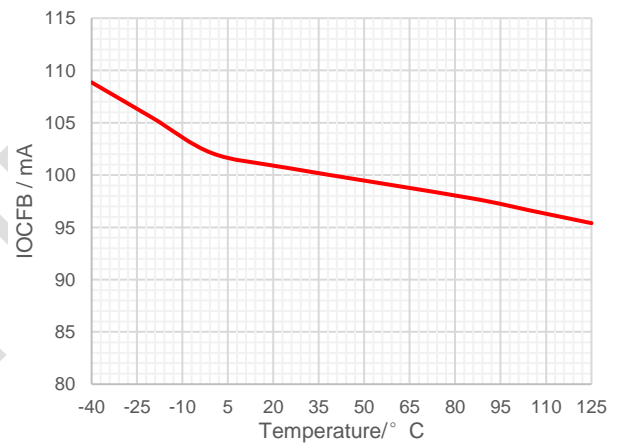


Figure 10. Output Current Limit vs Ambient Temperature at VIN≥55V

TYPICAL CHARACTERISTICS (continued)

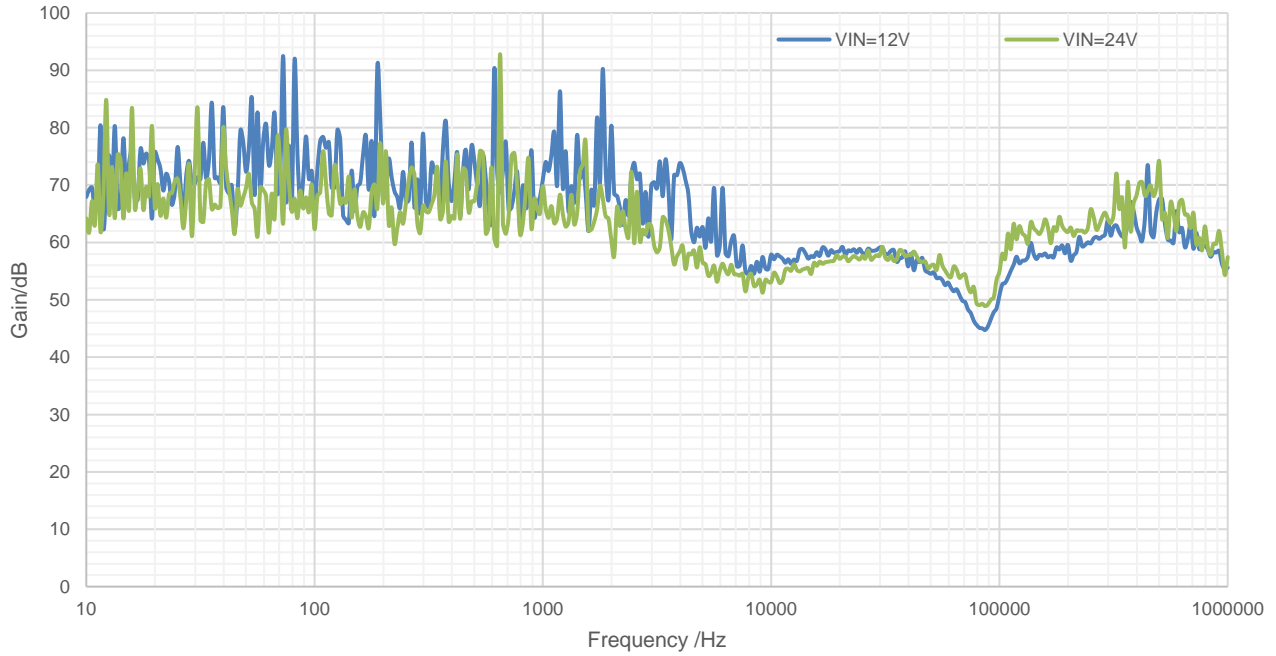


Figure 11. PSRR vs Frequency
VOUT=3.3V,Cf=10pF,COUT=10uF,IOUT=10mA

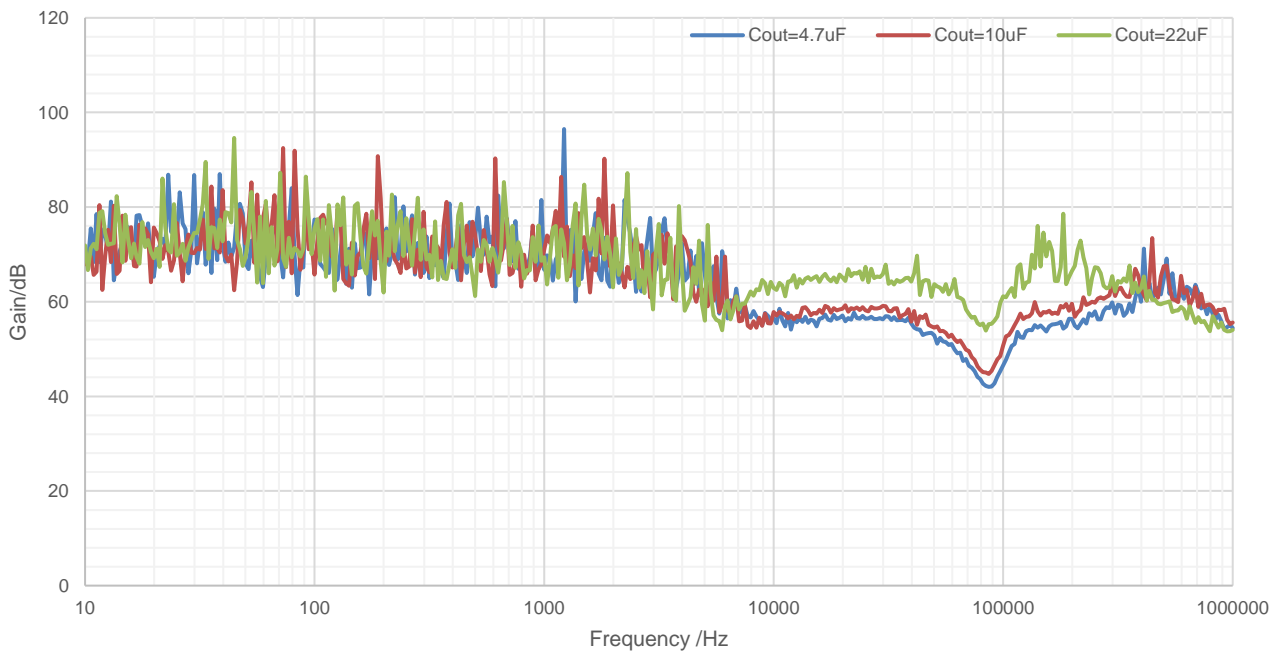


Figure 12. PSRR vs Frequency
VIN=12V,VOUT=3.3V,Cf=10pF,IOUT=10mA

TYPICAL CHARACTERISTICS (continued)

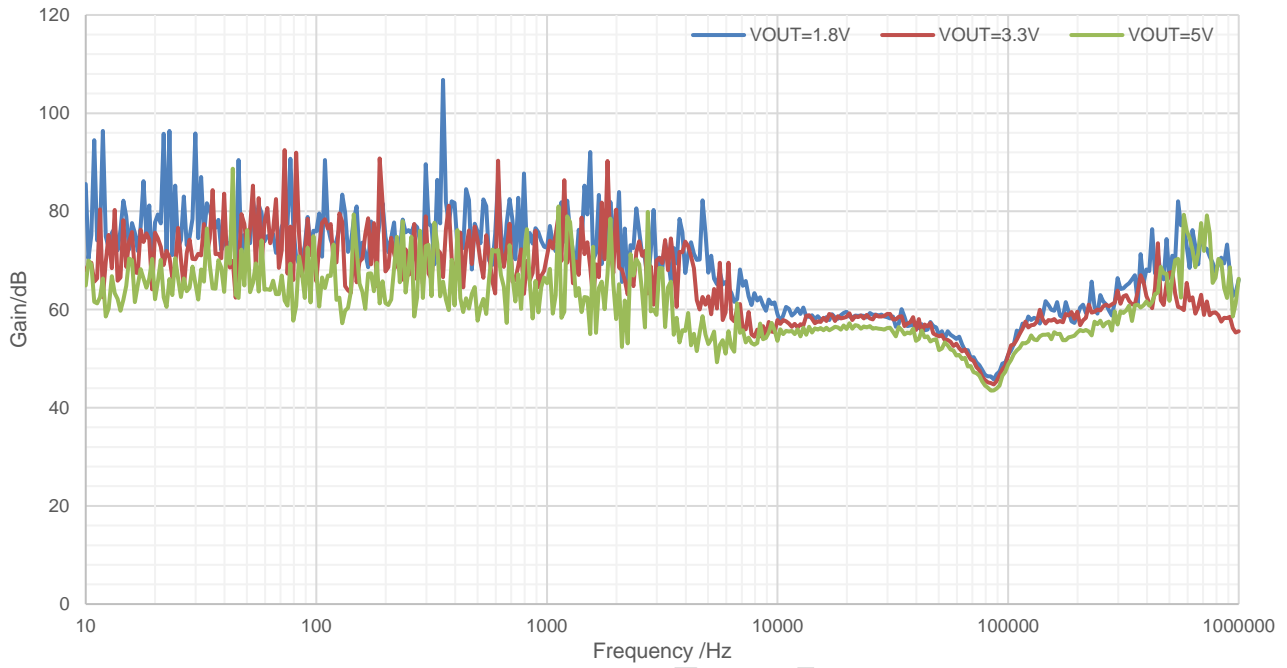


Figure 13. PSRR vs Frequency
VIN=12V, Cf=10pF, COU=10uF, IOU=10mA

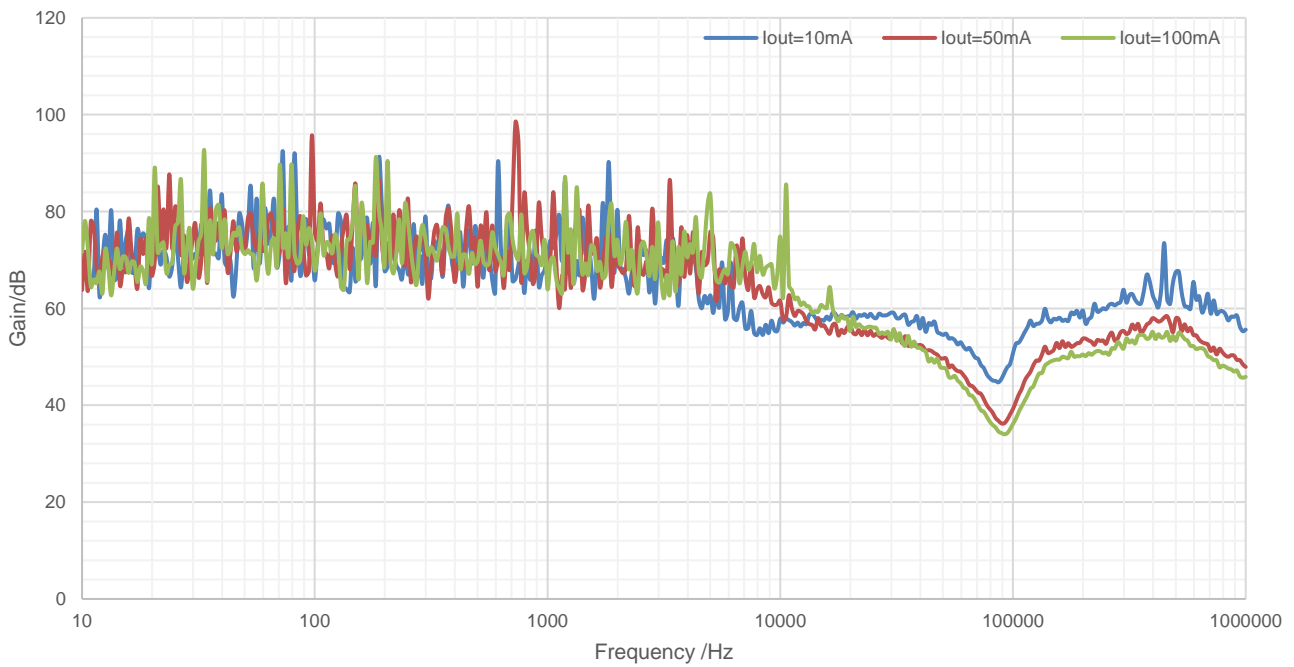


Figure 14. PSRR vs Frequency
VIN=12V, VOUT=3.3V, Cf=10pF, COU=10uF

FUNCTIONAL BLOCK DIAGRAM

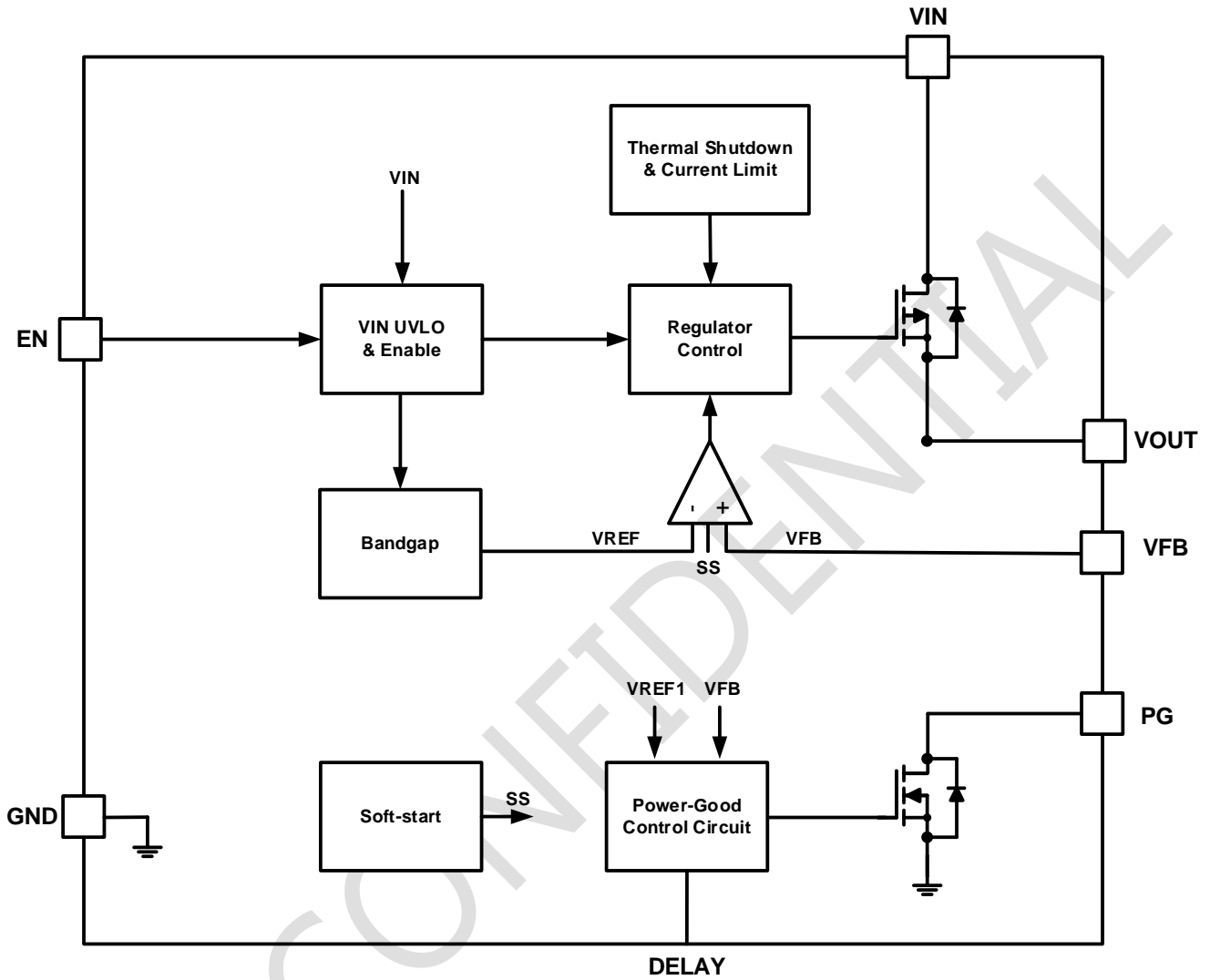


Figure 15. Functional Block Diagram of Adjust Output Version

OPERATION

Overview

The SCT71601Q series products are 100mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 60V DC input voltage and consume 4μA quiescent current at no load.

The SCT71601Q series products is stable with 3.3μF~220μF output capacitors, and 10μF ceramic capacitor is recommended. An internal 770us soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71601Q series products also provide enable control, Power-Good feature and programmable Power-Good delay time which is very suitable for the applications needing sequence configuration. Other protection features include the VIN input under-voltage lockout, over current protection, output hard short protection and thermal shutdown protection.

The SCT71601Q series products provide adjustable output version from 1.2V to 30V. If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

Enable and Under Voltage Lockout Threshold

The SCT71601Q series products is enabled when the VIN pin voltage rises above 2.65V and the EN pin voltage exceeds the enable threshold V_{EN_H} . The device is disabled when the VIN pin voltage falls below 2.65V or when the EN pin voltage is below V_{EN_L} . Internal pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) from VIN to GND shown in Figure 11. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN_H} * \frac{R1 + R2}{R2} \quad (1)$$

$$VIN_{hys} = (V_{EN_H} - V_{EN_L}) * \frac{R1 + R2}{R2} \quad (2)$$

Where

VIN_{rise} : Vin rise threshold to enable the device

VIN_{hys} : Vin hysteresis threshold

$I_1=0.2\mu A$ and could be neglected in the calculation

$V_{EN_H}=1.2V$

$V_{EN_L}=1.0V$

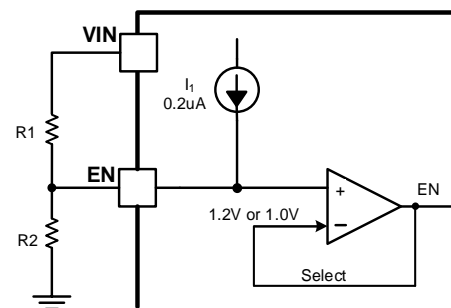


Figure 16. System UVLO by enable divide

Regulated Output Voltage

When the input voltage is higher than $V_{OUT(NOM)}+V_{DROD}$, output pin is the regulated output based on the required voltage version. When the input voltage falls below $V_{OUT(NOM)}+V_{DROD}$, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

Over Current Limit and Foldback Current Limit

The SCT71601Q series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is 200mA when $VIN < VIN_HIGH$, but SCT71601Q supplies a fold-back current limit 100mA when $VIN > VIN_HIGH$.

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The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

With the over current VIN_HIGH Control feature, the SCT71601Q series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than I_{sc} during startup. The characteristic is shown in the following figure.

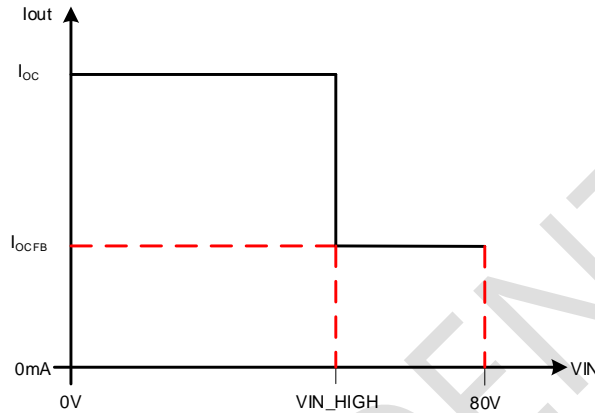


Figure 17. Current Limit with Foldback Feature

Internal Soft-Start

The SCT71601Q series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.2V reference voltage in 770us. If the EN pin is pulled below 1V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limit by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by current limit (I_{oc}) at VIN < VIN_HIGH, and the slope of VOUT is limited by current limit (I_{ocFB}), when VIN > VIN_HIGH.

In SCT71601Q series products, typical T_{ss} is 770us, and typical I_{oc} is 200mA and typical I_{ocFB} is 100mA, could use the following formula for initial startup time calculation.

$$T_{start} = \max \left\{ \frac{C_{OUT} \times V_{OUT}}{(I_{sc} - I_{load})}, T_{SS} \right\} \quad (3)$$

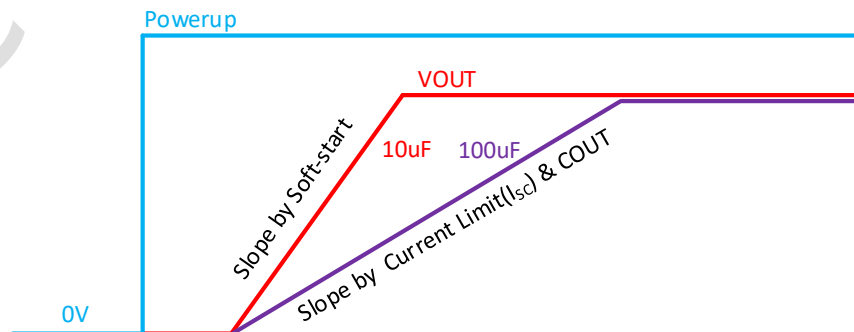


Figure 18. Soft-start Waveform vs Output Capacitor

Power-Good and Power-Good Delay

The power-good (PG) pin is an open-drain output and can be connected to any 6V or lower rail through an external pull-up resistor. The PG output is high-impedance when V_{OUT} is greater than the PG trip threshold ($V_{PG_R}=90\% \times V_{OUT(NOM)}$). If V_{OUT} drops below $V_{PG_F}=87\% \times V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

If the power-good delay time is not enough for some application, could connect a external capacitor from DELAY pin to GND, this capacitor is charged from 0 V to 1.2 V by the DELAY pin current (I_{DELAY}) and generate extra delay time. When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT} , and V_{DELAY} exceeds V_{REF} . The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF}) / I_{DELAY}$. For example, when $C_{DELAY} = 10 \text{ nF}$, the PG delay time is approximately 12 ms; that is, $(10 \text{ nF} \times 1.2\text{V}) / 1 \mu\text{A} = 12 \text{ ms}$.

To ensure proper operation of the power-good feature, maintain $V_{IN} \geq 3\text{V}$ (V_{IN_MIN}). It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's V_{OUT} level. Below are the connections examples.

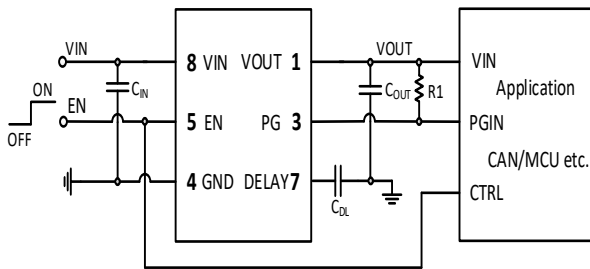


Figure 19. PG Connected to LDO's Output

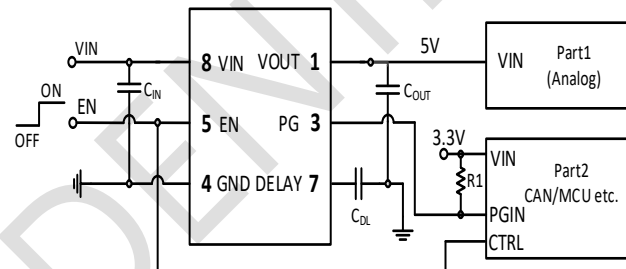


Figure 20. PG Connected to the other Power Supply

Below figure shows the startup and shutdown situation when slow power up and power down.

At the point 0, the input voltage starts to rise from 0 to 2.65 V, LDO is in shutdown (because V_{IN} is below its UVLO threshold) and output voltage is 0V.

At the point 1, the V_{IN} voltage reaches UVLO threshold level and LDO starts charging of output capacitor. V_{OUT} rising speed is defined by internal soft-start function.

At the point 2, the V_{OUT} voltage reaches almost the V_{IN} voltage as it rises faster and LDO gets into dropout region. The difference between V_{IN} and V_{OUT} is the dropout voltage.

At the point 3, the V_{OUT} reaches PG threshold ($V_{PG_R}=90\% \times V_{OUT(NOM)}$) and from this point LDO counts the power good delay time. After this delay, the PG pin rises to high level showing that V_{OUT} is ok.

At the point 4, the V_{OUT} reaches its nominal value (5.0V version) as the V_{IN} starts to be higher than ($V_{OUT(NOM)} + V_{DROD}$) and LDO gets into regulation region.

At the point 5, as the V_{IN} voltage slow power down and LDO returns to dropout region again.

At the point 6, the V_{OUT} drops below PG threshold ($V_{PG_F}=87\% \times V_{OUT(NOM)}$) and LDO starts counting the power good deglitch time, which filters fast V_{OUT} undershoots (caused for example by line/load transient responses). After this delay, the PG output is shorted to 0 V level to highlight "power fail" state.

At the point 7, the V_{IN} voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.

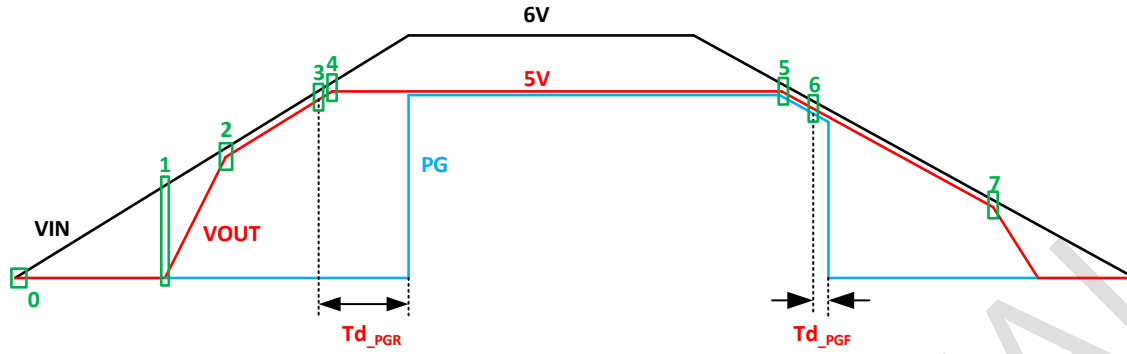


Figure 21. Startup and Shutdown Example —SCT71601Q Series

Thermal Shutdown

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

APPLICATION INFORMATION

Typical application 1:

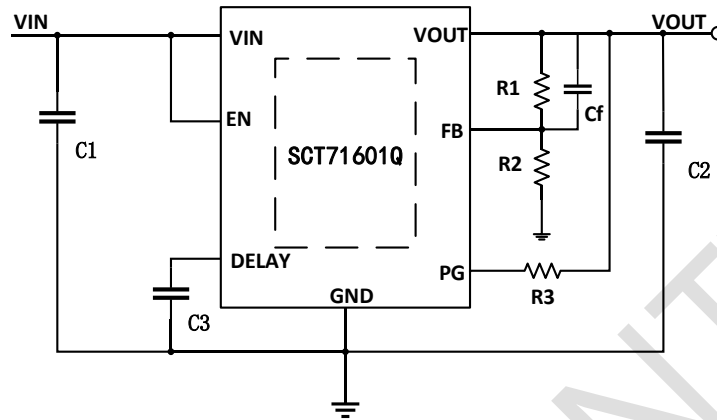


Figure 22. SCT71601Q Typical Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~60V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C ₂)	2.2uF~220uF , recommends 10uF
Input Capacitor Range (C ₁)	≥2.2uF , recommends 10uF
Pull-up resistor of power-good (R ₃)	>100kΩ

Typical application 2:

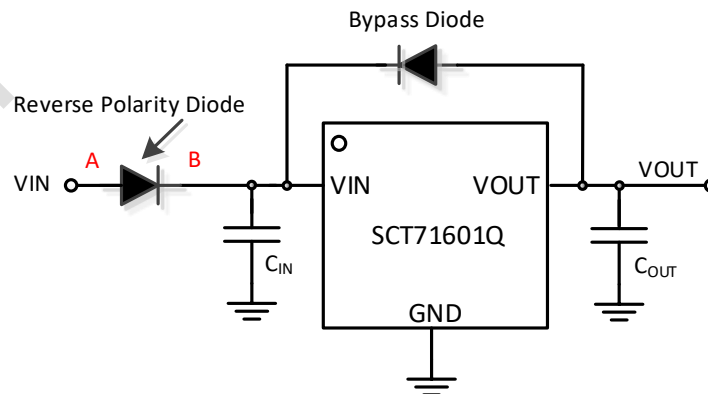


Figure 23. SCT71601Q Typical Application Schematic with Reverse Polarity Diode

SCT71601Q Series

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~60V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C_{OUT})	2.2uF~220uF , recommends 10uF
Input Capacitor Range (C_{IN})	$\geq 2.2uF$, recommends 10uF

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220 μ F. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

Typical application 3:

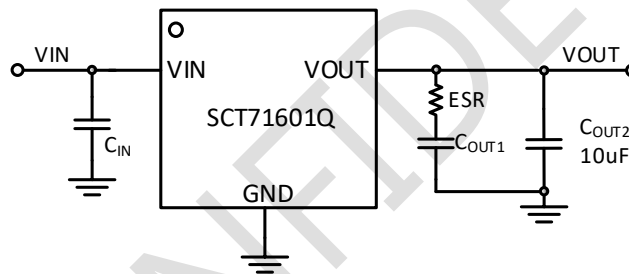


Figure 24. SCT71601Q Typical Application Schematic with Large Output Capacitor

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~60V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C_{OUT1} and ESR)	2.2uF~220uF with ESR=0.5 Ω ~5 Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	$\geq 2.2uF$, recommends 10uF

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 100kΩ. Use equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) * R_2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.2V

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

Vout/V	CO _{UT} /uF	C _f /pF	R1/kΩ	R2/kΩ	CO _{UT1} /uF (optional)	ESR/Ω
1.8	10	33	51.1	100	220	1
2.5	10	33	107	100	220	1
3.3	10	33	174	100	220	1
5	10	33	316	100	220	1
12	10	33	909	100	220	1

Input Capacitor and Output Capacitor

SCT recommends adding a 2.2μF or greater capacitor with a 0.1μF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71601Q product requires an output capacitor with a minimum effective capacitance value of 2.2μF. And the product could support output capacitor range from 2.2uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

SCT71601Q Series

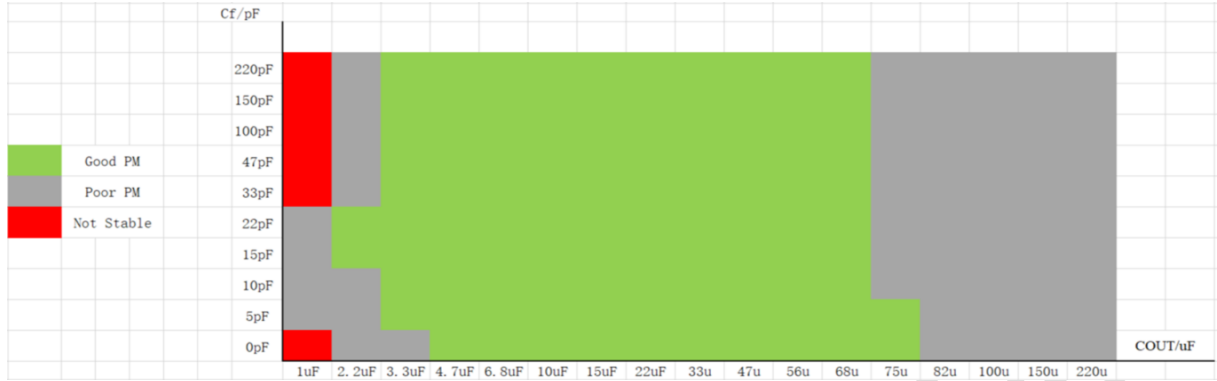


Figure 25. SCT71601Q Feed Forward Capacitors recommend($R_2=100\text{k}\Omega, V_{OUT}=1.8\text{V}$)

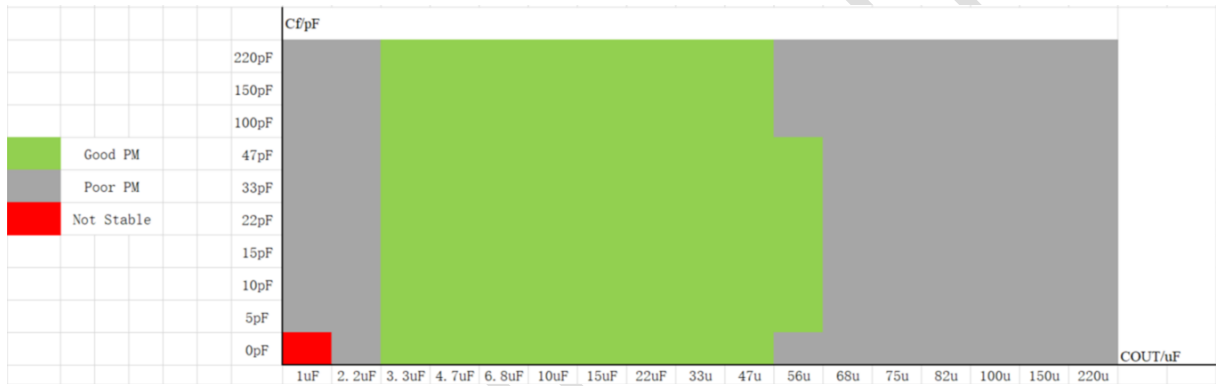


Figure 26. SCT71601Q Feed Forward Capacitors recommend($R_2=10\text{k}\Omega, V_{OUT}=1.8\text{V}$)

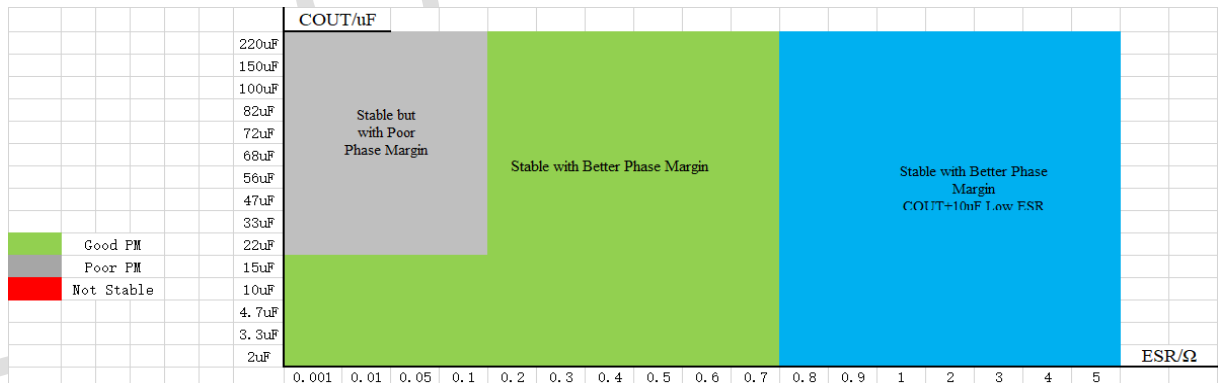


Figure 27. SCT71601Q Stability VS Output Capacitor

Power Dissipation and Thermal Performance

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 5. Because $I_{GND} \ll I_{OUT}$, the term $V_{IN} \times I_{GND}$ in Equation 5 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (5)$$

The junction temperature can be estimated using Equation 6. $R_{\theta JA_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J .

$$T_J = T_A + P_D \times R_{\theta JA_EVM} \quad (6)$$

$R_{\theta JA_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71601Q product, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer, 11oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD, VOUT=5V)	Max Allowable PD (W) (T _J ≤125°C)	R _{θJA_EVM} (°C/W)
EMSOP-8L	4.019	2.772	36.08
SOT223-4L	5.323	3.671	27.24

THERMAL CHARACTERISTICS

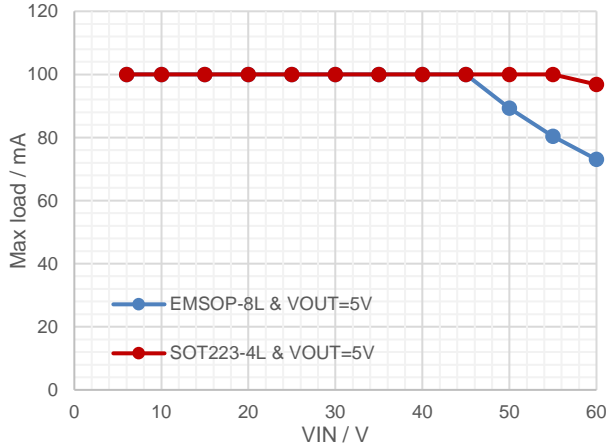


Figure 28. Maximum Output Current vs Input Voltage, VOUT=5V of different packages, $T_J \leq T_{SD_R}$

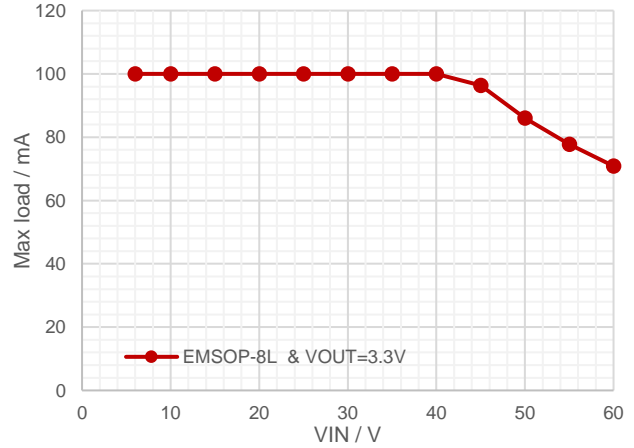


Figure 29. Maximum Output Current vs Input Voltage, VOUT=3.3V of EMSOP-8L, $T_J \leq T_{SD_R}$

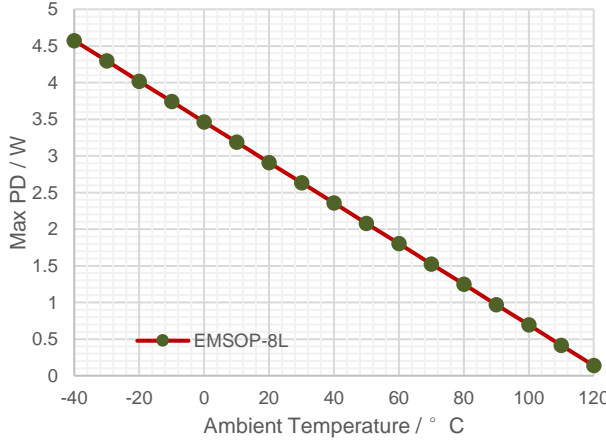


Figure 30. Maximum Allowed Power Dissipation vs Ambient Temperature, EMSOP-8L, $T_J \leq 125^\circ\text{C}$

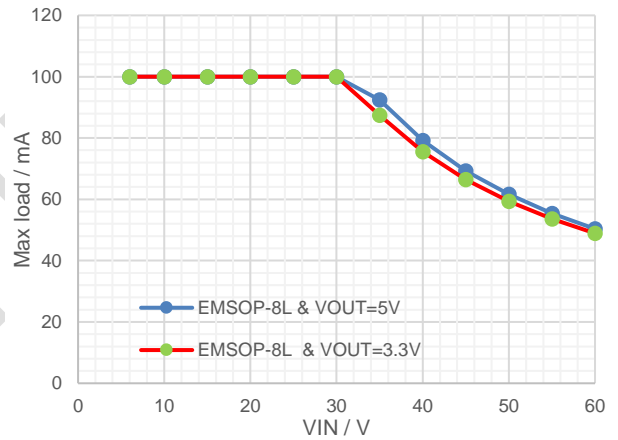


Figure 31. Maximum Output Current vs Input Voltage, EMSOP-8L, $T_J \leq 125^\circ\text{C}$

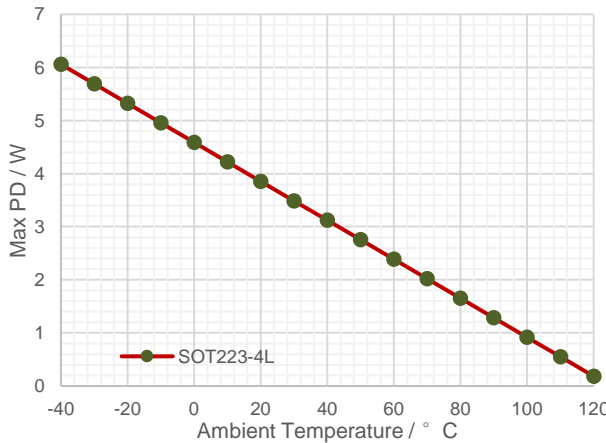


Figure 32. Maximum Allowed Power Dissipation vs Ambient Temperature, SOT223-4L, $T_J \leq 125^\circ\text{C}$

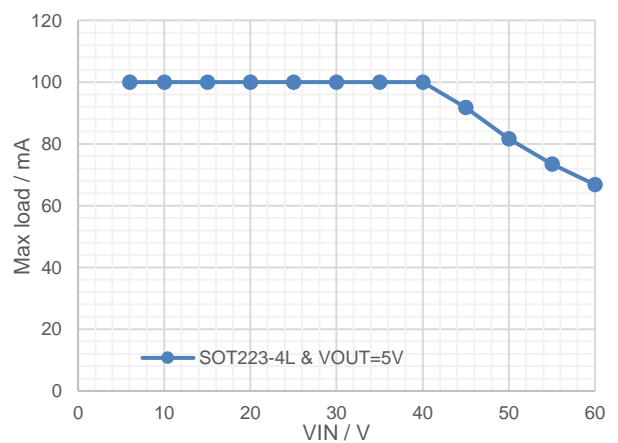


Figure 33. Maximum Output Current vs Input Voltage, SOT223-4L, $T_J \leq 125^\circ\text{C}$

Application Waveforms

Vin=Vout +1V, unless otherwise noted

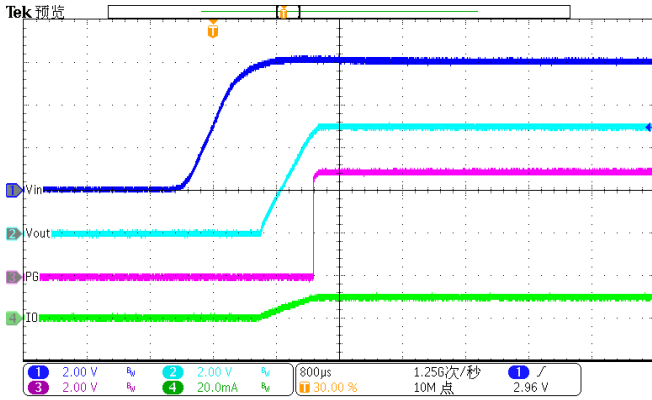


Figure 34. Power up (Iload=10mA)

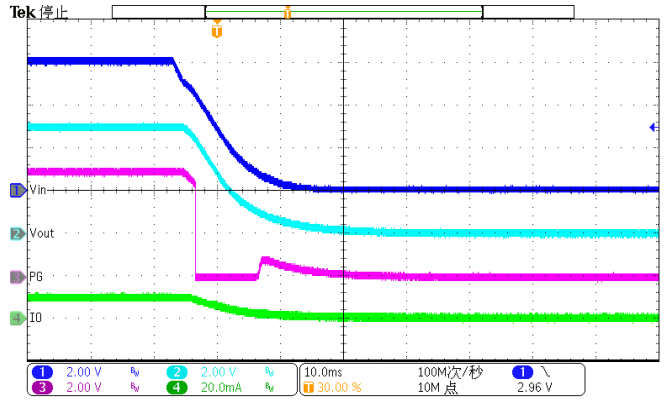


Figure 35. Power down (Iload=10mA)

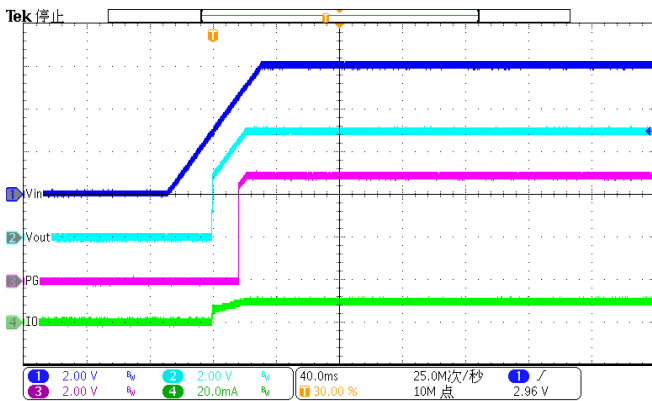


Figure 36. Slow Power up (Iload=10mA)

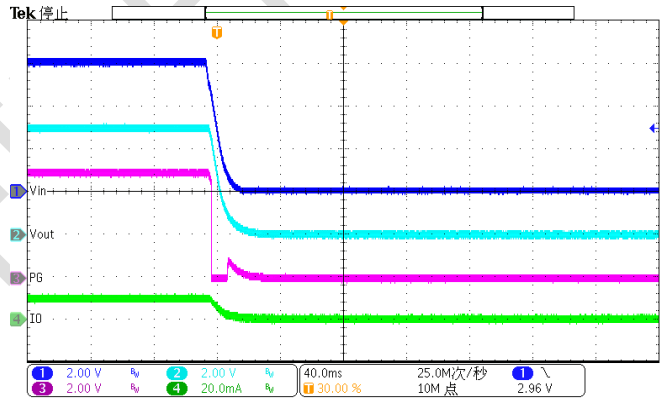


Figure 37. Slow Power down (Iload=10mA)

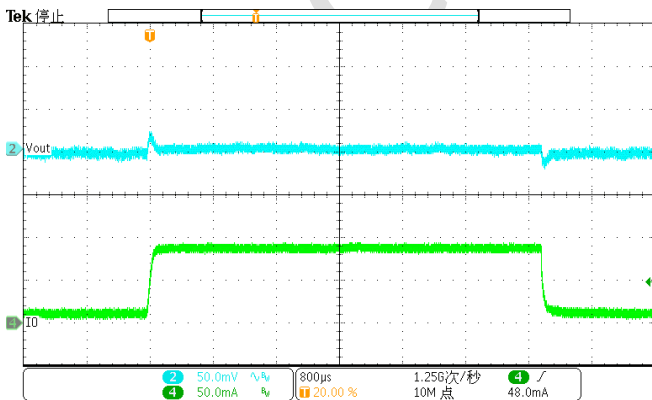


Figure 38. DC-DC Load Transient
(10mA-90mA), VOUT=5V

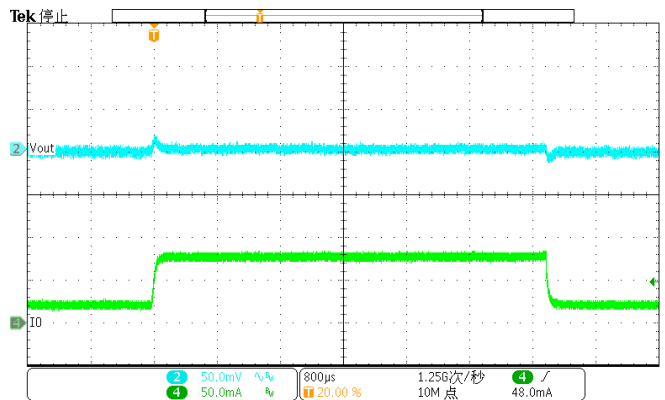


Figure 39. DC-DC Load Transient
(25mA-75mA), VOUT=5V

SCT71601Q Series

Application Waveforms(Continued)

Vin=Vout +1V, unless otherwise noted

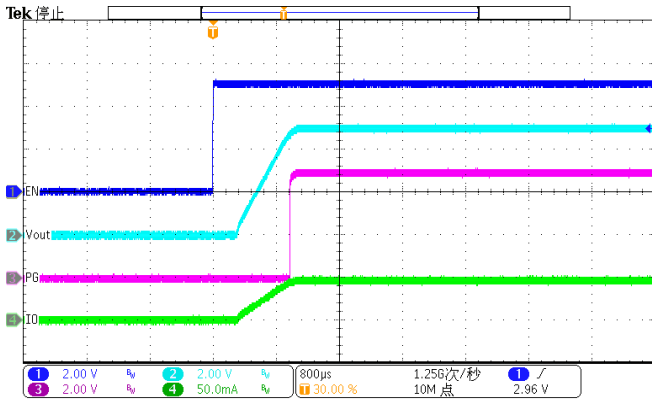


Figure 40. Enable (Iload=50mA)

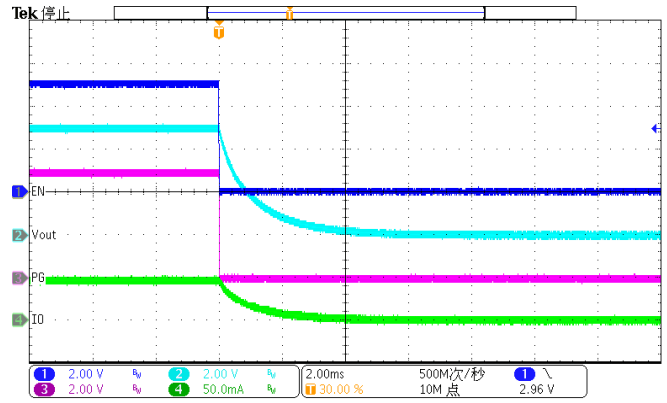


Figure 41. Disable (Iload=50mA)

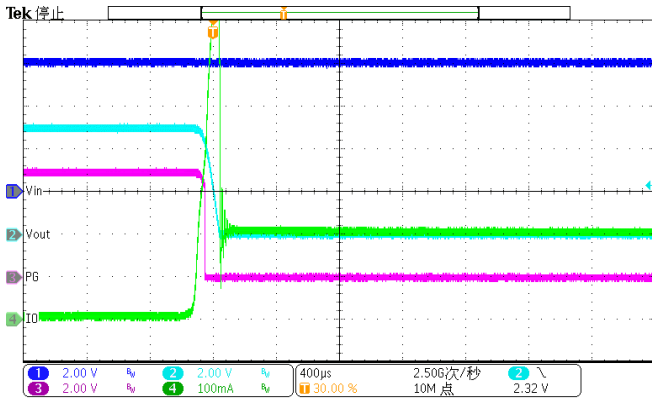


Figure 42. Enter Short Circuit Protection

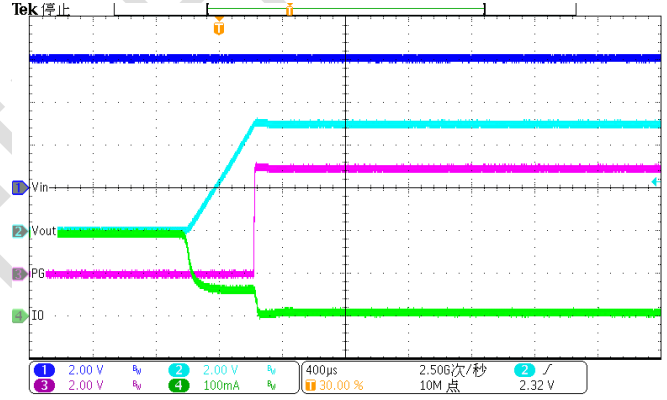


Figure 43. Exit Short Circuit Protection

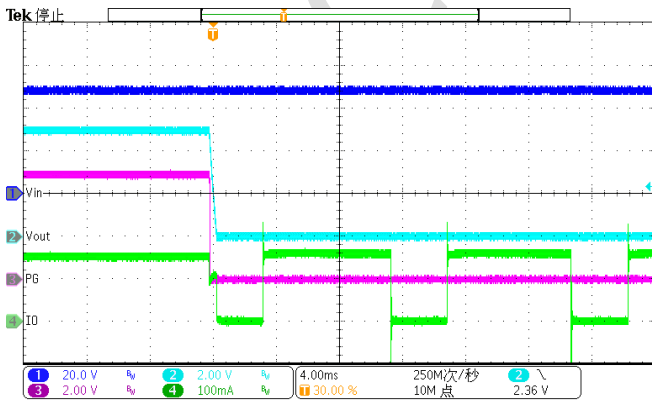


Figure 44. Enter Over Temperature Protection(Vin=48V)

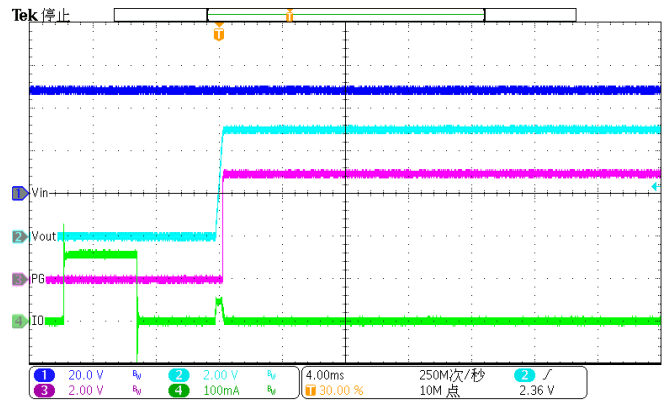


Figure 45. Exit Over Temperature Protection(Vin=48V)

Layout Guideline

Proper PCB layout is a critical for SCT71601Q's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a $0.1\mu\text{F}$ bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize $I \times R$ drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a $10\mu\text{F}$ low ESR capacitor parallel connection with the large electrolytic capacitor.

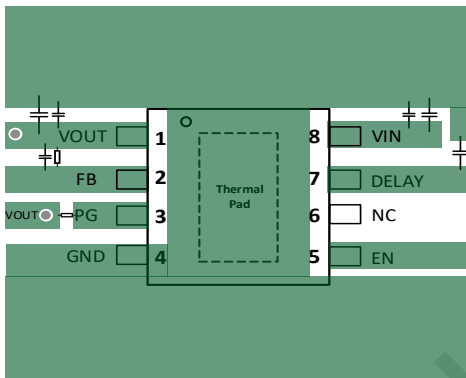


Figure 46. PCB Layout Example

SCT71601A00QMTER

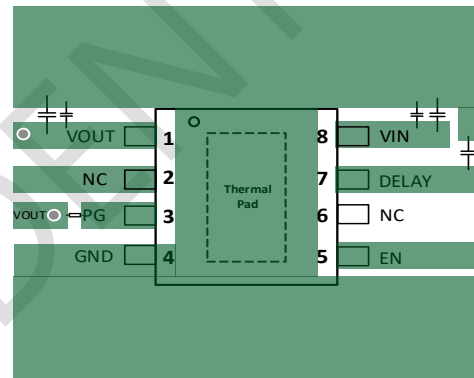


Figure 47. PCB Layout Example

SCT71601FxxQMTER

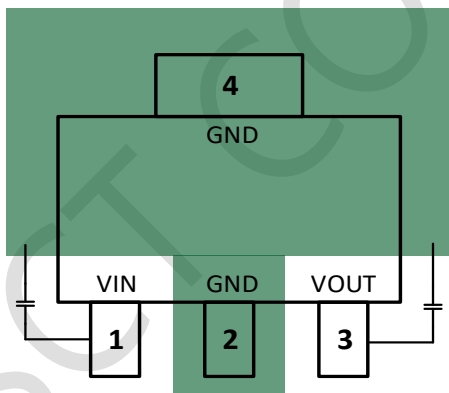


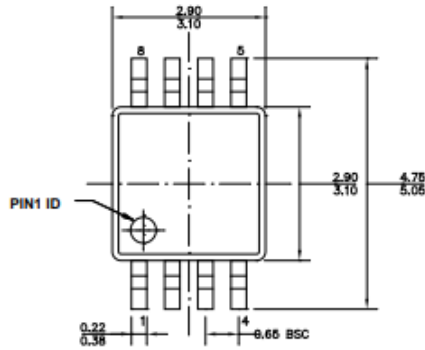
Figure 48. PCB Layout Example

SCT71601F50QTXER

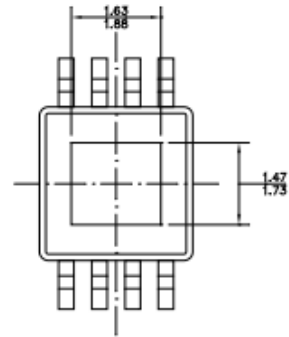
SCT71601Q Series

PACKAGE INFORMATION

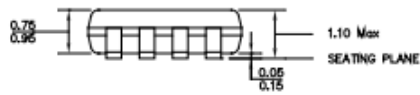
PACKAGE OUTLINE DRAWING FOR MSOP8L-EP POD-0050 Revision 0.0



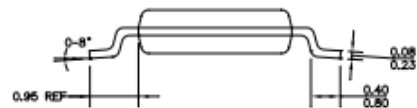
TOP VIEW



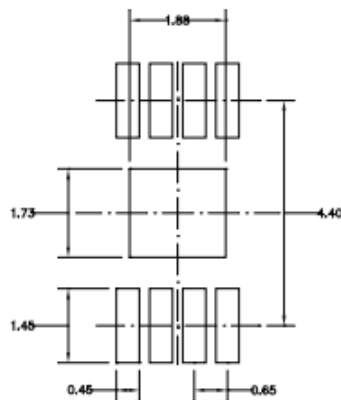
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) DRAWING MEETS JEDEC MO-187, VARIATION BA.
- 4) DRAWING IS NOT TO SCALE.

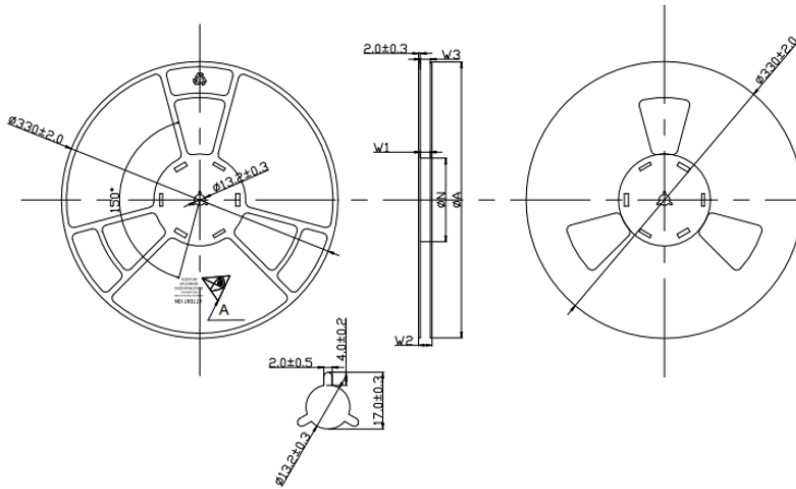
EMSOP-8L Package Outline Dimensions

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SCT71601Q Series

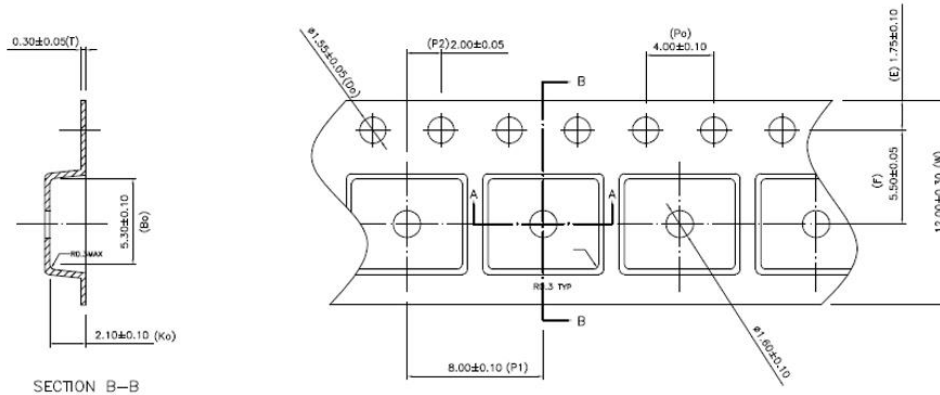
TAPE AND REEL INFORMATION



注意:

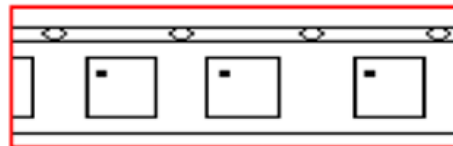
1. 材料: 聚苯乙烯;
2. 平整度: 最大允许3毫米;
3. 所有尺寸为毫米;
4. 表面电阻: $10E5 \sim 10E11$ OHMS/SQ (除了16mm width的卷盘在温度 $25^{\circ}C \pm 5^{\circ}$ 以及湿度为50%RH~60%RH条件下, 表面电阻满足 $10^5 \sim 10^9$ ohm范围内)
5. 所有未标注公差: ± 0.5
6. 卷盘不可错位, 可通过检验两个盘上A处的印字是否对应判断。

PRODUCT SPECIFICATIONS					
TYPE WIDTH	ϕA	ϕN	$W1(+tol)$	$W2(Max)$	$W3(Max)$
12MM	330 ± 2.0	100 ± 1.0	12.4	18.4	11.9/15.4



NOTES:

- 1.10 sprocket hole pitch cumulative tolerance ± 0.2
- 2.Camber not to exceed 1mm in 100mm.
- 3.Material: Black conductive Polystyrene.
- 4.Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
- 5.Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- 6.Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
- 7.Pocket center and pocket hole center must be same position.

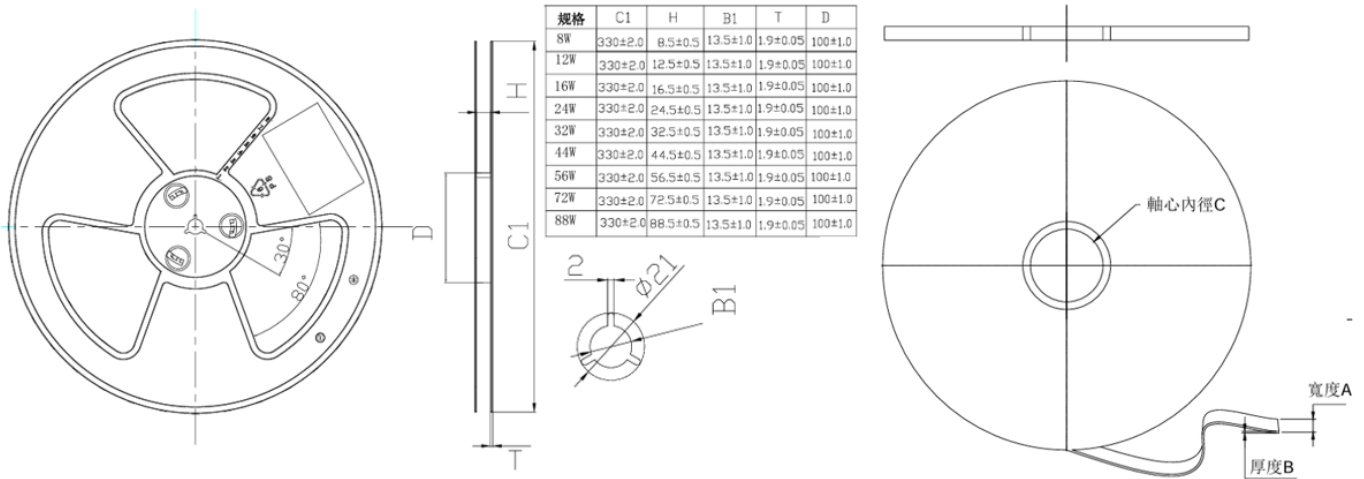


User Direction of Feed

EMSOP-8L

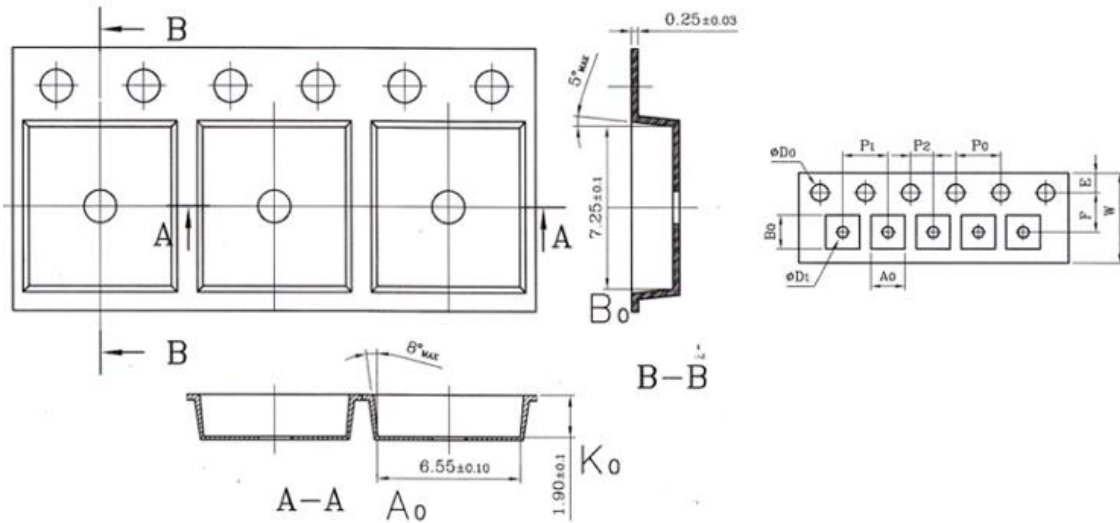
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TAPE AND REEL INFORMATION

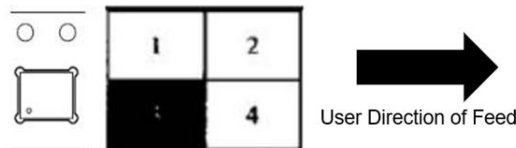


产品尺寸规格				(UNIT:mm)			
规格	A	B	C				
尺寸	9.50±0.1	0.061±0.005	76.5±0.2				

产品尺寸规格										(UNIT:mm)		
规格	W	P1	E	F	D0	D1	P0	P2	10P0			
尺寸	12 ^{+0.3} / _{-0.1}	8.0±0.1	1.75±0.1	5.5±0.05	1.5 ^{+0.1} / ₋₀	1.5 ^{+0.25} / ₋₀	4±0.1	2±0.05	40±0.2			
规格	A0	A1	B0	B1	K0	K1	T					
尺寸	6.55±0.1		7.25±0.1		1.90±0.1		0.25±0.03					



Pin1 dot located at Q3



SOT223-4L

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