80V Input, 100mA Output Current, Low Quiescent Current LDO

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
- - Device Temperature Grade 1: -40°C to 125°C
- Wide Input Range: 3V-80V
- Maximum Output Current: 100mA
- Adjustable Voltage: 1.2V-30V
- Output Voltage Accuracy:
  - T_J= 25℃：±1%
  - T_J= -40℃~ 125℃：±2%
- Low Quiescent Current: 4 uA
- Ultra-Low Shutdown Current: 0.35uA
- Low Dropout Voltage：
  - 60mV at 20mA load current
  - 340mV at 100mA load current
- 770us Internal Soft-start Time
- Integrated Short-Circuit Protection with OCFB (Over Current Fold-back) Feature
- Enable pin is available
- Over-Temperature Protection
- Active Output Discharge
- Available Package: EMSOP-8L

APPLICATIONS

- Emergency Call (eCall)
- Battery Management System (BMS)
- On-Board Charger (OBC) and wireless charger
- DC/DC converter

DESCRIPTION

The SCT71801A00Q product is a low-dropout linear regulator designed to operate with a wide input-voltage range from 3 V to 80 V and 100mA output current with Enable control(EN) and an integrated open-drain, active-high, power-good output (PG) with a user programmable delay.

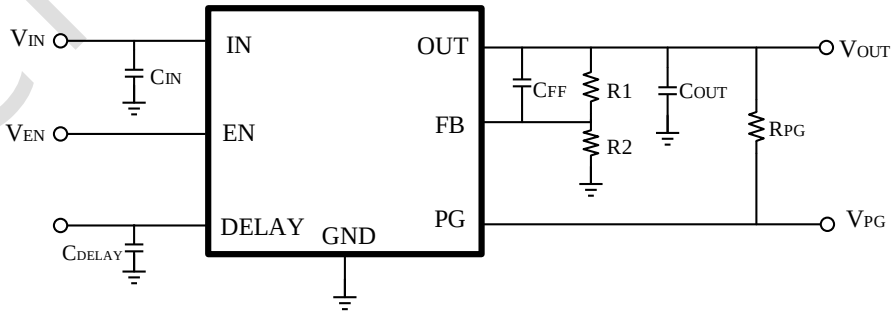
Only 4-μA typical quiescent current at light load makes the SCT71801A00Q product ideal choices for portable devices with battery power supply and an optimal solution for powering microcontrollers (MCUs) and CAN/LIN transceivers in always-on systems.

The SCT71801A00Q product integrated short-circuit and overcurrent protection with OCFB (Over Current Fold-back) feature, which makes the device more reliable during transient high-load current faults or shorting events.

The SCT71801A00Q product could adjust output voltage version with 1.2V feedback voltage and have active output discharge.

The SCT71801A00Q product is available in EMSOP-8L packages, for other package options, please contact SCT sales.

TYPICAL APPLICATION



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Sampling.

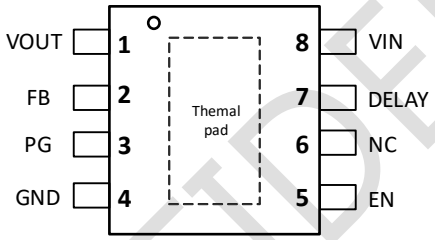
Revision 0.81: Update electricical characteristic and typical characteristic.

Revision 0.82: Update package information.

DEVICE ORDER INFORMATION

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
SCT71801A00QMTER	Adjust	EMSOP-8L	1A00Q	8	TBD	Tape & Reel, 4000

PIN CONFIGURATION



SCT71801A00QMTER

EMSOP-8L Package

PIN FUNCTIONS

EMSOP-8L/SCT71801A00Q:

NAME	NAME	PIN FUNCTION
1	VOUT	Regulated output voltage pin, A cap＞2.2uF must be tied from this pin to ground to assure stability.
2	FB	Feedback voltage pin.
3	PG	Power-good pin; Open-collector output; leave open or connect to GND if the power-good function is not needed.
4	GND	Ground reference pin.
5	EN	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_H}$, or EN is floating, the regulator is enabled. If $V_{EN} < V_{EN\_L}$, the regulator is disabled. EN pin can be connected to VIN. Make sure that $V_{EN} \leq$ VIN at all times.
6	NC	No connection.
7	DELAY	Power-Good Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
8	VIN	Input voltage pin. A cap＞0.1uF must be tied from VIN to GND.

9	Thermal Pad	Connect the thermal pad to a large area GND plane for improved thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3	80	V
V_{OUT}	Output voltage range	1.2	30	V
V_{EN}	Enable input voltage	0	V_{IN}	V
V_{PG}	Power-good pin voltage	0	5.5	V
DELAY	Programmable Power-Good Delay Time.	0	5	V
C_{IN}	Input capacitor	2.2	--	uF
C_{OUT}	Output capacitor	2.2	220	uF
ESR	Output capacitor ESR requirements	0.001	5	Ω
T_J	Operating junction temperature	-40	125	°C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (1)

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range	-0.3	90	V
V_{OUT}	Maximum output voltage range	-0.3	35	V
V_{FB}	Maximum feedback pin voltage	-0.3	6.6	V
V_{EN}	Maximum enable input voltage	-0.3	V_{IN}	V
V_{PG}(2)	Maximum power-good pin voltage	-0.3	6.6	V
V_{PGDL}	Maximum power-good delay pin voltage	-0.3	5.5	V
T_J (3)	Junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) A current limit resistor should be connected between PG and the pulled-up power（eg. VOUT or other power supply）, When the pulled-up power is higher than 6V, the maximum Current Limit is better lower than 100uA to protect the Zener.
(3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-3	+3	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-1	+1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. Because they were simulated in accordance with JESD 51-7. They do not represent the performance obtained in an actual application. For design information see Power Dissipation and Thermal Performance section.

The value of $R_{\theta JA\_EVM}$ is the tested results based on our EVM, and is more useful for thermal design. Even if it still do not represent the thermal performance of customer's PCB design, but it was a good starting point for thermal performance design.

The PCB information of our EVM: 4-layer,1oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

The values given in this table are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB), thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the device. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual values of the below table.

PARAMETER	THERMAL METRIC	EMSOP-8L	UNIT
$R_{\theta JA}$ (1)	Junction to ambient thermal resistance	54.14	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.57	
Ψ_{JB}	Junction-to-board characterization parameter	19.28	
$R_{\theta JCtop}$ (2)	Junction to case thermal resistance	31.57	
$R_{\theta JA\_EVM}$(3)	junction to ambient thermal resistance	36.08	

(1) $R_{\theta JA}$ is junction to ambient thermal resistance, based on JESD51-7.

(2) $R_{\theta JC}$ is junction to case thermal resistance, based on JESD51-7.

(3) $R_{\theta JA\_EVM}$ is junction to ambient thermal resistance, which is tested on SCT EVM.

ELECTRICAL CHARACTERISTICS

V_{IN}=V_{OUT}+1V, C_{OUT}=10uF, T_J= -40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3		80	V
V_{UVLO}	V_{IN} UVLO Threshold	V_{IN} rising		2.65		V
	Hysteresis			145		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, V_{IN}=4.3V		0.35	0.65	μA
		EN=0, V_{IN}=48V		2.4	5	μA
I_Q	Quiescent current from GND pin	EN float, no load, V_{IN}=4.3V, T_J= 25°C		4	6	μA
		EN float, no load, V_{IN}=4.3V, T_J= -40°C~125°C			8.5	μA
		EN float, no load, V_{IN}=80V, T_J= 25°C		7.5	10	μA
		EN float, no load, V_{IN}=80V, T_J= -40°C~125°C			14	μA
Regulated Output Voltage and Current						
V_{FB}	Feedback voltage accuracy	T_J= 25°C	1.188	1.2	1.212	V
		T_J= -40°C~125°C	1.176		1.224	V
ΔV_{OUT}	Line regulation	V_{IN}=V_{OUT}+1V to 80V		1	55	mV
	Load regulation	Iout=10uA to 100mA		6	25	mV
V_{DROP}	Dropout voltage(1)	V_{IN}=V_{OUT}-0.1V ,Iout =20mA		60		mV
		V_{IN}=V_{OUT}-0.1V ,Iout =100mA		340		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		100	mA
I_{OC}	Output current limit			200		mA
I_{OCFB}	Over Current Fold-back	T_J= 25°C		100		mA
PSRR	Power supply rejection ratio(2)	V_{OUT} =1.8V, Iout=10mA , f=1kHz, C_{OUT}=10μF		73		dB
		V_{OUT} =1.8V, Iout=10mA , f=10kHz, C_{OUT}=10μF		59		dB
		V_{OUT} =1.8V, Iout=10mA , f=100kHz, C_{OUT}=10μF		51		dB
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.0		V
V_{EN_Hys}	Enable threshold hysteresis			200		mV
I_{EN_0V}	Enable pin pull-up current	EN=0V		0.2		μA
T_{SS}	Soft-start time			770		us
Over Voltage Protection						
OVP_H	overshoot of Vout when discharge occur			115%		
OVP_L	overshoot of Vout when discharge disappear			110%		
OVP_{Hys}	overshoot of Vout hysteresis			5%		
Power Good						
V_{PG_R}	PG rising threshold percentage	V_{OUT}/$V_{OUT(NOM)}$,when V_{OUT} rising		90%		

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} falling		87%		
V_{HYS}	PG trip hysteresis			3%		
V_{PG_LOW}	PG output low voltage	V_{OUT}=0.8x$V_{OUT(NOM)}$,PG sink 100uA		76		mV
R_{GR}	PG pull down resistor	R_{GR} = VPG_LOW /0.1mA		150		Ω
I_{PG_LKG}	PG leakage current	$V_{OUT(NOM)}$, V_{OUT} in regulation			0.2	uA
I_{PGDL}	PGDL charging current(3)	T_J= 25°C		1	2	uA
Thermal Protection						
T_{SD}	Thermal shutdown threshold(4)	T_J rising Hysteresis		170 15		°C °C

(1) The dropout voltage is defined as V_{IN}-V_{OUT}, when force V_{IN} is 100mV below the value of V_{OUT} for V_{IN}=$V_{OUT(NOM)}$+1V.
(2) PSRR is derived from bench characterization, not production test.
(3) I_{PGDL} will have updated to 1uA when this product has released to production.
(4) Thermal shutdown threshold is derived from bench characterization, not production test.

TYPICAL CHARACTERISTICS

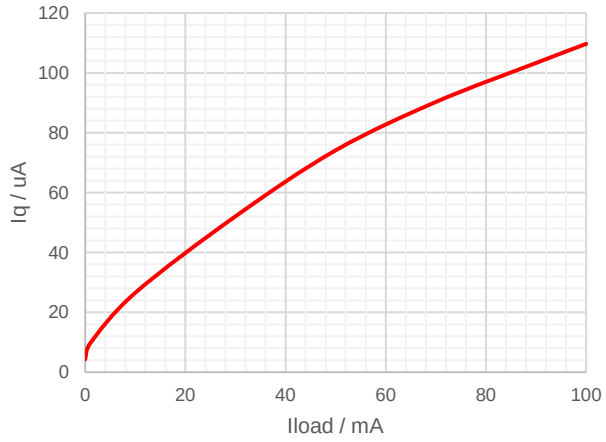


Figure 1. Quiescent Current vs Output Current

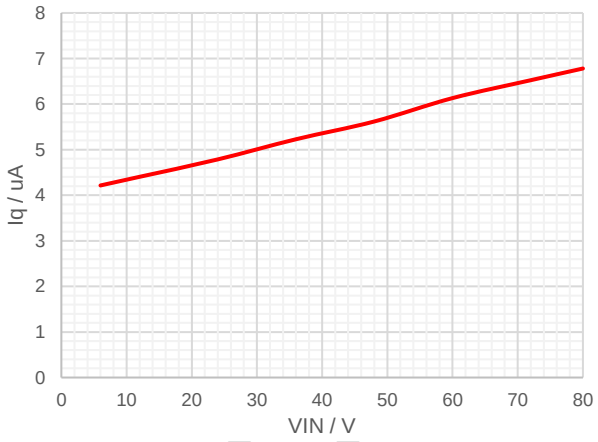


Figure 2. Quiescent Current vs Input Voltage, No load

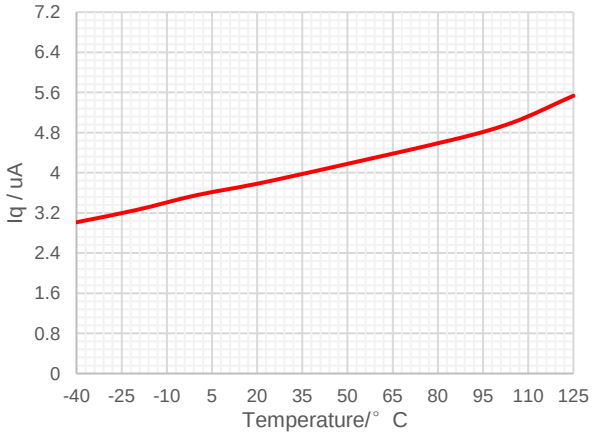


Figure 3. Quiescent Current vs Ambient Temperature

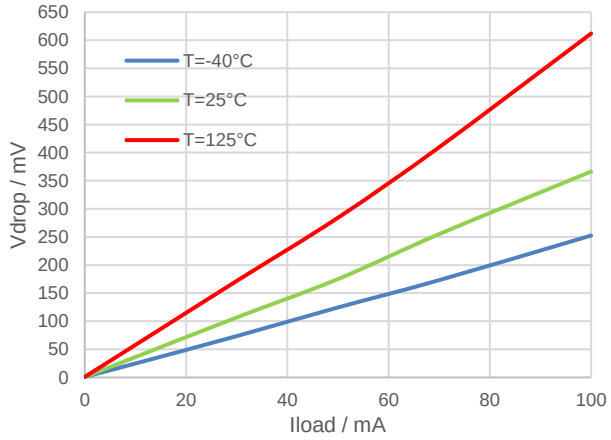


Figure 4. Dropout Voltage vs Output Current

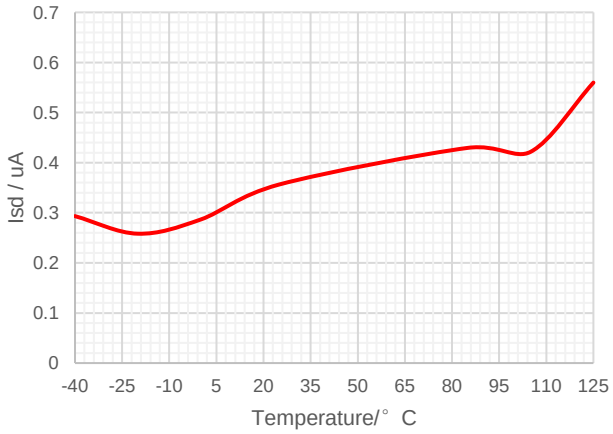


Figure 5. Shutdown Current vs Ambient Temperature

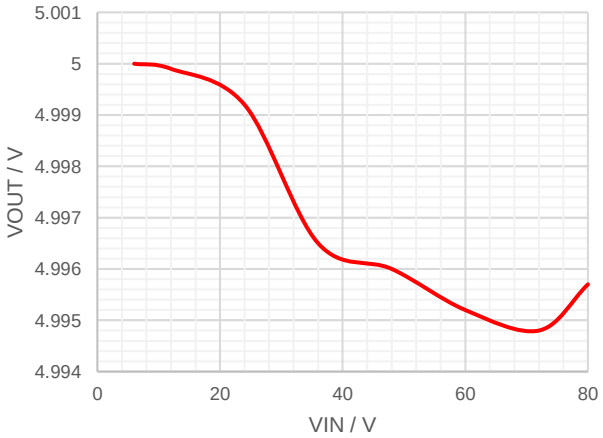


Figure 6. Output Voltage vs Input Voltage

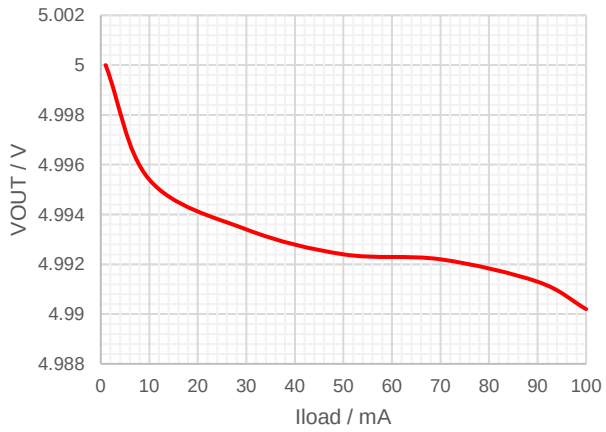


Figure 7. Output Voltage vs Output Current

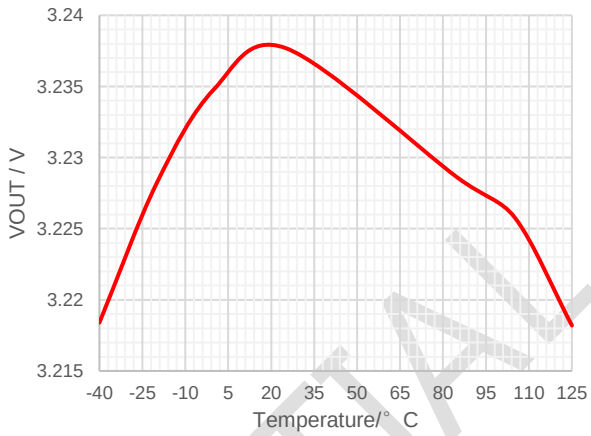


Figure 8. Output Voltage vs Ambient Temperature at VOUT=3.3V

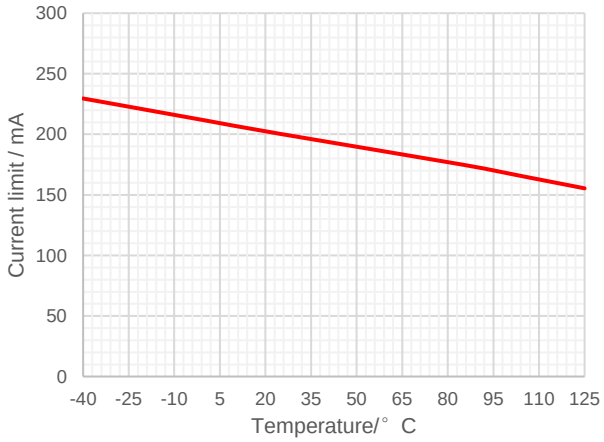


Figure 9. Output Current Limit vs Ambient Temperature at VIN<55V

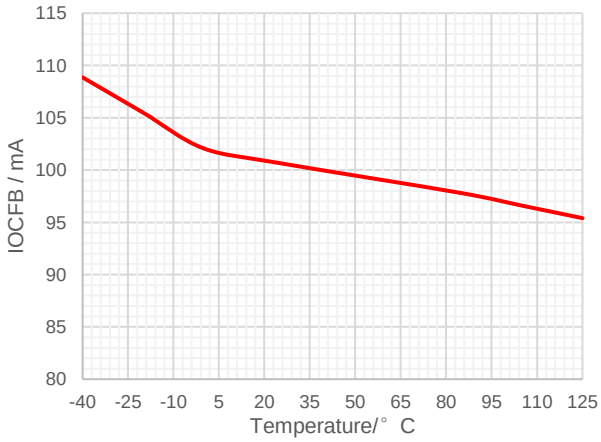


Figure 10. Output Current Limit vs Ambient Temperature at VIN≥55V

TYPICAL CHARACTERISTICS (continued)

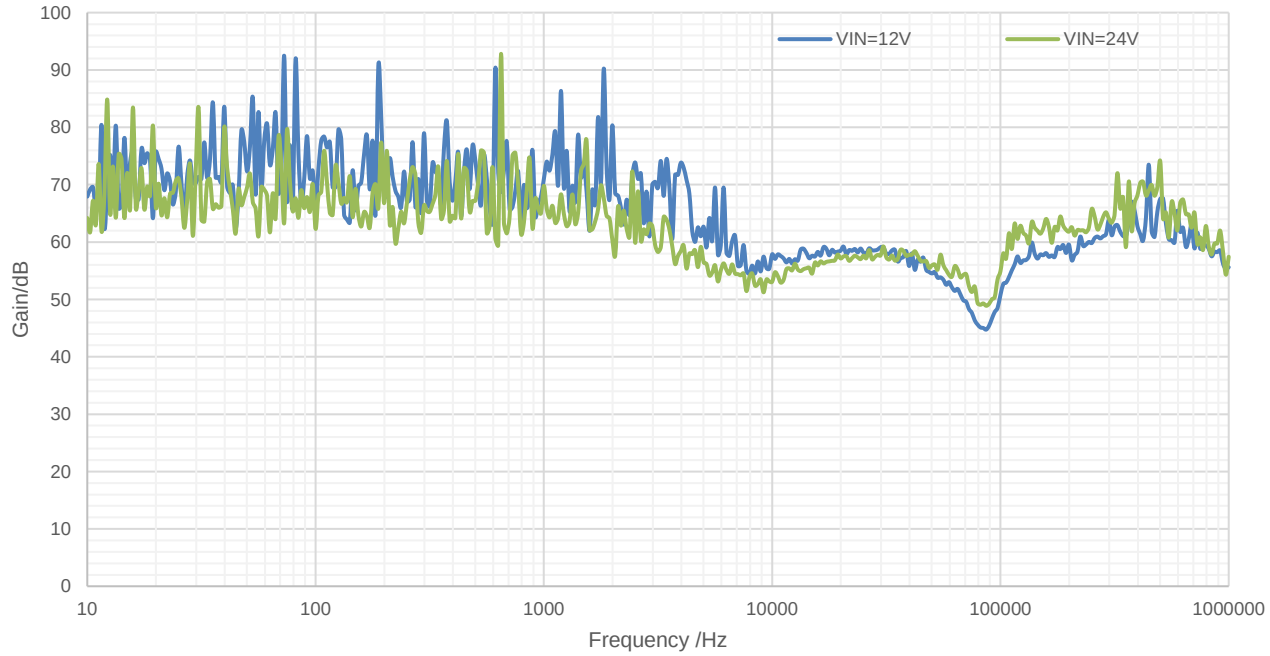


Figure 11. PSRR vs Frequency
VOUT=3.3V,Cf=10pF,COUT=10uF,IOUT=10mA

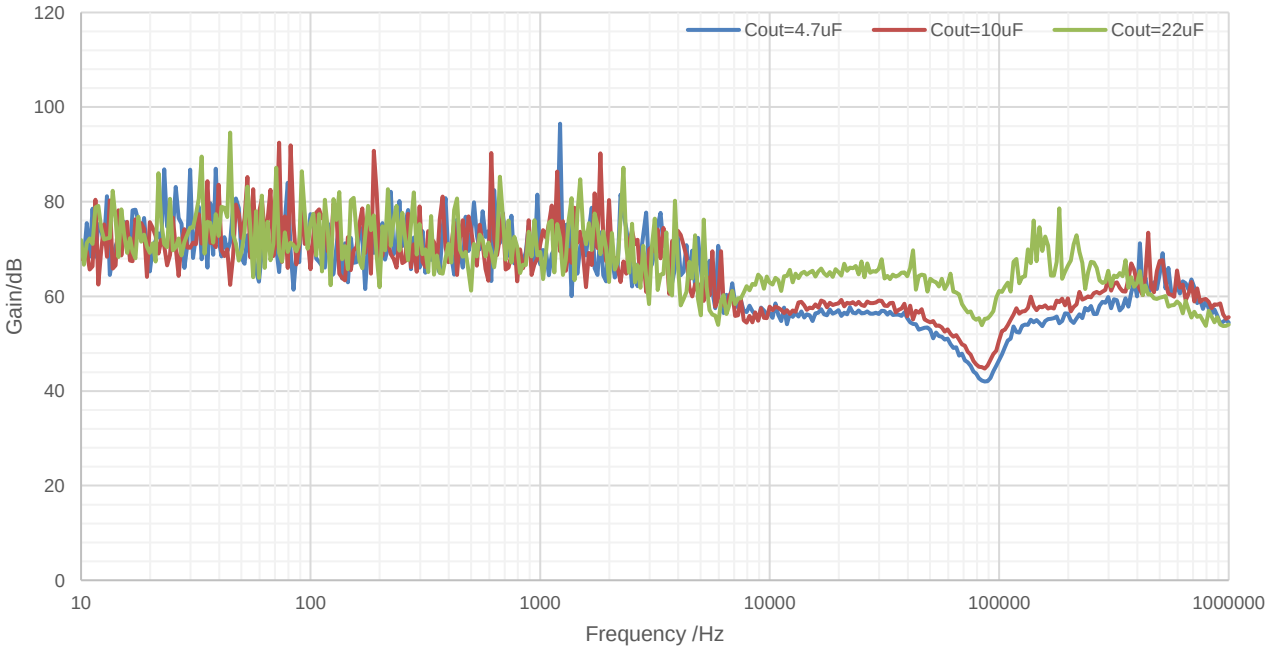


Figure 12. PSRR vs Frequency
VIN=12V,VOUT=3.3V,Cf=10pF,IOUT=10mA

TYPICAL CHARACTERISTICS (continued)

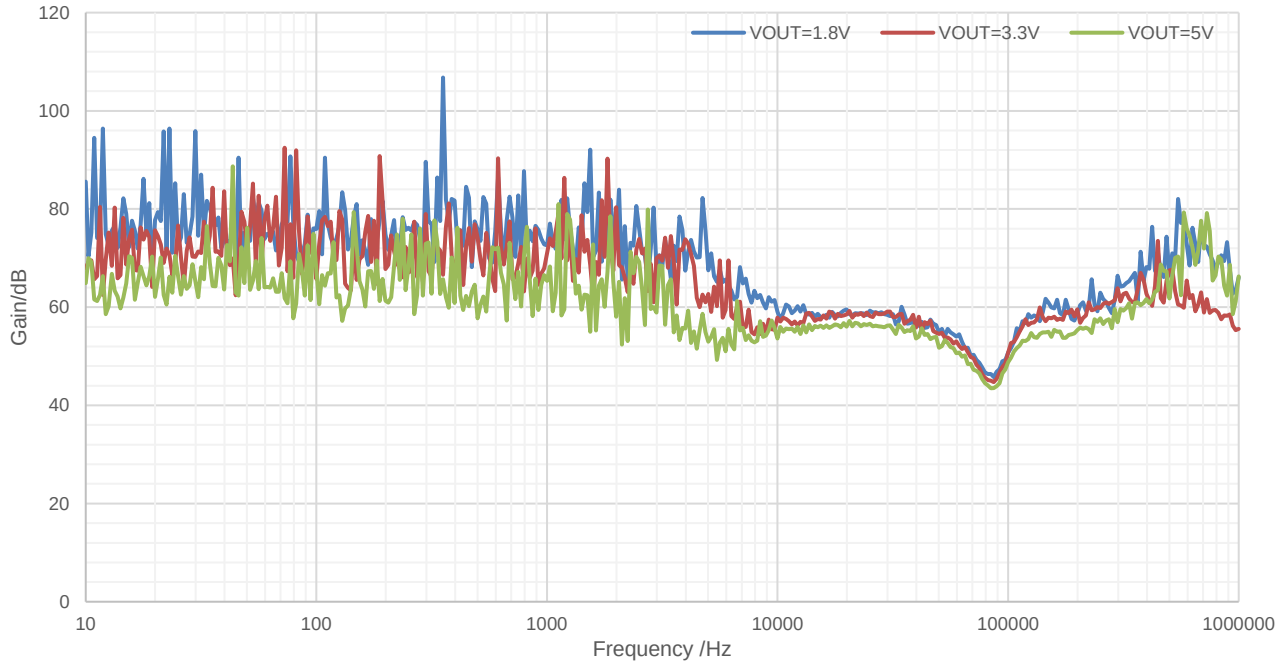


Figure 13. PSRR vs Frequency
VIN=12V, Cf=10pF,COUT=10uF,IOUT=10mA

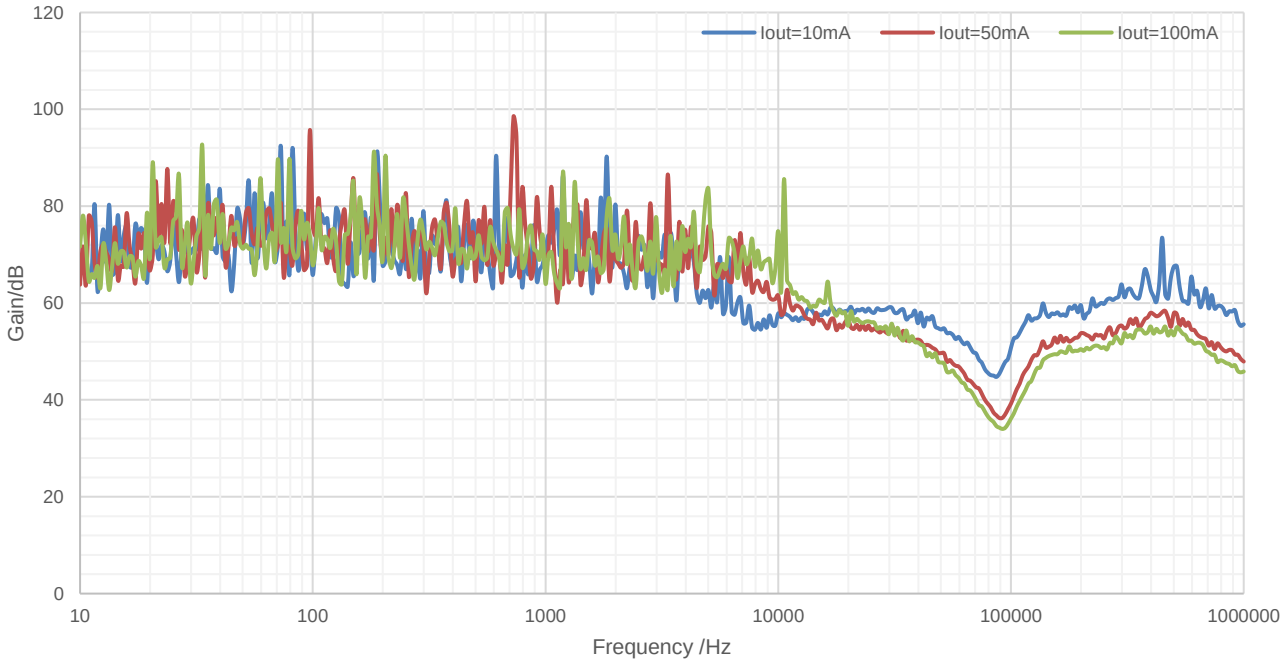


Figure 14. PSRR vs Frequency
VIN=12V,VOUT=3.3V,Cf=10pF,COUT=10uF

FUNCTIONAL BLOCK DIAGRAM

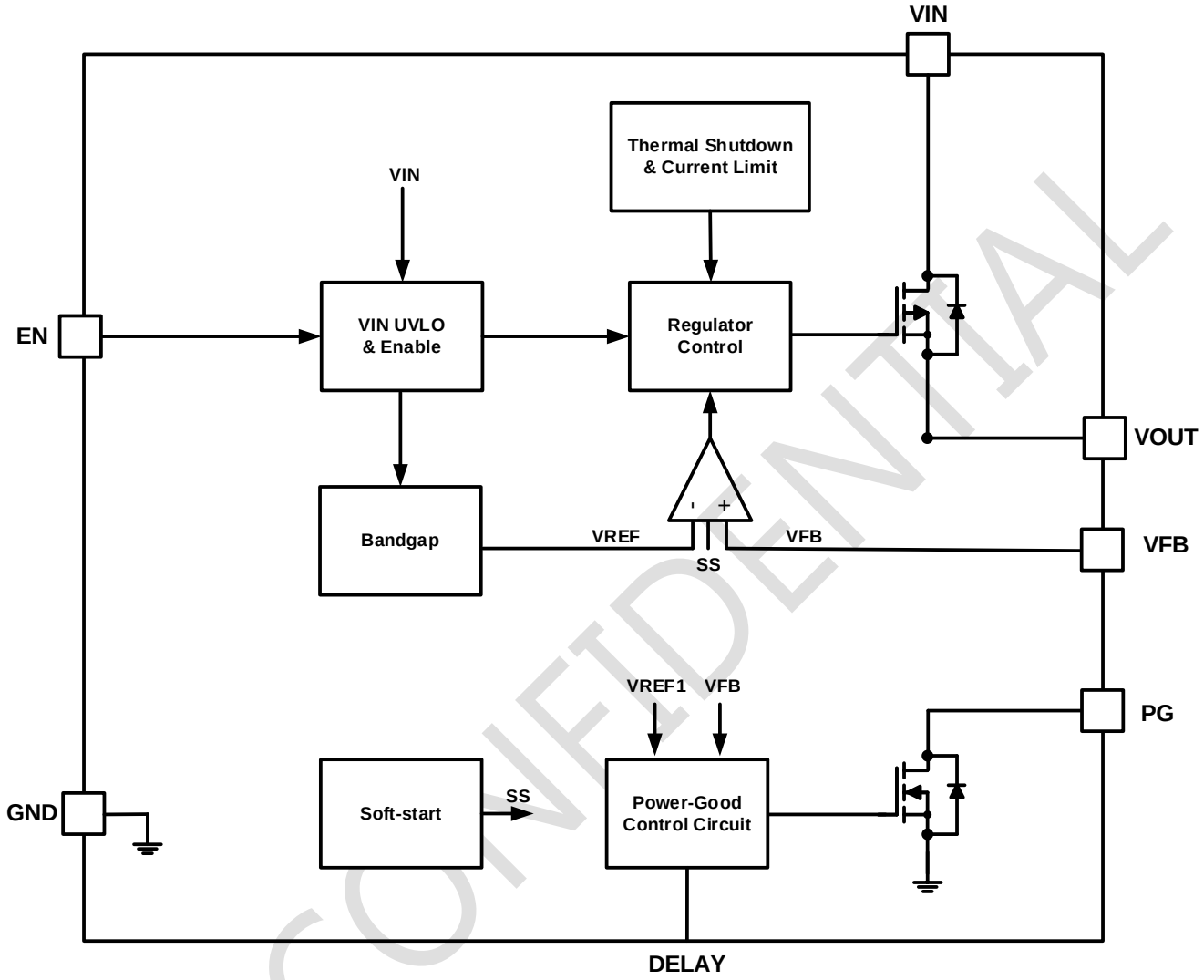


Figure 15. Functional Block Diagram of Adjust Output Version

OPERATION

Overview

The SCT71801A00Q series products are 100mA wide input voltage range linear regulators with very low quiescent current. These voltage regulators operate from 3V to 80V DC input voltage and consume 4μA quiescent current at no load.

The SCT71801A00Q series products is stable with 3.3uF~220uF output capacitors, and 10uF ceramic capacitor is recommended. An internal 770us soft-start time avoids large inrush current and output voltage overshoot during startup.

The SCT71801A00Q series products also provide enable control, Power-Good feature and programmable Power-Good delay time which is very suitable for the applications needing sequence configuration. Other protection features include the VIN input under-voltage lockout, over current protection, output hard short protection and thermal shutdown protection.

The SCT71801A00Q series products provide adjustable output version from 1.2V to 30V. If you need a new output voltage version or a new package option, please feel free to contact SCT sales.

Enable and Under Voltage Lockout Threshold

The SCT71801A00Q series products is enabled when the VIN pin voltage rises above 2.65V and the EN pin voltage exceeds the enable threshold V_{EN_H}. The device is disabled when the VIN pin voltage falls below 2.65V or when the EN pin voltage is below V_{EN_L}. Internal pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) from VIN to GND shown in Figure 11. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$VIN_{rise} = V_{EN\_H} * \frac{R1 + R2}{R2} \quad (1)$$

$$VIN_{hys} = (V_{EN\_H} - V_{EN_L}) * \frac{R1 + R2}{R2} \quad (2)$$

Where

VIN_{rise}: Vin rise threshold to enable the device

VIN_{hys}: Vin hysteresis threshold

I_1=0.2uA and could be neglected in the calculation

V_{EN_H}=1.2V

V_{EN_L}=1.0V

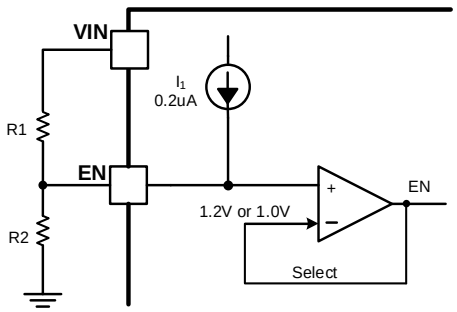


Figure 16. System UVLO by enable divide

Regulated Output Voltage

When the input voltage is higher than $V_{OUT(NOM)}$+V_{DROP}, output pin is the regulated output based on the required voltage version. When the input voltage falls below $V_{OUT(NOM)}$+V_{DROP}, output pin tracks the input voltage minus the dropout voltage based on the load current.When the input voltage drops below UVLO threshold, the output keeps shut off.

Over Current Limit and Foldback Current Limit

The SCT71801A00Q series products has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is 200mA when VIN<VIN_HIGH, but SCT71801A00Q supplies a fold-back current limit 100mA when VIN> VIN_HIGH.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the regulator begins to heat up because of the increase in power dissipation. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition persists, the device cycles between current limit and thermal shutdown.

With the over current VIN_HIGH Control feature, the SCT71801A00Q series products would be more robust and safer when over current faults and shorting events occur. But it also requires the maximum loading current should be smaller than Isc during startup. The characteristic is shown in the following figure.

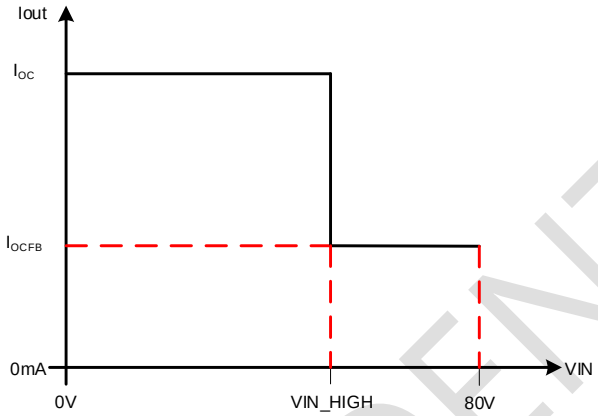


Figure 17. Current Limit with Foldback Feature

Internal Soft-Start

The SCT71801A00Q series products integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.2V reference voltage in 770us. If the EN pin is pulled below 1V, LDO will be shut off and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Below figure shows the startup waveform at small output capacitor and large output capacitor. When output capacitor is small, for example 10uF, the slope of VOUT is limit by soft-start. When output capacitor is large, for example 100uF, the slope of VOUT is limited by current limit (I_{OC}) at VIN< VIN_HIGH, and the slope of VOUT is limited by current limit (I_{OCFB}), when VIN> VIN_HIGH.

In SCT71801A00Q series products, typical Tss is 770us, and typical I_{OC} is 200mA and typical I_{OCFB} is 100mA, could use the following formula for initial startup time calculation.

$$\text{Tstart} = \max\left\{\frac{C_{OUT}\times V_{OUT}}{(I_{sc}-I_{load})}, T_{SS}\right\} \quad (3)$$

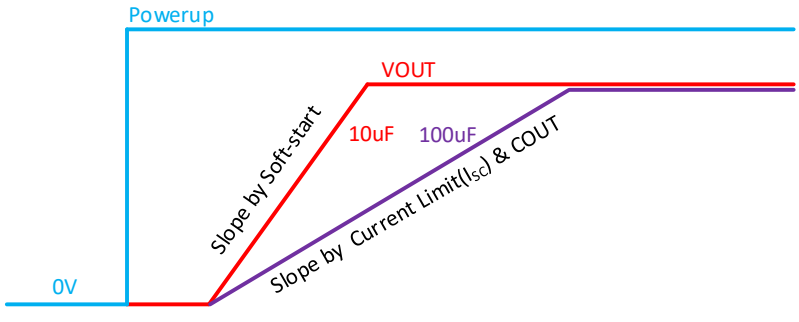


Figure 18. Soft-start Waveform vs Output Capacitor

Power-Good and Power-Good Delay

The power-good (PG) pin is an open-drain output and can be connected to any 6V or lower rail through an external pull-up resistor. The PG output is high-impedance when VOUT is greater than the PG trip threshold (V_{PG_R}=90% x $V_{OUT(NOM)}$). If VOUT drops below V_{PG_F}=87% x $V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

If the power-good delay time is not enough for some application, could connect a external capacitor from DELAY pin to GND, this capacitor is charged from 0 V to 1.2 V by the DELAY pin current(I_{DELAY}) and generate extra delay time. When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}. The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY}= 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.2V) / 1μA = 12 ms.

To ensure proper operation of the power-good feature, maintain VIN≥ 3V (VIN_MIN). It allows connections of PG pin to circuit with the same or different power supply voltage to the LDO's VOUT level. Below are the connections examples.

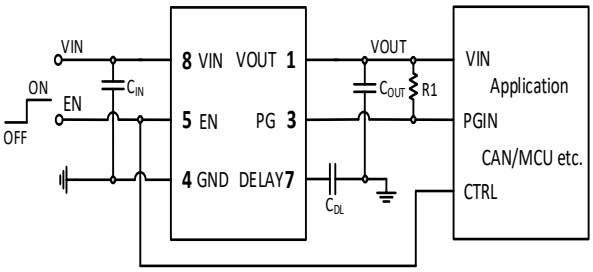


Figure 19. PG Connected to LDO's Ouput

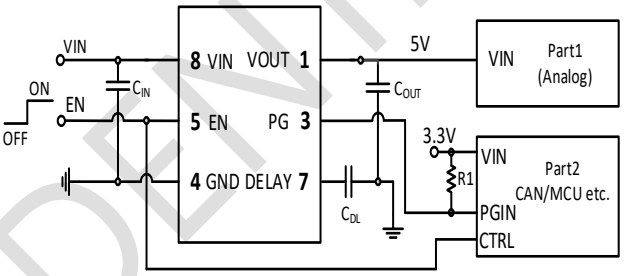


Figure 20. PG Connected to the other Power Supply

Below figure shows the startup and shutdown situation when slow power up and power down.

At the point 0, the input voltage starts to rise from 0 to 2.65 V, LDO is in shutdown (because VIN is below its UVLO threshold) and output voltage is 0V.

At the point 1, the VIN voltage reaches UVLO threshold level and LDO starts charging of output capacitor. VOUT rising speed is defined by internal soft-start function.

At the point 2, the VOUT voltage reaches almost the VIN voltage as it rises faster and LDO gets into dropout region. The difference between VIN and VOUT is the dropout voltage.

At the point 3, the VOUT reaches PG threshold (V_{PG_R}=90% x $V_{OUT(NOM)}$) and from this point LDO counts the power good delay time. After this delay, the PG pin rises to high level showing that VOUT is ok.

At the point 4, the VOUT reaches its nominal value (5.0V version) as the VIN starts to be higher than ($V_{OUT(NOM)}$ + V_{DROP}) and LDO gets into regulation region.

At the point 5, as the VIN voltage slow power down and LDO returns to dropout region again.

At the point 6, the VOUT drops below PG threshold (V_{PG_F}=87% x $V_{OUT(NOM)}$) and LDO starts counting the power good deglitch time, which filters fast VOUT undershoots (caused for example by line/load transient responses). After this delay, the PG output is shorted to 0 V level to highlight "power fail" state.

At the point 7, the VIN voltage is lower than input voltage UVLO threshold minus UVLO hysteresis level and LDO goes into the shutdown state.

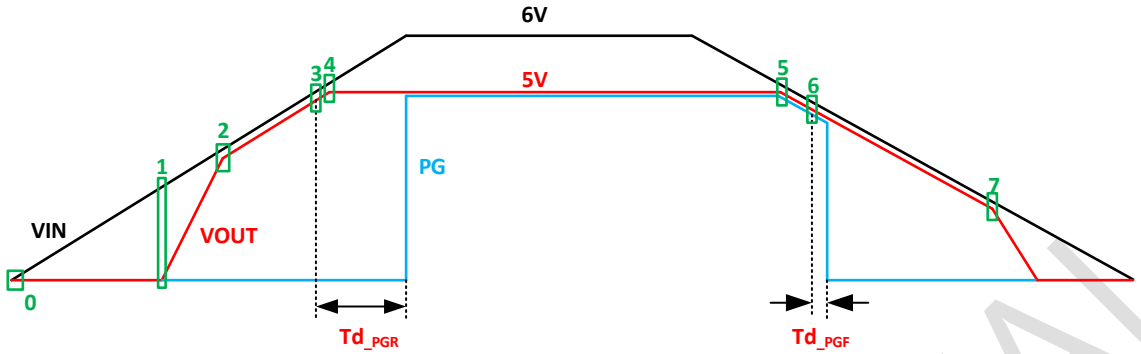


Figure 21. Startup and Shutdown Example —SCT71801A00Q Series

Thermal Shutdown

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

APPLICATION INFORMATION

Typical application 1:

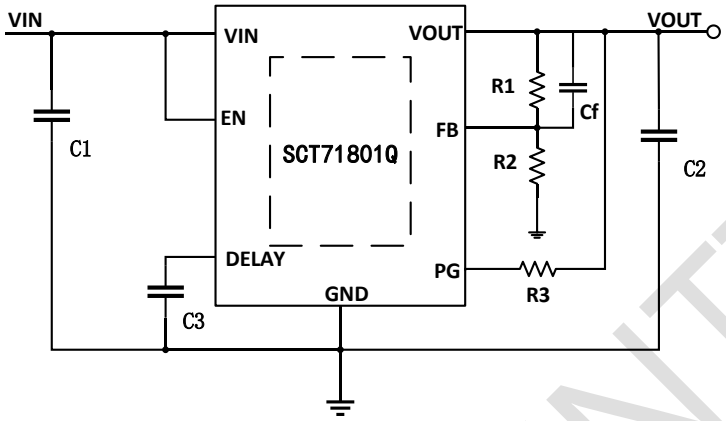


Figure 22. SCT71801A00Q Typical Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~80V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C_2)	2.2uF~220uF , recommends 10uF
Input Capacitor Range (C_1)	≥2.2uF , recommends 10uF
Pull-up resistor of power-good (R3)	>100kΩ

Typical application 2:

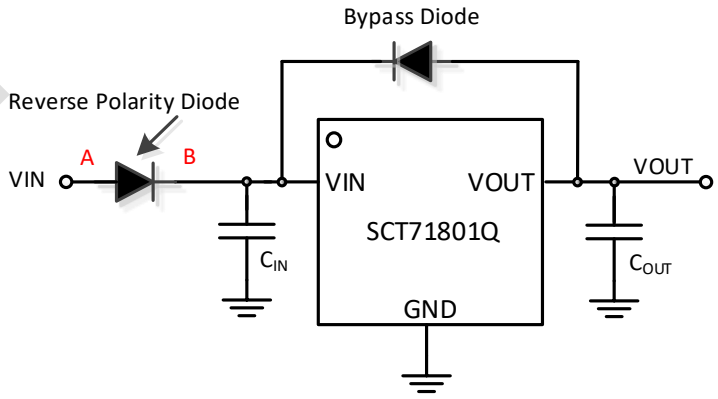


Figure 23. SCT71801A00Q Typical Application Schematic with Reverse Polarity Diode

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~80V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C_{OUT})	2.2uF~220uF , recommends 10uF
Input Capacitor Range (C_{IN})	≥2.2uF , recommends 10uF

In some applications, the VIN and the VOUT potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flowing backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220μF. Also by inserting a reverse polarity diode in series to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

Typical application 3:

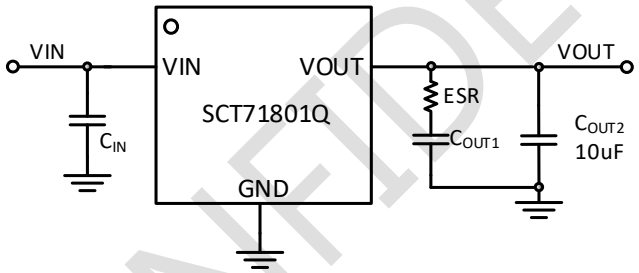


Figure 24. SCT71801A00Q Typical Application Schematic with Large Output Capacitor

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal, 3V~80V
Output Voltage	5V or 1.2V~30V
Maximum Output Current	100mA
Output Capacitor Range (C_{OUT1} and ESR)	2.2uF~220uF with ESR=0.5Ω~5Ω
Output Capacitor Range (C_{OUT2})	recommends 10uF with low ESR
Input Capacitor Range (C_{IN})	≥2.2uF , recommends 10uF

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 100kΩ. Use equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 1.2V

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

Vout/V	COUT/uF	Cf/pF	R1/kΩ	R2/kΩ	COUT1/uF (optional)	ESR/Ω
1.8	10	33	51.1	100	220	1
2.5	10	33	107	100	220	1
3.3	10	33	174	100	220	1
5	10	33	316	100	220	1
12	10	33	909	100	220	1

Input Capacitor and Output Capacitor

SCT recommends adding a 2.2μF or greater capacitor with a 0.1μF bypass capacitor in parallel at VIN pin to keep the input voltage stable. Aluminum electrolytic capacitor or other capacitor with high capacitance is suggested for the system power with large voltage spike. The voltage rating of the capacitors must be greater than the maximum input voltage

To ensure loop stability, the SCT71801A00Q product requires an output capacitor with a minimum effective capacitance value of 2.2μF. And the product could support output capacitor range from 2.2uF to 220uF and with an ESR range between 0.001Ω and 5Ω. SCT recommends selecting a X5R- or X7R-type 4.7uF~10uF ceramic capacitor with low ESR over temperature range to improve the load transient response.

When using large output capacitor with higher ESR resistor, for example 100uF output electrolytic capacitor with 1Ω ESR resistor in the application, SCT recommends adding extra 10uF low ESR output capacitor parallel connection with the large electrolytic capacitor, this will eliminate the undershoot/overshoot voltage caused by the large ESR resistor and get better load transient performance.

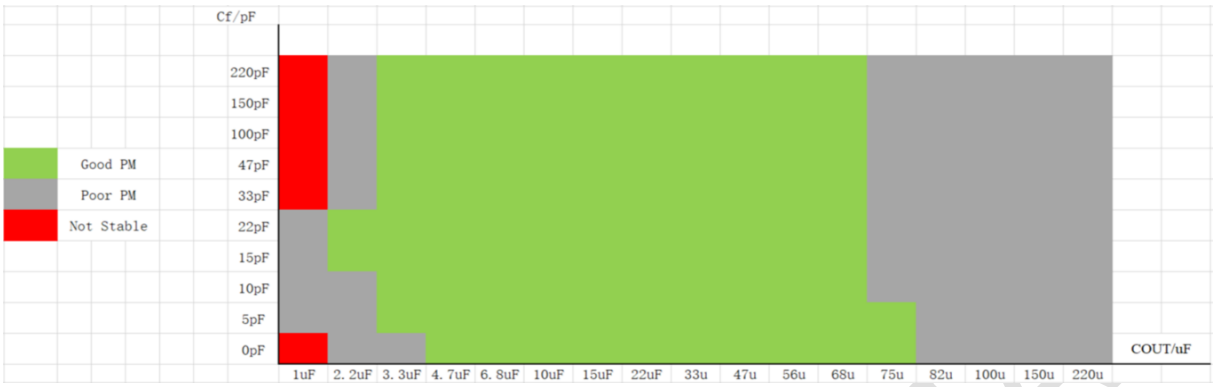


Figure 25. SCT71801A00Q Feed Forward Capacitors recommend(R2=100kΩ,VOUT=1.8V)

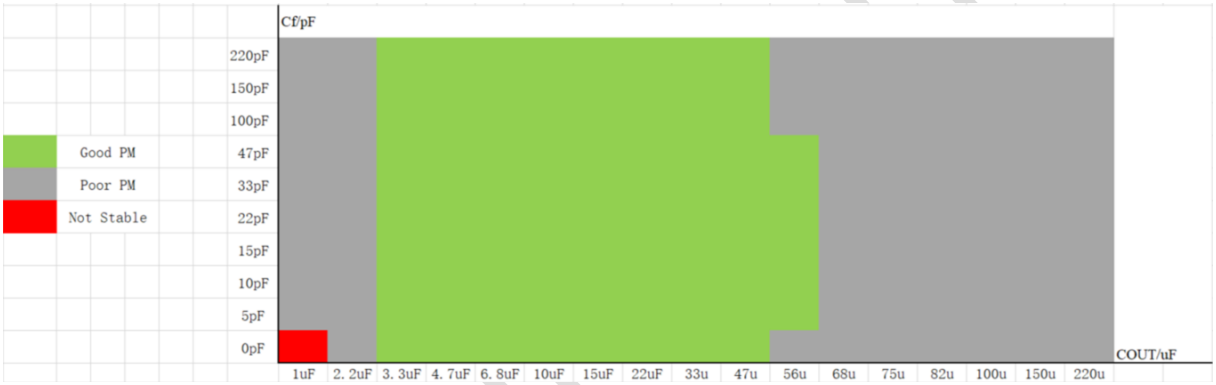


Figure 26. SCT71801A00Q Feed Forward Capacitors recommend(R2=10kΩ,VOUT=1.8V)

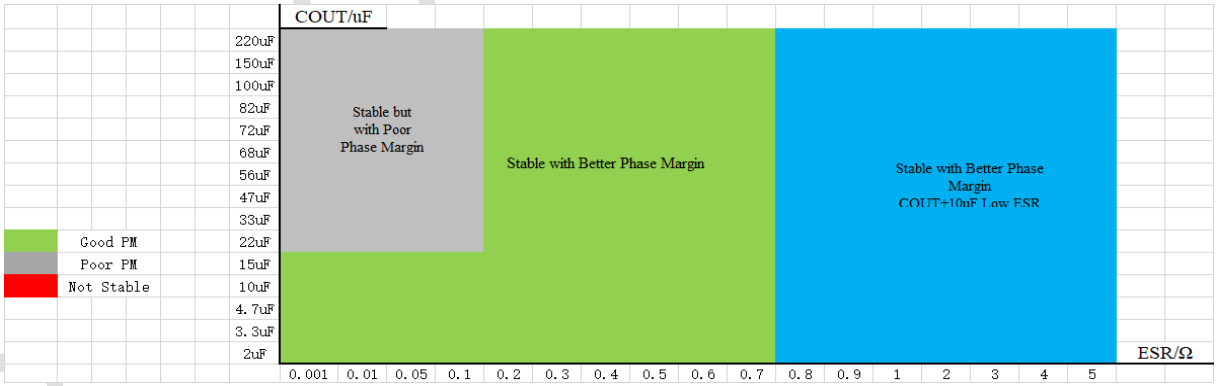


Figure 27. SCT71801A00Q Stability VS Output Capacitor

Power Dissipation and Thermal Performance

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum junction temperature is dependent on power dissipation, package, the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature.

During normal operation, LDO junction temperature should not exceed 150°C, or else it may result in deterioration of the properties of the chip. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 5. Because I_{GND} « I_{OUT}, the term V_{IN} x I_{GND} in Equation 5 could be ignored.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (5)$$

The junction temperature can be estimated using Equation 6. $R_{\theta JA\_EVM}$ is the junction-to-ambient thermal resistance based on customer's PCB. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature T_J.

$$T_J = T_A + P_D \times R_{\theta JA\_EVM} \quad (6)$$

$R_{\theta JA\_EVM}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

For the SCT71801A00Qproduct, the maximum allowable power dissipation of different packages was listed in the following table, and the test results are based on our EVM board, larger power dissipation will trigger thermal shutdown protection. As a result, we could calculate the $R_{\theta JA\_EVM}$ of different packages. The following table is just for your reference based on our EVM test, please leave enough margin when you design thermal performance.

The PCB information of our EVM: 4-layer, 11oz Cu (inner 0.5oz Cu), 50mm x 30mm size.

Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤125℃)	$R_{\theta JA\_EVM}$ (℃/W)
EMSOP-8L	4.019	2.772	36.08

THERMAL CHARACTERISTICS

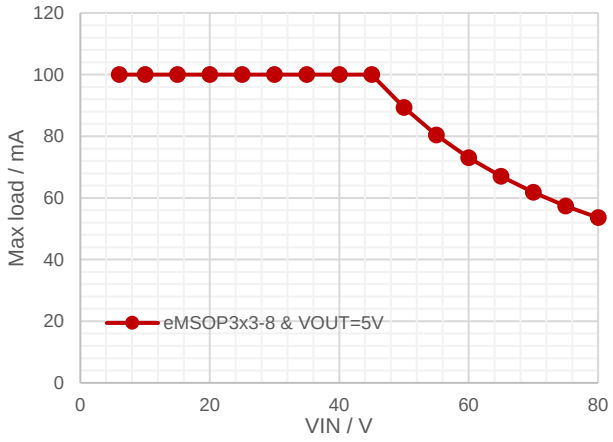


Figure 28. Maximum Output Current vs Input Voltage, VOUT=5V of EMSOP-8L ,$T_J \le$ TSD_R

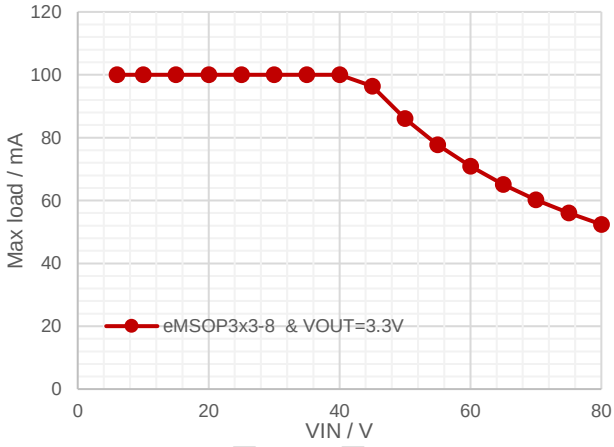


Figure 29. Maximum Output Current vs Input Voltage, VOUT=3.3V of EMSOP-8L ,$T_J \le$ TSD_R

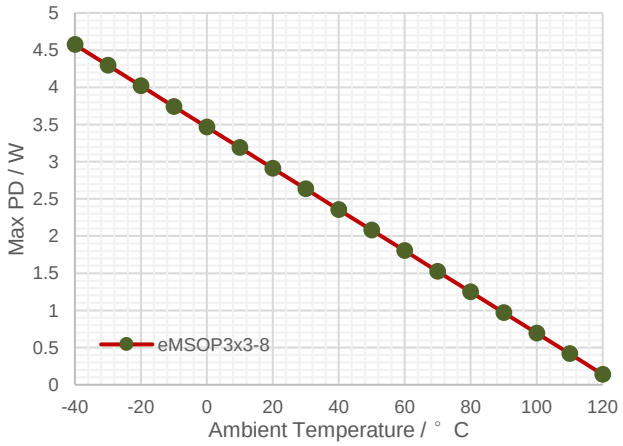


Figure 30. Maximum Allowed Power Dissipation vs Ambient Temperature, EMSOP-8L,TJ ≤ 125℃

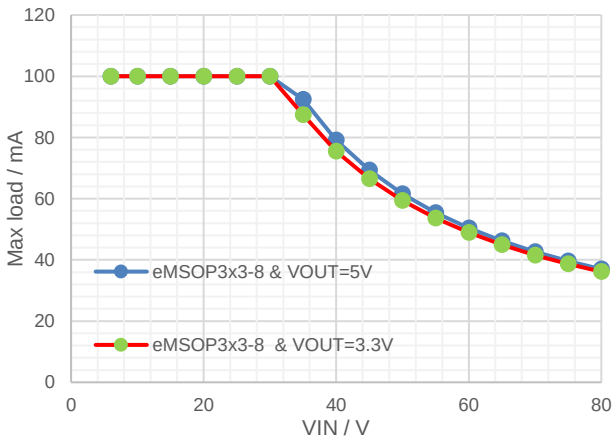


Figure 31. Maximum Output Current vs Input Voltage, EMSOP-8L,TJ ≤ 125℃

Application Waveforms

Vin=Vout +1V, unless otherwise noted

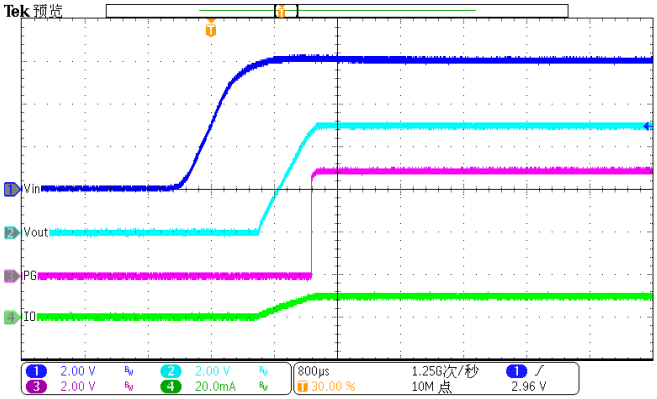


Figure 32. Power up (Iload=10mA)

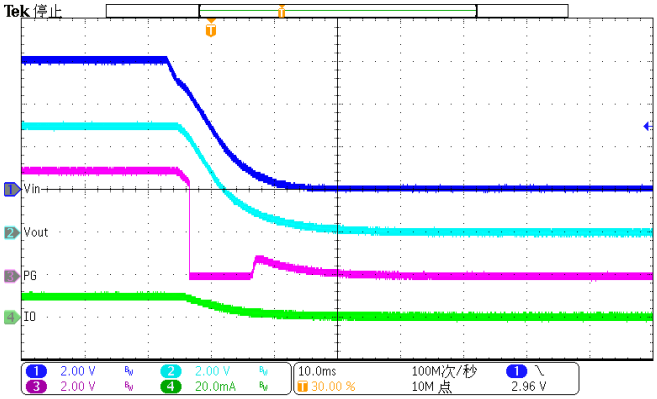


Figure 33. Power down (Iload=10mA)

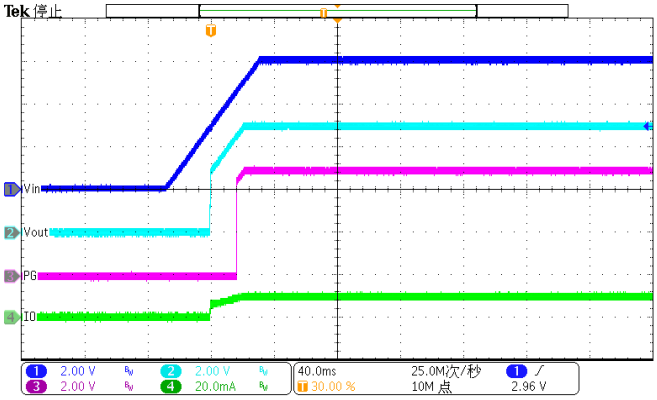


Figure 34. Slow Power up (Iload=10mA)

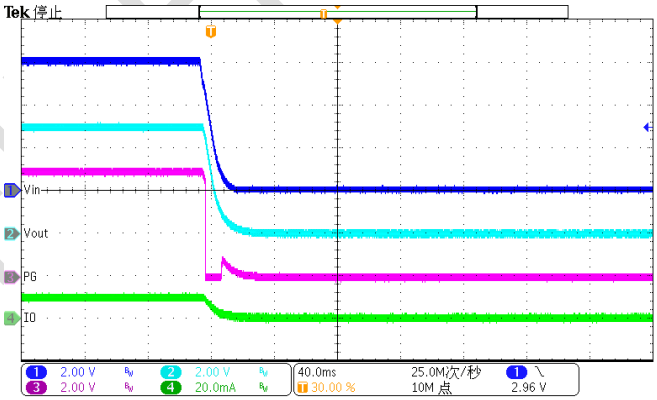


Figure 35. Slow Power down (Iload=10mA)

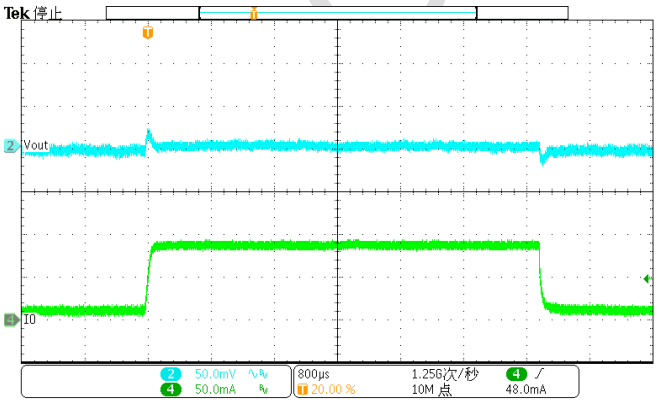


Figure 36. DC-DC Load Transient (10mA-90mA),VOUT=5V

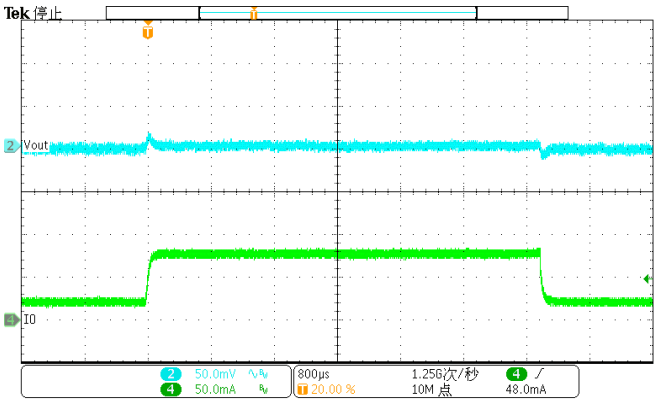


Figure 37. DC-DC Load Transient (25mA-75mA),V_{OUT}=5V

Application Waveforms(Continued)

Vin=Vout +1V, unless otherwise noted

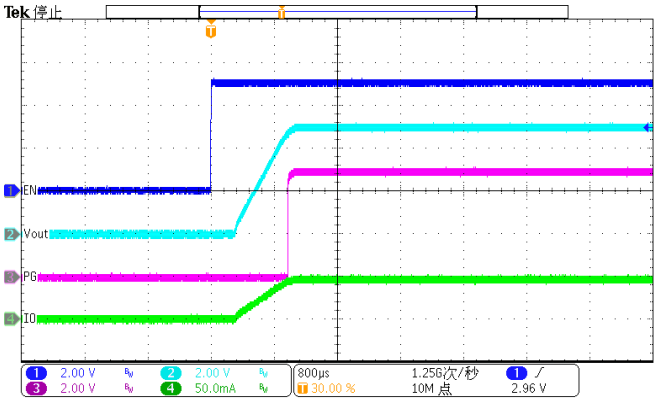


Figure 38. Enable (Iload=50mA)

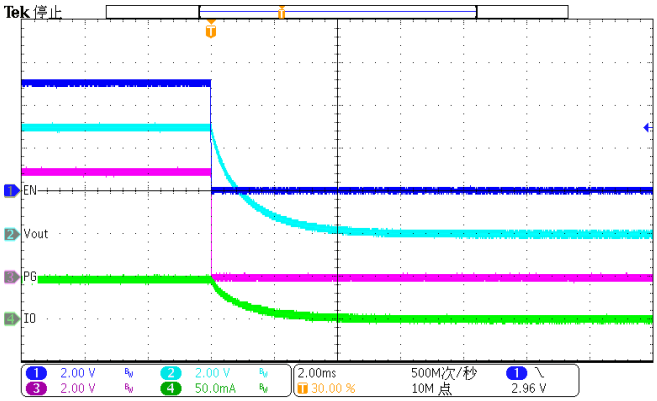


Figure 39. Disable (Iload=50mA)

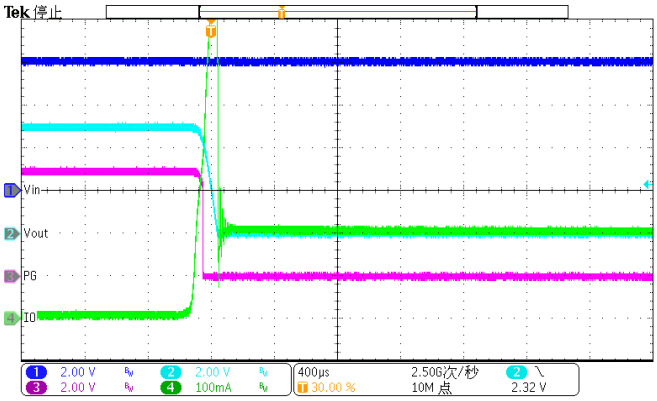


Figure 40. Enter Short Circuit Protection

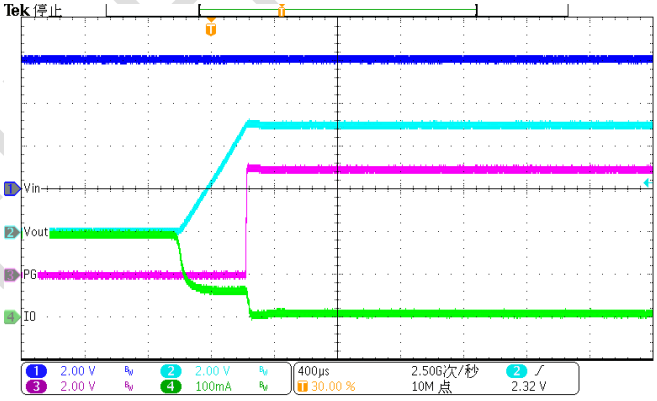


Figure 41. Exit Short Circuit Protection

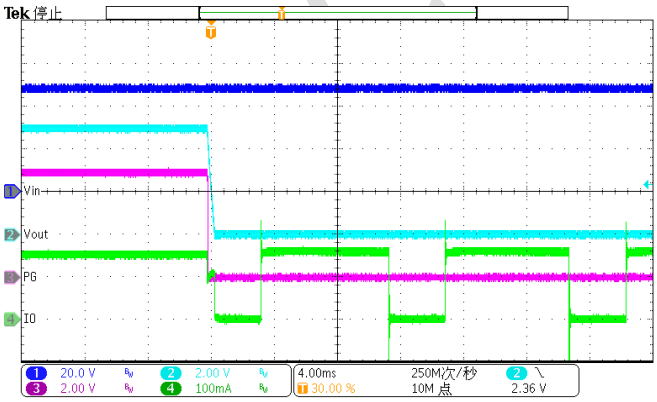


Figure 42. Enter Over Temperature Protection(Vin=48V)

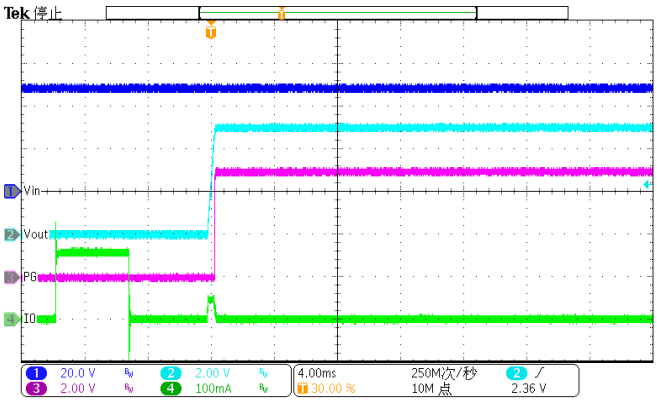


Figure 43. Exit Over Temperature Protection(Vin=48V)

Layout Guideline

Proper PCB layout is a critical for SCT71801Q's stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1μF bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and placing enough thermal vias on the copper under the thermal pad.
5. If using large electrolytic capacitor with high ESR resistor, SCT recommends adding a 10uF low ESR capacitor parallel connection with the large electrolytic capacitor.

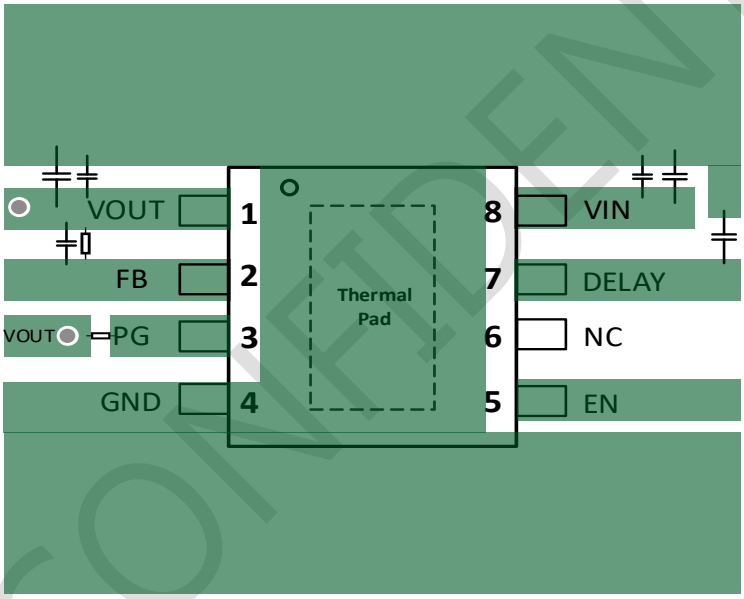
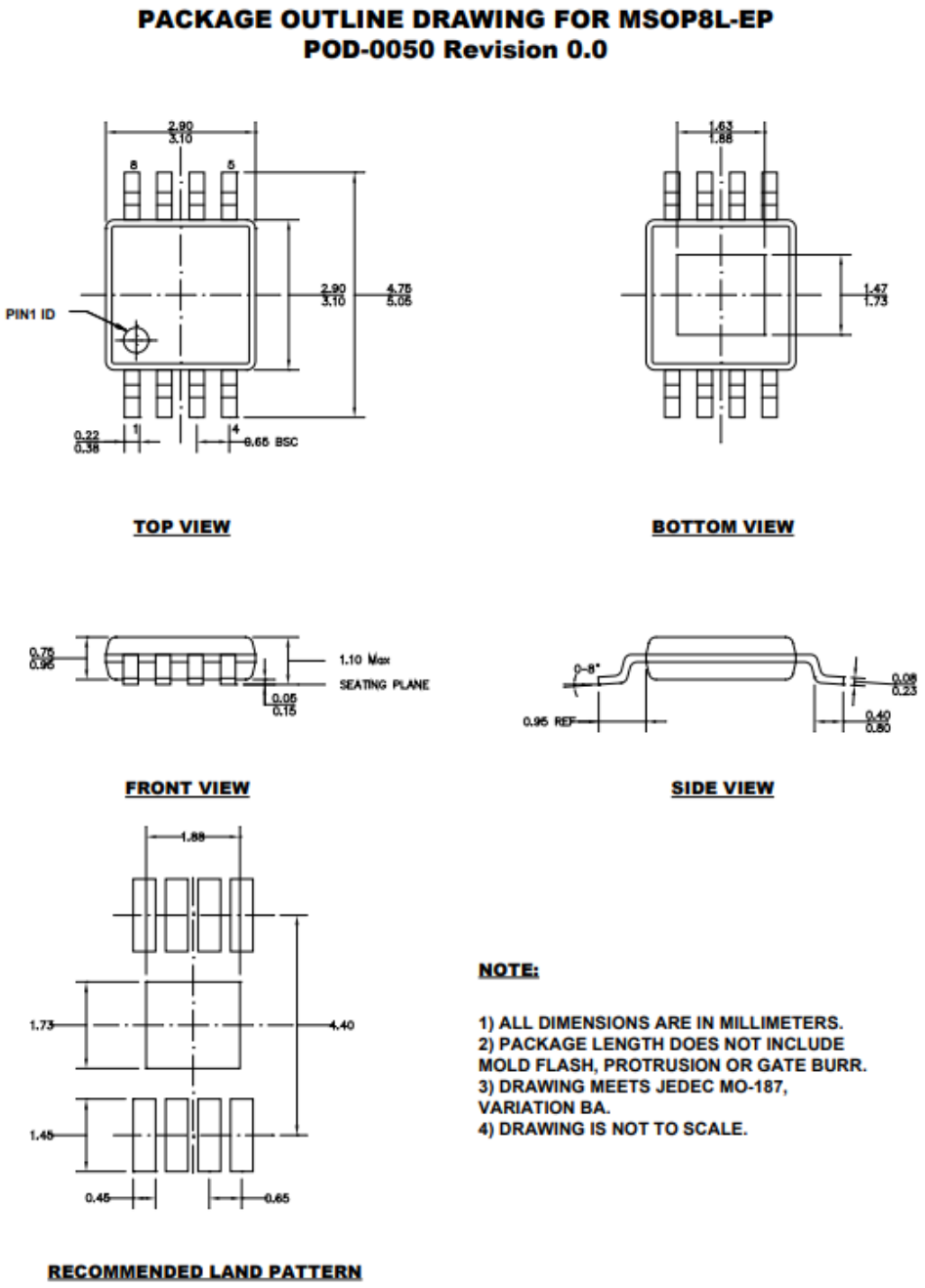


Figure 44. PCB Layout Example

SCT71801A00QMTER

PACKAGE INFORMATION

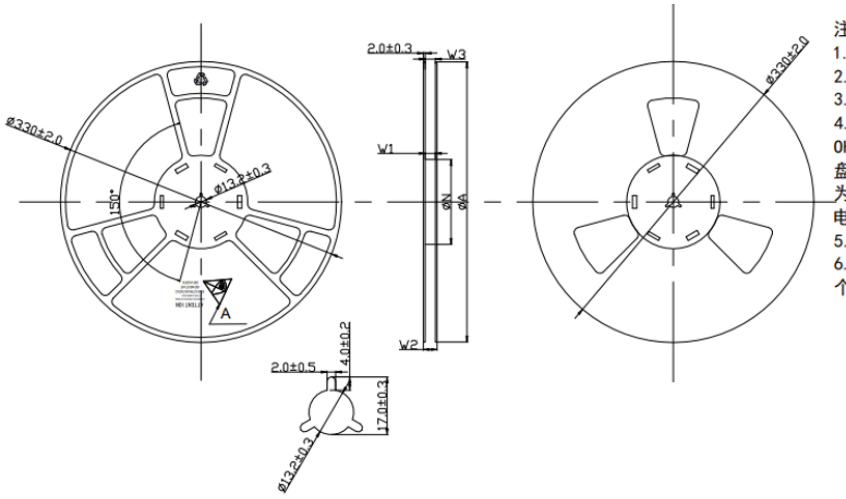


EMSOP-8L Package Outline Dimensions

NOTE:

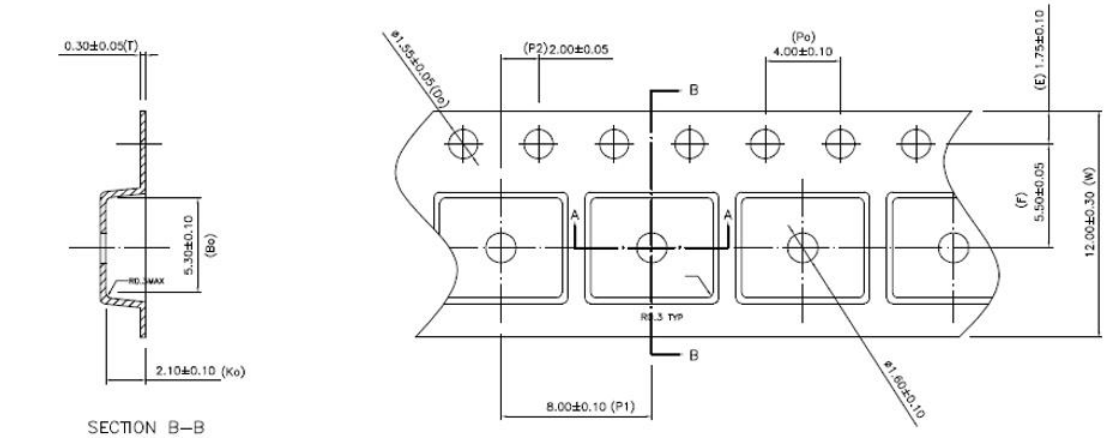
1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION



注意：
1. 材料：聚苯乙烯；
2. 平整度：最大允许3毫米；
3. 所有尺寸为毫米；
4. 表面电阻：10E5~10E11 OHMS/SQ（除了16mm width的卷盘在温度25° C+/-5° 以及湿度为50%RH～～60%RH条件下，表面电阻满足10^5--10^9ohm范围内）
5. 所有未标注公差：±0.5
6. 卷盘不可错位，可通过检验两个盘上A处的印字是否对应判断。

PRODUCT SPECIFICATIONS					
TYPE WIDTH	øA	øN	W1(+2/0)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4	11.9/15.4



NOTES:
1.10 sprocket hole pitch cumulative tolerance±0.2
2.Camber not to exceed 1mm in 100mm.
3.Material: Black conductive Polystyrene.
4.Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5.Ko measured from a plane on the inside bottom of the pocket to the top suface of the carrier.
6.Pocket postion ralative to sprocket hole measured as true postion of pocket ,not pocket hole.
7.Pocket center and pocket hole center must be same postion.