7V Vin, 6A/8A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide 2.9V-7V Input Voltage Range
- 0.6V-VIN*D_{max} V Output Voltage Range
- Integrated 15mΩ/5mΩ Rdson of HS/LS Power MOSFETs
- Fixed 0.8ms Soft-start Time
- Fixed 2.2MHz Switching Frequencies
- Selectable PFM, USM and FCCM Operation Modes
- Selectable 8A Current Limit to support 6A Output Current
- Selectable 10A Current Limit to support 8A Output Current
- Cycle-by-Cycle Current Limiting
- Output Over-Voltage Protection
- Over-Temperature Protection
- Available in a QFN2X3-12L Package

APPLICATIONS

- Automotive Infotainment
- Infotainment and Cockpit Systems
- Solid state driver
- Portable Instruments
- Industrial Supplies

DESCRIPTION

The SCT2161Q is a high efficiency synchronous step-down DC-DC converter with 2.9V-7V input voltage range and adjustable output voltage down to 0.6V. It offers a small saving 2mmx3mm QFN package that supplies continuous 6A/8A output current. The device fully integrates high-side and low-side power MOSFETs with 15mΩ/5mΩ on-resistance to minimize the conduction loss.

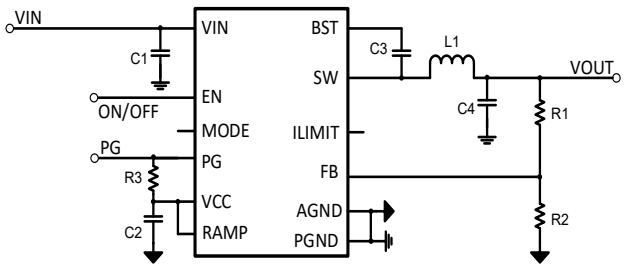
The SCT2161Q adopts a Constant On-Time (COT) control to provide fast transient response and easy loop stabilization. The switching clock frequency is fixed 2.2MHz for optimization of the filter size and output voltage ripple. The device offers fixed 0.8ms soft start to prevent inrush current during the startup of output voltage ramping. Power Good with open drain output signals that the output voltage is within regulation.

The SCT2161Q has the MODE pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save, or Ultrasonic Mode (USM) to keep the switching frequency above audible frequency areas during light-load or no-load conditions, or Forced Continuous Conduction Mode (FCCM) to achieve the small output ripple.

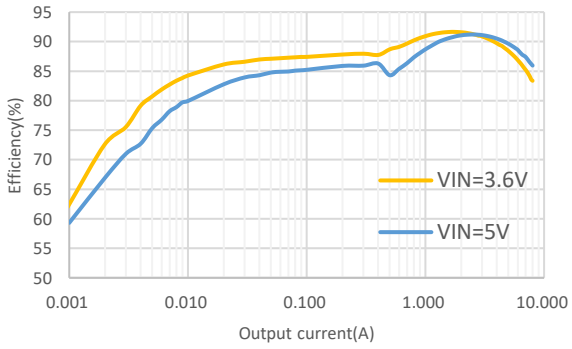
Full protection includes over current protection, under-voltage protection, and thermal shutdown.

The converter requires a minimum number of external components and is available in a QFN- 12 (2mmx3mm) package.

TYPICAL APPLICATION



2.9V-7V, Synchronous Buck Converter



Vout=1.8V, fsw=2.2MHz, PFM

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to market

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2161QFNBR	Tape & Reel	5000	2161Q	12	QFN2X3-12L	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	12	V
BST	SW-0.3	SW+6	V
SW	-1	VIN+0.3	V
MODE	-0.3	6	V
FB	-0.3	6	V
FSEL	-0.3	6	V
ILIMIT	-0.3	6	V
PG	-0.3	6	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

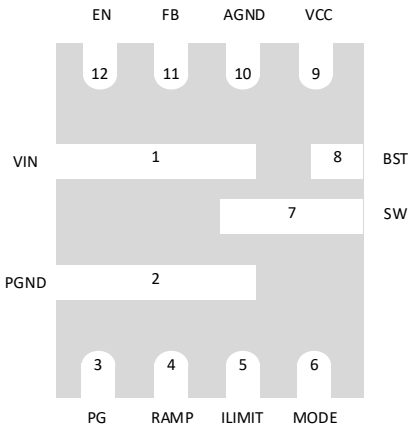

Figure 1. 12-Lead Plastic QFN
(Top view: 2mmx3mm)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VIN	1	Input voltage. Decouple the input rail with at least 0.1uF input ceramic capacitor. Place the capacitor as close as to VIN and PGND pins as possible. Use wide PCB traces and multiple vias to make the connection. SCT2161Q is a high efficiency power converter with 2-3ns fast turning on and turning off power MOSFETs for the best efficiency. If not placing the input capacitor close to VIN and GND pin, the voltage spike caused by trace parasitic inductance might EOS damage the device.
PGND	2	Power ground. Using wide PCB traces and multiple vias large enough to handle the load current.
PG	3	Power good open-drain output. PG is high if the output voltage is higher than 95% or lower than 105% of the nominal voltage.
RAMP	4	Internal compensation set pin. Need to pull up this pin to VCC.
ILIMIT	5	Overcurrent limit selection. The current limit is 8A when pull the pin to low, 10A when the pin is float, and 14A when the pin pull to VCC.

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PIN FUNCTIONS (continued)

NAME	NO.	PIN FUNCTION
MODE	6	PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Conduction Mode (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM.
SW	7	Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.
BST	8	Bootstrap. Must connect a 0.1uF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET.
VCC	9	Internal VCC LDO output. The driver and control circuits are powered by VCC. Don't connect VCC to external circuit. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
AGND	10	Signal logic ground. AGND is need Kelvin connection to PGND.
FB	11	Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical.
EN	12	Enable logic input. EN is a digital input that controls the converter on or off. EN high turns on the device and EN low turns off the device. Connecting to VIN with a 100kΩ pull-up resistor can enable the device.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.9	7	V
V_{OUT}	Output voltage range	0.6	VIN*D_{max}	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model (CDM), per AEC-Q100-011	-0.5	+0.5	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN2X3-12L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	62.5	°C/W
$R_{\theta JCtop}$	Junction to case thermal resistance (1)	73.1	
Ψ_{JT}	Junction-to-top characterization parameter (1)	2.3	
Ψ_{JB}	Junction-to-board characterization parameter (1)	4.78	
$R_{\theta JB}$	Junction-to-board thermal resistance (1)	4.84	
$R_{\theta JA\_EVM}$	Junction to ambient thermal resistance (EVM) (2)	38.2	
Ψ_{JT_EVM}	Junction-to-top characterization parameter (EVM) (2)	3.2	°C/W
Ψ_{JB_EVM}	Junction-to-board characterization parameter (EVM) (2)	7.1	

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(1) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(2) Simulated on SCT standard EVM: SCT2161Q Demo Board, 1oz copper thickness, 70mm x 60mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40°C~150°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.9		7	V
V_{INUVLO} $V_{INUVLO\ HYS}$	Vin UVLO rising threshold VIN UVLO Hysteresis		2.3	2.5 270	2.8	V mV
I_{SD}	Shutdown current	EN=0, Measured on VIN pin		1	5.5	μA
I_Q	Quiescent current from VIN	EN=2V, Vout=5V, No load, No switching. Measured on VIN pin.		160	280	μA
V_{CC}	V_{CC} internal LDO regulator voltage	I_{VCC}=0mA	4.5	4.7	5	V
V_{CC_LR}	V_{CC} internal LDO load regulation	I_{VCC}=5mA			0.5	%
I_{VCC_LIM}	V_{CC} internal LDO current limit	VCC short to ground		30		mA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	T_J=25°C	0.594	0.6	0.606	V
		T_J=-40°C~150°C	0.591	0.6	0.609	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V		100		nA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance	V_{CC}=5V		15	26	mΩ
R_{DSON_L}	Low side FET on-resistance	V_{CC}=5V		5	12	mΩ
Enable and Soft-start						
V_{EN_H} V_{EN_L}	Enable high threshold Enable low threshold		 1.03	1.2 1.1	1.27	V V
I_{EN}	Enable pin input current	EN=1V	0.9	1.5	2	uA
T_{SS}	Soft-start time	VOUT 10% to 90%		0.8	2	ms
Operation Mode						
V_{MD_FCCM}	FCCM mode with logic high threshold	VCC=5V			4.7	V
V_{MD_USM}	PFM mode with USM logic threshold		1.5		3.5	V
V_{MD_PFM}	PFM mode input logic low threshold		0.4			V
Switching Frequency						
F_{SW}	Switching frequency		1.9	2.2	2.5	MHz
T_{ON_TIME}	Minimum On-time(1)			60		ns
T_{OFF_TIME}	Minimum Off-time(1)			120		ns
Power Good						
$PG_{Rising(in)}$	V_{FB} rising, percentage of V_{REF} (Good)			95		%
$PG_{Falling(in)}$	V_{FB} falling, percentage of V_{REF}		79	85	91	%
$PG_{Rising(out)}$	V_{FB} rising, percentage of V_{REF}		108	115	122	%
$PG_{Fallng(out)}$	V_{FB} falling, percentage of V_{REF} (Good)			105		%
PG_{TD}	PG low to high delay			0.5	0.8	ms
V_{PG}	Power Good PG pull-down strength	I_{PG} =4mA		0.4	0.8	V
I_{PG_LEAK}	Power Good PG leakage current	VPG=5V			1	μA

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Protection						
I_{LIM_P}	LS MOSFET positive current limit	From source to drain，ILIMIT connects to GND	5	8		A
		From source to drain，ILIMIT floating	7	10		A
		From source to drain，ILIMIT connects to VCC.	10	14		A
I_{LIM_N}	LS MOSFET negative current limit	From drain to source, MODE connects to VCC	2.5	5	7.5	A
T_{HICCUP}	Hiccup waiting time			10		ms
V_{OVP_R}	V_{FB} OVP threshold % of V_{REF}	V_{FB} rising	116	123	130	%
V_{OVP_F}	V_{FB} OVP threshold % of V_{REF}	V_{FB} falling		118		%
V_{UVP_F}	V_{FB} UVP threshold % of V_{REF}	V_{FB} falling	69	75	81	%
T_{SD}	Thermal shutdown threshold	T_J rising		170		°C
	Hysteresis			30		°C

Note:
(1) Guaranteed by design, test on bench.

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TYPICAL CHARACTERISTICS

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.8V, Temperature=25C.

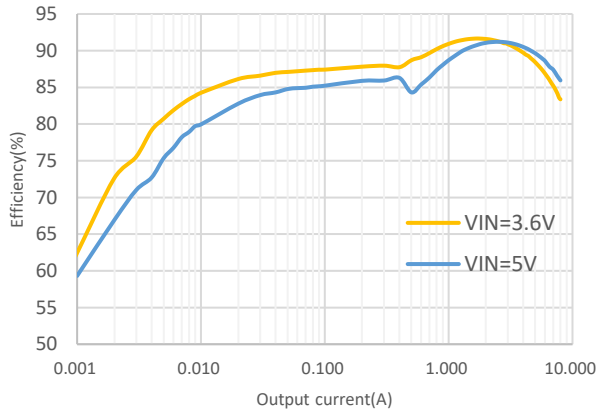

Figure 2. Efficiency at PFM, Vout=1.8V

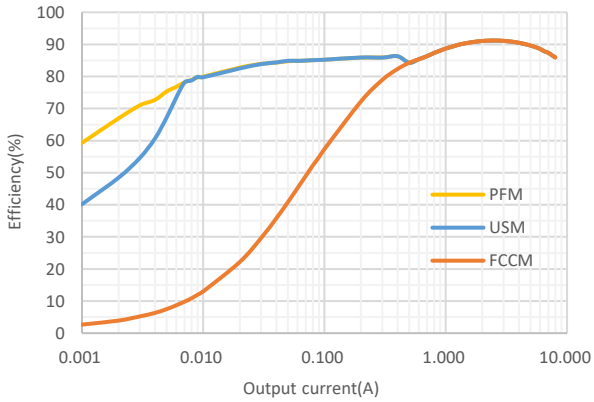

Figure 3. Efficiency at VIN=5V, Vout=1.8V

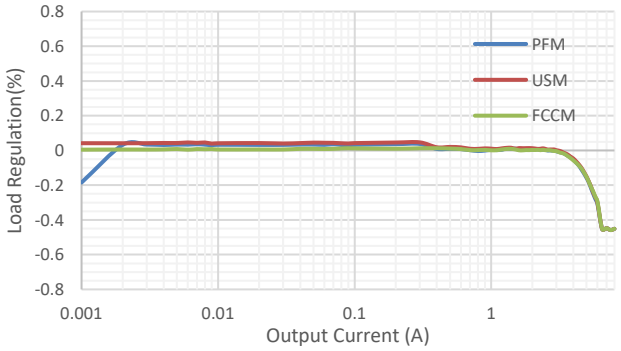

Figure 4. Load Regulation

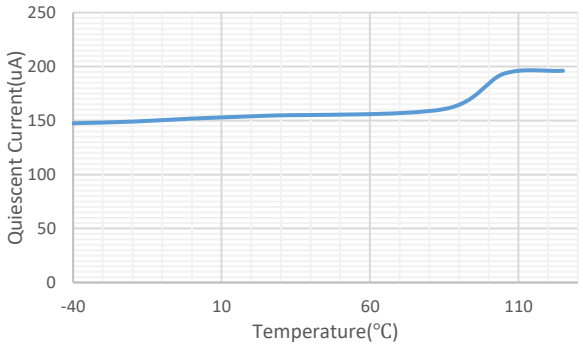

Figure 5. Quiescent Current VS Temperature

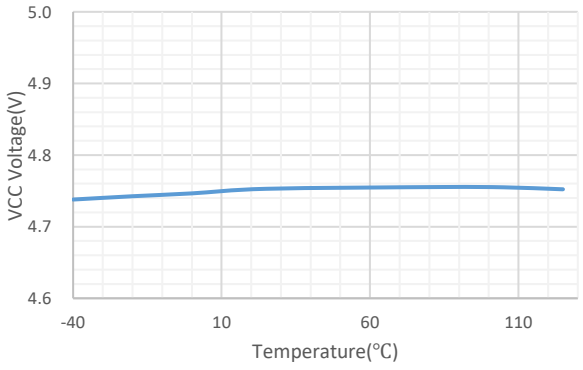

Figure 6. VCC Voltage VS Temperature

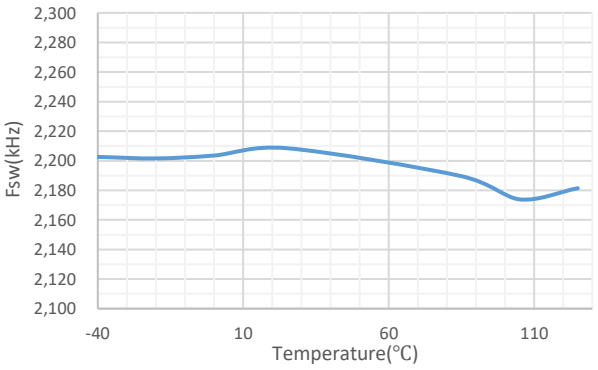

Figure 7. Fsw VS Temperature

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FUNCTIONAL BLOCK DIAGRAM

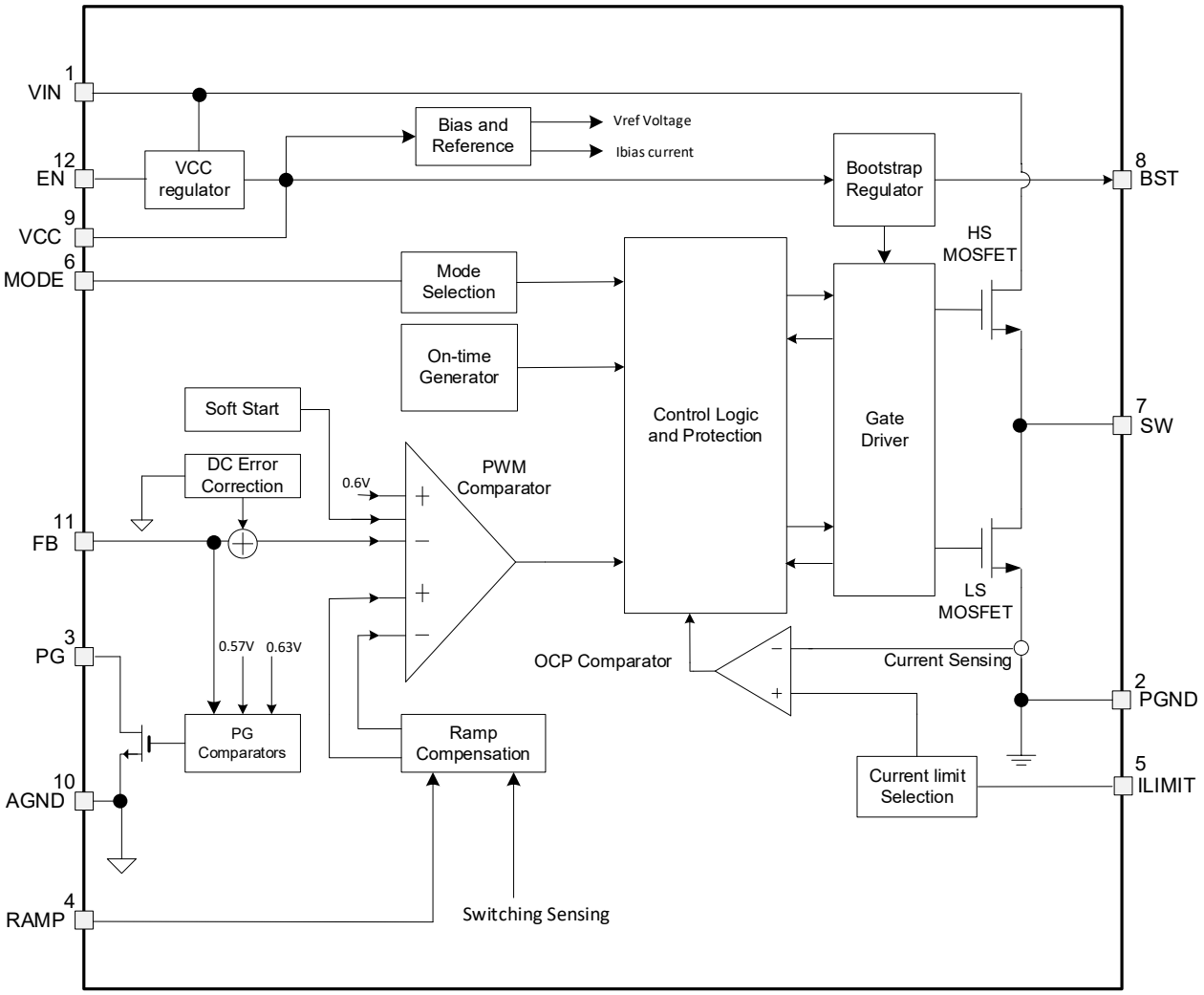

Figure 8. Functional Block Diagram

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OPERATION

Overview

The SCT2161Q is a 2.9V-7V input, 6A/8A continuous output synchronous buck converter with built-in 15mΩ Rdson high-side and 5mΩ Rdson low-side power MOSFETs. It implements the Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is fixed 2.2MHz to optimize external components' sizes. The SCT2161Q features an internal 0.8ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device features three different operation modes at light loading: Pulse Frequency Modulation (PFM) mode, Ultra-Sonic Modulation (USM) mode and Forced Continuous Conduction Mode (FCCM). The quiescent current is typically 160uA under no load and sleep mode condition to achieve high efficiency at light load.

The SCT2161Q has a default start-up voltage of 2.5V with 270mV hysteresis. The EN function features with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Connecting EN pin to VIN with a 100kΩ resistor starts up the device automatically.

The SCT2161Q full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant on-time (COT) Mode Control

The SCT2161Q employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and output voltage. After the on-time, the Q1 turns off and the low-side MOSFET (Q2) turns on after dead time duration. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreases below the VREF, the Q1 turns during one on-time after another dead time duration. This repeats on cycle-by-cycle based.

The SCT2161Q works with internal compensation for optimizing the loop stability and transient response.

Pulse Frequency Modulation (PFM) and Ultra-sonic Modulation (USM) Modes

Grounding the MODE pin makes the SCT2161Q works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current.

Floating the MODE pin makes the device works at PFM with Ultra-Sonic Modulation (USM) mode to keep the switching frequency out of the acoustic audible frequency. The USM mode block monitors the state of both high-side and low-side MOSFETs. When both high-side and low-side MOSFETs are off for 33us, the low-side MOSFET forces to turn on until the negative current limit is triggered or the feedback voltage (VFB) drops below the internal reference voltage (VREF).

Forced Continuous Conduction Mode (FCCM)

Connecting MODE pin to VCC, the SCT2161Q forces the device operating at Forced Continuous Conduction Mode (FCCM) with pseudo-fixed switching frequency regardless loading current. Operating in FCCM mode can achieve smaller output voltage ripple compared with PFM or USM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

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Enable and Under Voltage Lockout Threshold

The SCT2161Q is enabled when the VIN pin voltage rises above 2.9V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 2.23V or when the EN pin voltage is below 1.1V.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.2 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

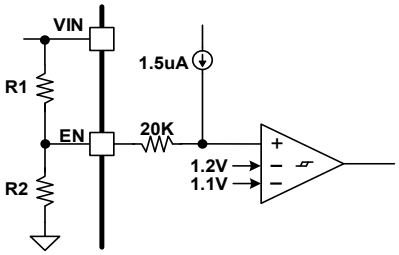

Figure 9. System UVLO by enable divide

Output Voltage

The SCT2161Q regulates the internal reference voltage at 0.6V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2161Q integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 0.8ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Overcurrent Limit Selection

The current limit of the SCT2161Q is selectable to be one of three options: 8A, 10A, 14A. The current limit selection programmed by LIMIT pin. The selection information shown in following table. The current limit setting is latched in at each power up and not be able to be modified during operation. Cycling the input power or the EN pin can reselect the Current limit.

Table 1. LIMIT Pin Set-up for Current limit Selection

LIMIT pin Set-up	Connect to GND directly	Floating	Connect to VCC directly
Current Limit	8A	10A	14A

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Mode Selection

The SCT2161Q features three different operation modes at light load by easily programming the MODE pin. The programming information is listed in following table. The mode setting is latched in at each power up and is not be able to be modified during operation. Cycling the input power or the EN pin can reselect the switching frequency.

Table 2. MODE Pin Set-up for Mode Selection

MODE pin Set-up	Connect to GND directly	Floating	Connect to VCC directly
Operation mode at light load	PFM	PFM with USM	FCCM

Power Good (PG)

The Power Good (PG) pin is the output of an open drain output. When the FB pin is typically between 95% and 105% of V_{REF} the PG is de-asserted and floats after a 500μs de-glitch time. A pull-up resistor of 10 kΩ to 100 kΩ is recommended to pull it up to VCC. The PGOOD pin is pulled low when the FB pin voltage falls under 85% or rises over 115% of V_{REF}, including UVP and OVP, or in an event of thermal shutdown or during the soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from 5V VCC power when high-side power MOSFET is off and low-side power MOSFET is on.

Over Current Limit and Hiccup Mode

The output over-current limit (OCL) is implemented in SCT2161Q by using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state of the high-side FET (Q1) by measuring the low-side FET(Q2) drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decrease linearly. The average value of the switch current is the load current IOUT.

If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. When the current is limited, the output voltage tends to drop because the load demand is higher than what the converter can support. After soft start end with 0.8ms waiting time, when the output voltage falls below 75% of the target voltage, the UVP comparator detects it and shuts down the device immediately, the device re-starts after a hiccup time of 10ms. When the overcurrent condition is removed, the output voltage returns to the regulated value.

The hiccup protection mode above makes the average short circuit current lower to alleviate thermal issues and protect the regulator.

Under-voltage Protection

The SCT2161Q features the Under-voltage Protection (UVP) by monitoring the output voltage to detect the under-voltage voltage. When the feedback voltage falls below 75% of V_{REF}, the SCT2161Q enters hiccup mode until the under-voltage scenario released.

Over voltage Protection

The SCT2161Q implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When the feedback voltage rises higher than 122% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on until trigger negative current limit or FB below reference voltage. Then HS-FET turns

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on with normal ON-time and turn off, following with a LS-FET on until negative current limited triggered or FB lower than reference voltage. The device exits this regulation period when the feedback voltage falls below 117% of the reference voltage.

Thermal Shutdown

The SCT2161Q protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 140C, the device restarts with internal soft start phase.

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2161Q.

Use Equation 4 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, two 10V/22uF input ceramic capacitors are recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation 5.

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (5)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current. Typical values range from 0.3 to 0.5.

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Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in equation 6.

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (6)$$

Set the peak current I_{LPEAK} lower than the current limit of the SCT2161Q and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 7 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (7)$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

Output Feedback Resistor Divider Selection

The SCT2161Q features external programmable output voltage by using a resistor divider network R7 and R8 as shown in the typical application circuit Figure10. Use equation 8 to calculate the resistor divider values.

$$R_7 = \frac{(V_{OUT} - V_{ref}) \times R_8}{V_{ref}} \quad (8)$$

Table 3 Recommended Component Values for Typical Output Voltage (Vin=5V)

Vout (V)	L (uH)	R7 (kΩ)	R8 (kΩ)	Cf (pF)
1.0	0.22	6.8	10.2	N/A
1.8	0.33	20.4	10.2	N/A
3.3	0.47	45.9	10.2	N/A

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APPLICATION INFORMATION

Typical Application

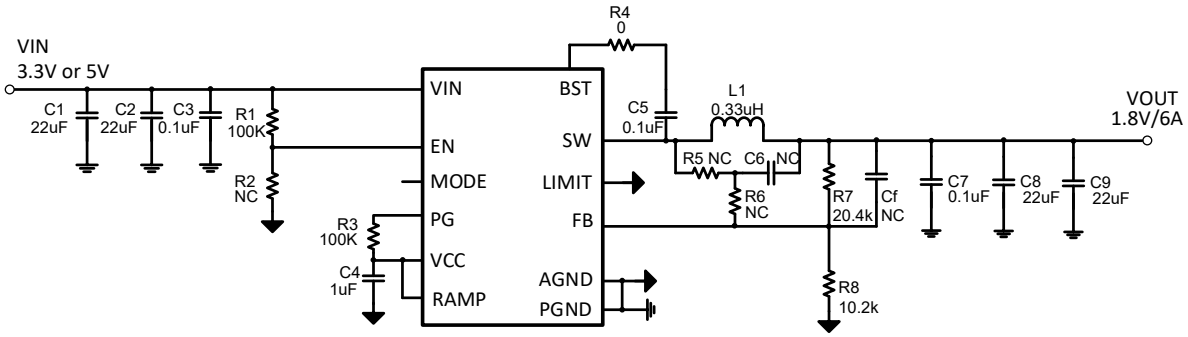

Figure 10. SCT2161Q Design Example, 1.8V/6A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.3V or 5V
Output Voltage	1.8V
Maximum Output Current	6A
Switching Frequency	2.2MHz
Output voltage ripple (peak to peak)	10mV

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Application Waveforms

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.8V, IOUT=6A, Temperature=25C.

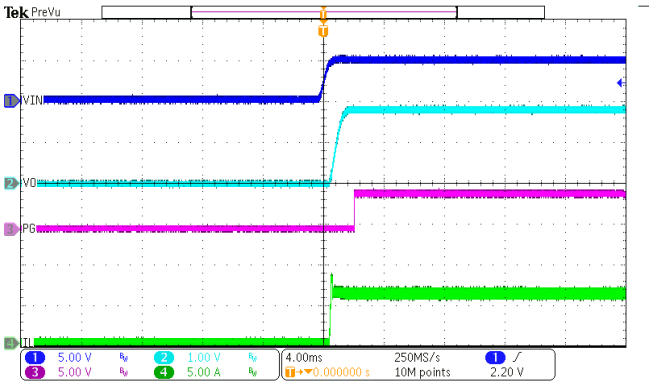

Figure 11. Power up (Iload=6A)

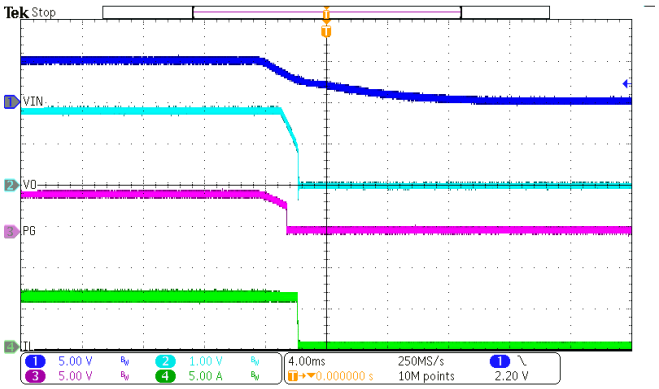

Figure 12. Power down (Iload=6A)

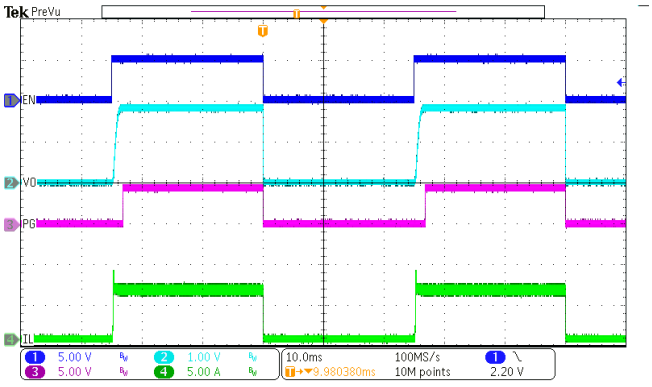

Figure 13. EN toggle (Iload=6A)

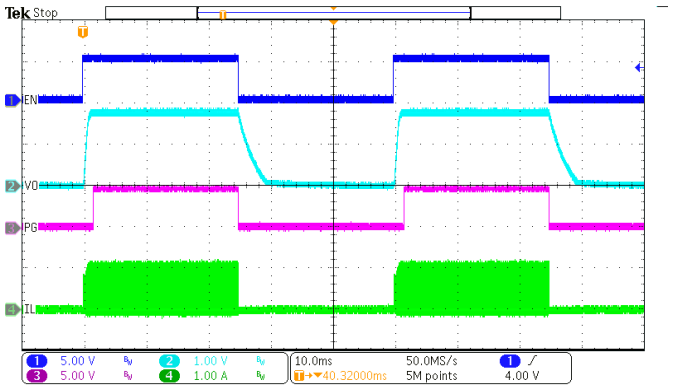

Figure 14. EN toggle PFM (Iload=10mA)

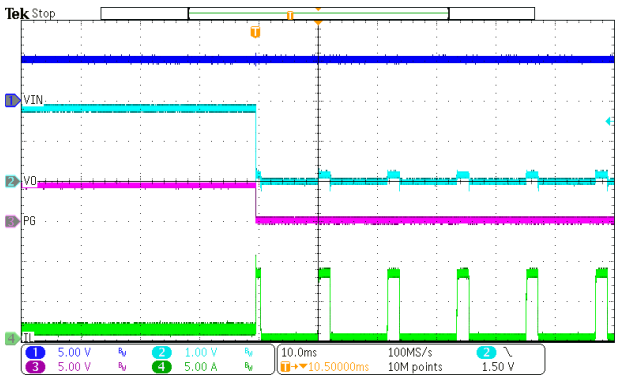

Figure 15. Over Current Protection(1A to hard short)
ILIMIT=8A

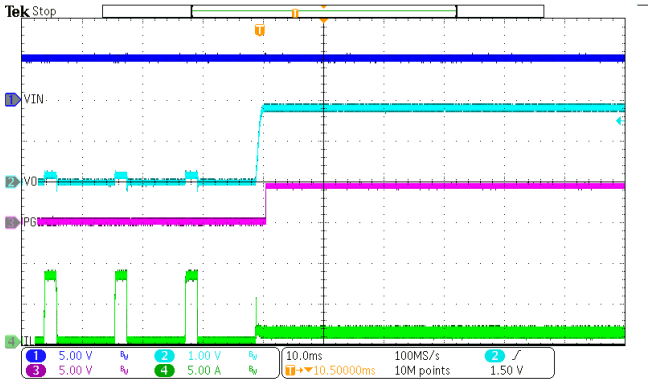

Figure 16. Over Current Release (hard short to 1A)
ILIMIT=8A

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Application Waveforms(Continued)

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.8V, IOUT=6A, Temperature=25C.

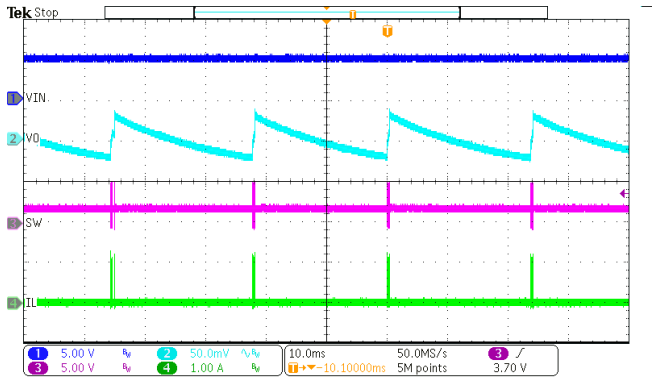

Figure 17. Output Ripple (Iload=0A, PFM)

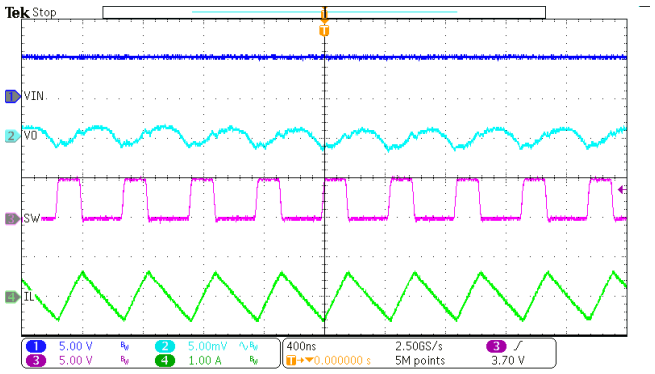

Figure 18. Output Ripple (Iload=0A, FCCM)

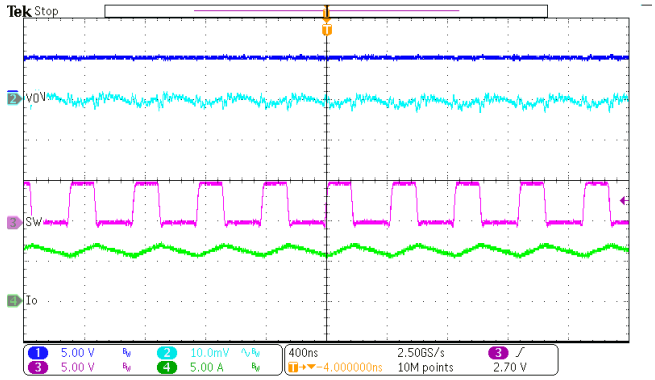

Figure 19. Output Ripple (Iload=6A)

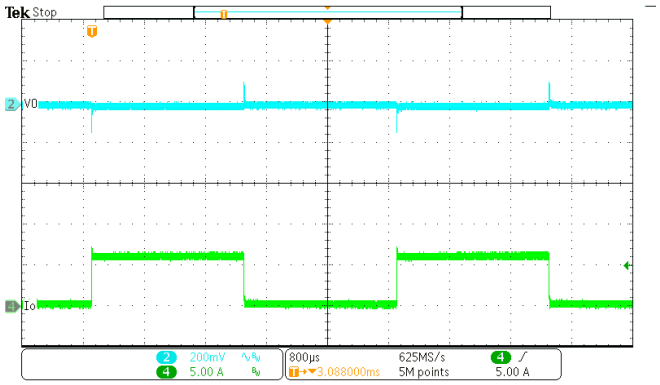

Figure 20. Load Transient (0A-6A, 1.6A/us)

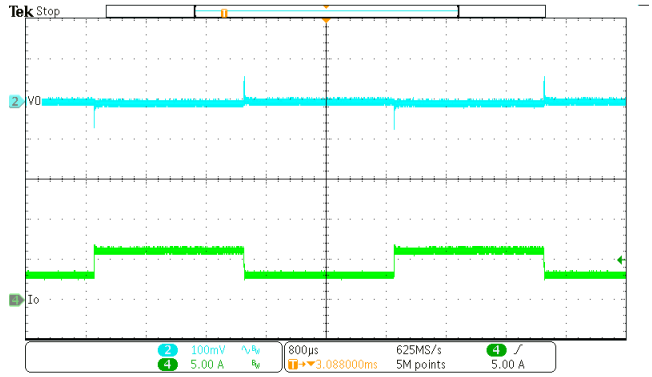

Figure 21. Load Transient (3A-6A, 1.6A/us)

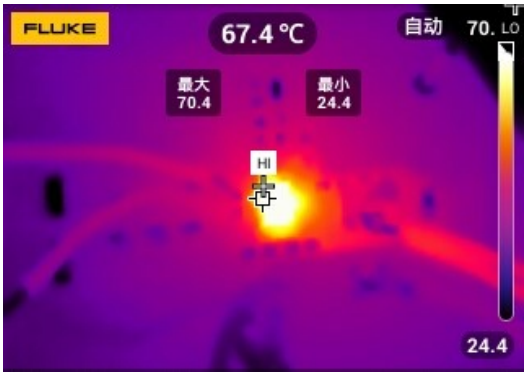

Figure 22. Thermal, Fsw=2.2MHz, Iload=6A

APPLICATION INFORMATION

Typical Application

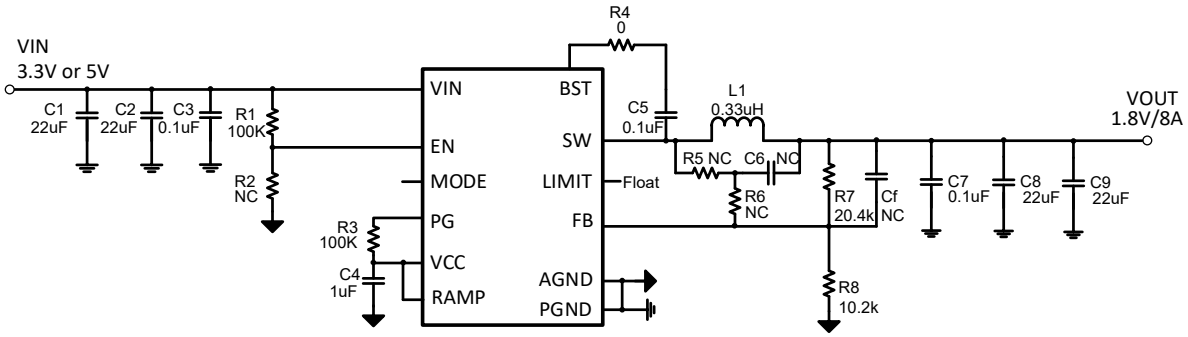

Figure 23. SCT2161Q Design Example, 1.8V/8A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.3V or 5V
Output Voltage	1.8V
Maximum Output Current	8A
Switching Frequency	2.2MHz
Output voltage ripple (peak to peak)	10mV

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Application Waveforms

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.8V, IOUT=8A, Temperature=25C.

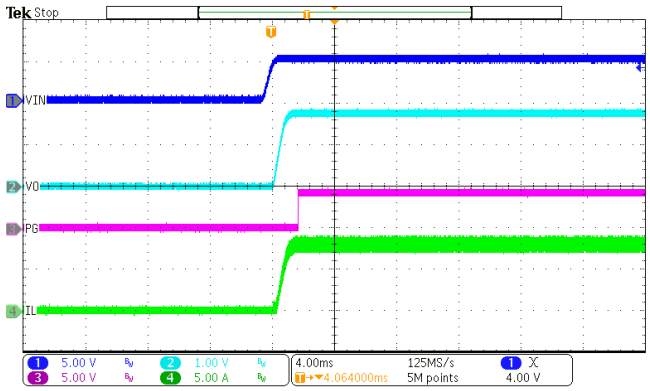

Figure 24. Power up (Iload=8A)

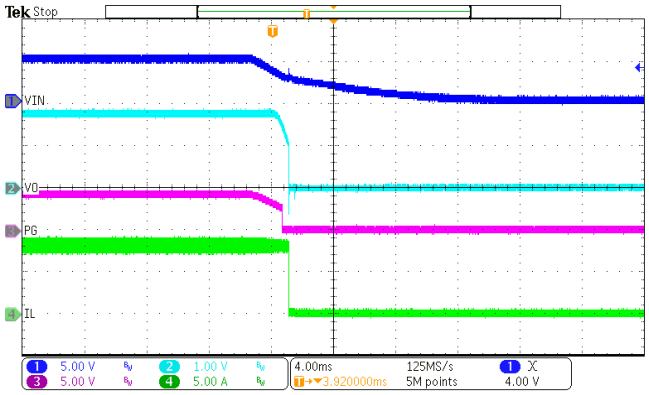

Figure 25. Power down (Iload=8A)

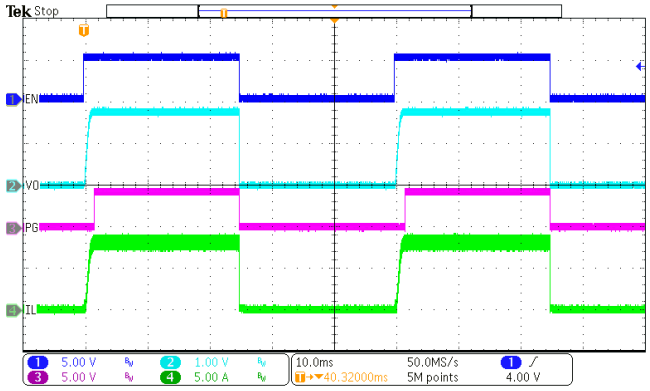

Figure 26. EN toggle (Iload=8A)

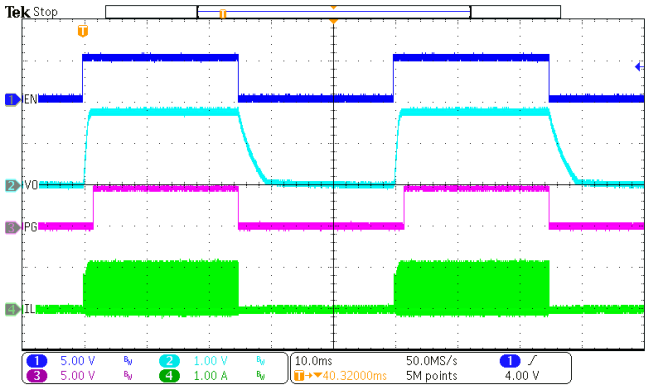

Figure 27. EN toggle PFM (Iload=10mA)

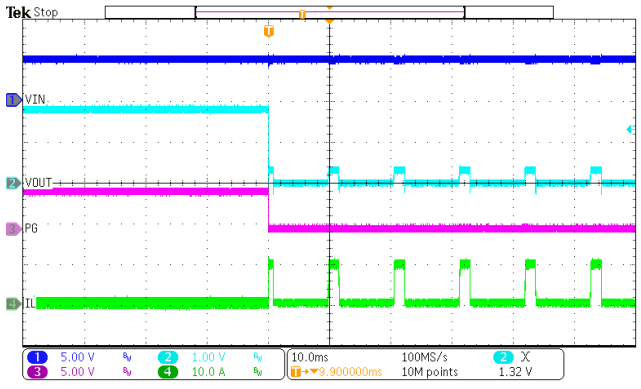

Figure 28. Over Current Protection(1A to hard short)
ILIMIT=10A

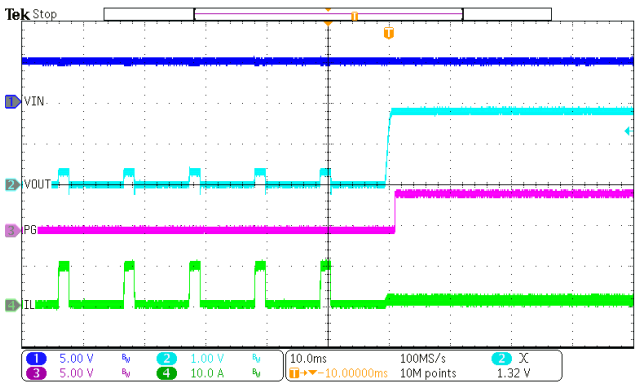

Figure 29. Over Current Release (hard short to 1A)
ILIMIT=10A

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Application Waveforms(Continued)

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.8V, IOUT=8A,Temperature=25C.

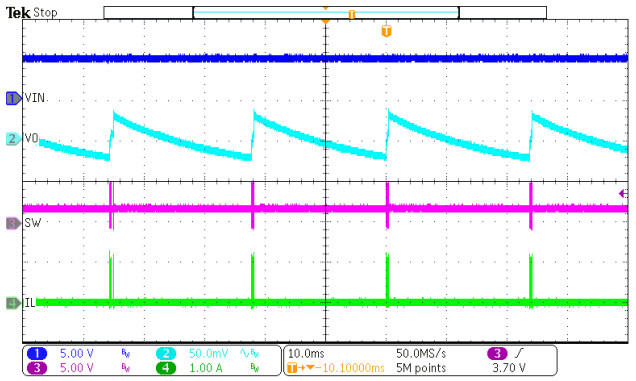

Figure 30. Output Ripple (Iload=0A, PFM)

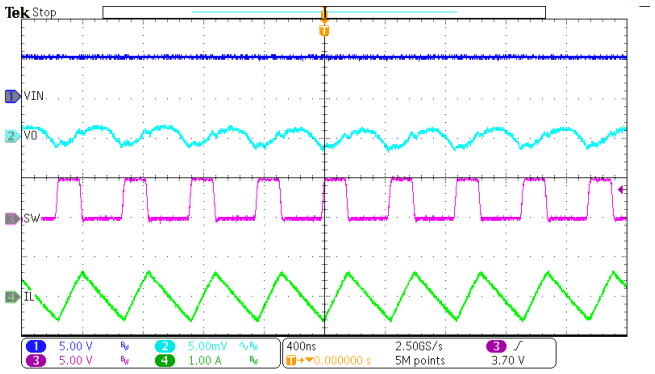

Figure 31. Output Ripple (Iload=0A, FCCM)

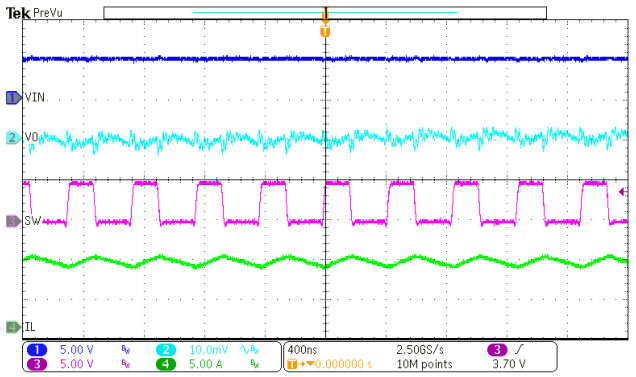

Figure 32. Output Ripple (Iload=8A)

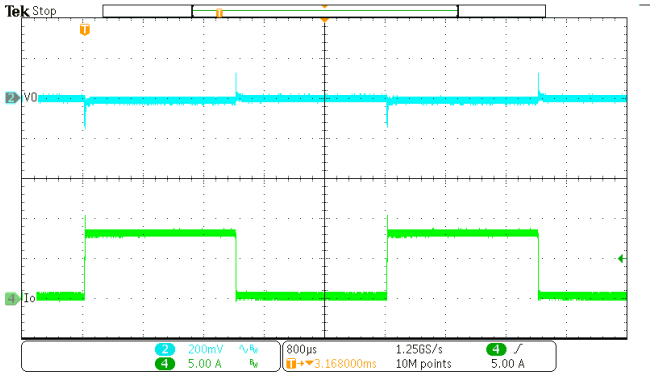

Figure 33. Load Transient (0A-8A, 1.6A/us)

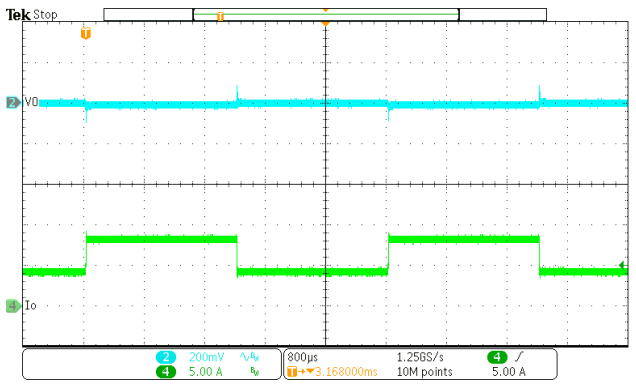

Figure 34. Load Transient (4A-8A, 1.6A/us)

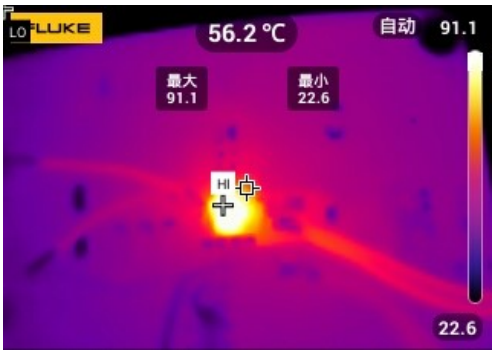

Figure 35. Thermal, Fsw=2.2MHz, Iload=8A

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Layout Guideline

Proper PCB layout is a critical for SCT2161Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
3. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
4. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
5. UVLO adjust and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. Route BST resistor and capacitor with a minimized length between the BST PIN and SW PIN.

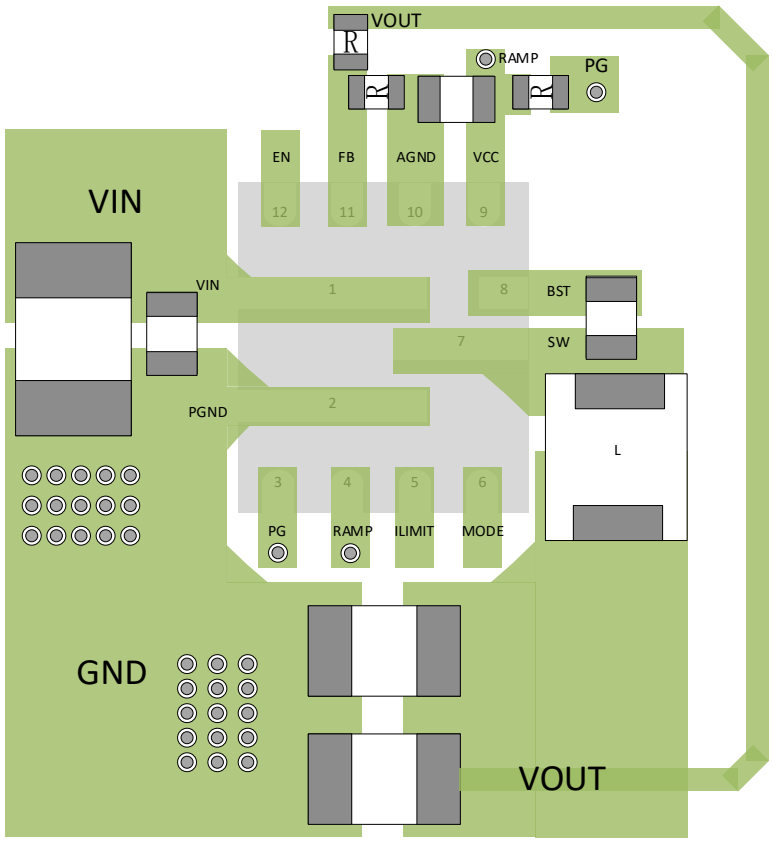
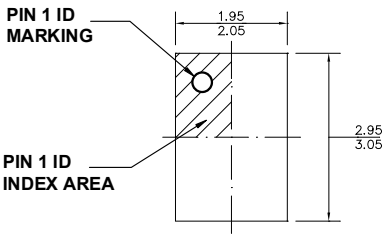


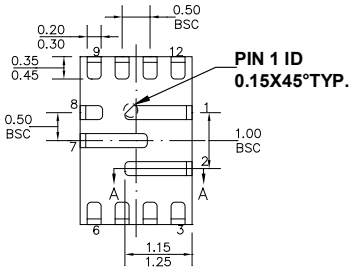
Figure 36. PCB Layout Example

PACKAGE INFORMATION

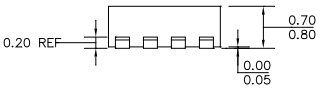
PACKAGE OUTLINE DRAWING FOR 12L FCTQFN (2.0X3.0MM)



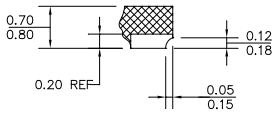
TOP VIEW



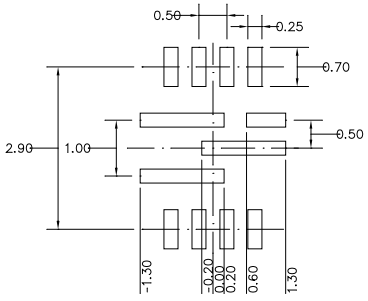
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFIRMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

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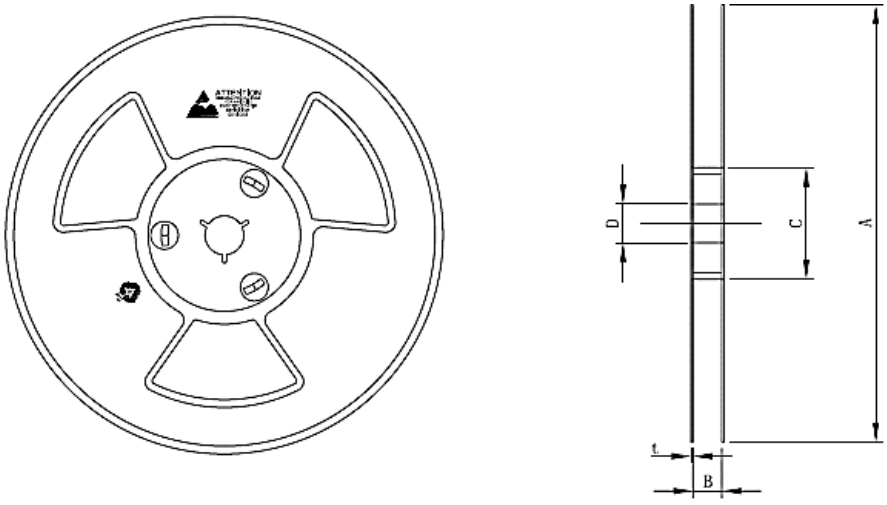
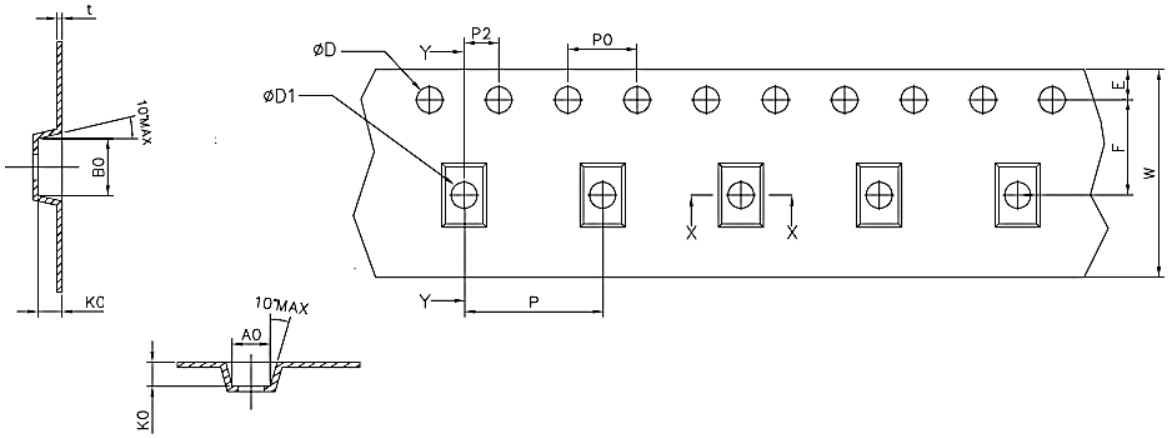
TAPE AND REEL INFORMATION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	328	329	330
B	11.80	12.80	13.80
C	99	100	101
D	13.00	13.30	13.60
t	1.70	2.00	2.30



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
E	1.65	1.75	1.85
F	5.45	5.50	5.55
P2	1.95	2.00	2.05
D		1.50	1.60
D1		1.50	1.75
P0	3.90	4.00	4.10
W	11.90	12.00	12.30
P	7.90	8.00	8.10
A0	2.10	2.20	2.30
B0	3.20	3.30	3.40
K0	1.04	1.14	1.24
t	0.23	0.25	0.27

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