2.65V-5.5V Vin, 0.6A Synchronous Step Down PPD Module™ with integrated inductor

FEATURES

- Input Voltage Range: 2.65V-5.5V
- 0.6A Continuous Output Current Capability
- Low Shutdown Current: 0.05μA
- 0.6V Feedback Reference Voltage
- 2.2MHz Switching Frequency
- Active output discharge
- Pulse Frequency Modulation at light load
- 100% Duty Cycle function
- Integrated soft start
- Integrated Protection Feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - Hiccup Over Current Protection
  - Thermal Shutdown Protection:160°C
- Available in an ECLGA1.5X2-6L Package

APPLICATIONS

- Optical Modules
- Industrial Products
- Internet of Things (IoT) Devices
- Space-Constrained Applications
- Low-Dropout(LDO) Regulator Replacement
- Portable Devices
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DESCRIPTION

The SCT2113M is a highly integrated step-down PPD Module™ optimized for small solution size and high efficiency.

The device achieves 0.6A of continuous output current from a 2.65V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

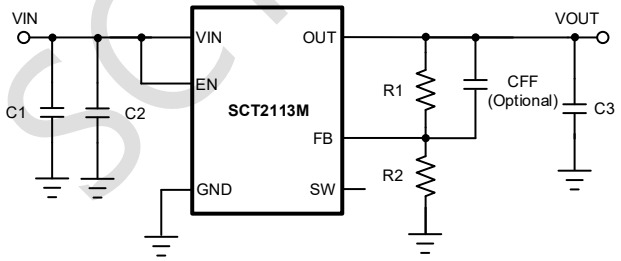
The SCT2113M, adopting the constant-on time (COT) mode control provides fast transient response and eases loop stabilization, greatly simplifies the converter off-chip configuration.

The SCT2113M device operates in Pulse Frequency Modulation (PFM) to achieve high efficiency during light load operation. It features a fixed 2.2MHz switching frequency and supports 100% duty cycle function.

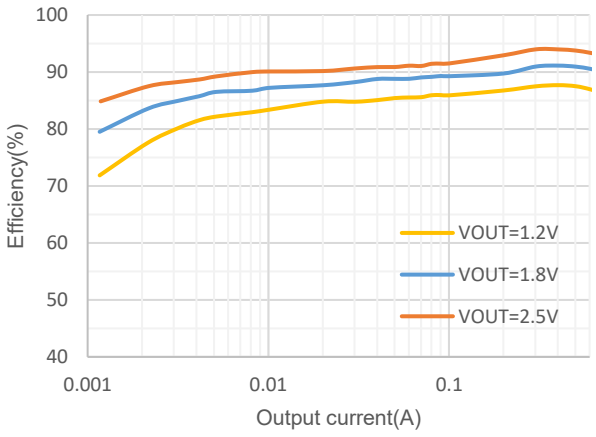
The SCT2113M includes comprehensive protection features, such as cycle-by-cycle current limit and hiccup over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2113M requires only five external components and is available in a space-saving ECLGA1.5X2X0.959-6L package.

TYPICAL APPLICATION



2.65V-5.5V, Synchronous Buck Converter Module



Efficiency, VIN=3.3V

REVISION HISTORY

Revision 0.8: Customer sample.

DEVICE ORDER INFORMATION

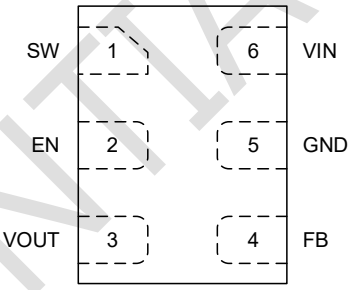
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PINS	PACKAGE DESCRIPTION	MSL
SCT2113MLVAR	Tape & Reel	TBD	6	ECLGA1.5X2-6L	TBD

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, SW, VOUT, FB	-0.3	6	V
SW (Pulse<10ns)	-2.5	6.5	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-55	125	°C

PIN CONFIGURATION



Top View: ECLGA-6L
1.5mm*2.0mm*0.959mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
SW	1	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time.
EN	2	Enable logic input. Connect high to enable device.
VOUT	3	Power output, please use as large an output capacitor as possible to reduce output voltage ripple.
FB	4	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage.
GND	5	Ground.
VIN	6	Power supply input pin.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.65	5.5	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-1	1	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ECLGA1.5X2-6L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	81.67	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.91	
Ψ_{JB}	Junction-to-board characterization parameter(1)	6.75	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	7.09	
$R_{\theta JA\_EVM}$	Junction to ambient thermal resistance(2)	46.35	

(1) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(2) Simulated on SCT standard EVM: SCT2113M Demo Board, 2oz top and bottom copper thickness, 1oz inner copper thickness, 50mm x 50mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=3.3V, T_J=-40°C~125°C(1), typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.65		5.5	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.55		V
	Hysteresis			110		mV
I_{SD}	Shutdown current			0.05	2.2	μA
I_Q	Quiescent current from VIN	no load, no switching		35	45	μA
V_{FB}	Reference voltage of FB	Tj=25°C	0.594	0.6	0.606	V
		Tj=-40°C~125°C	0.591		0.609	V
I_{FB}	FB pin leakage current				80	nA
Power switch						
$ILIM_{HS}$	High-side peak current limit		1.7	2.16	2.5	A
$ILIM_{LS}$	Low-side valley current limit		1.2	1.6		A
Soft start						
T_{SS}	Soft-start Time			1.5		ms
EN						
V_{ENH}	High-level Threshold voltage		1.2			V
V_{ENL}	Low- level Threshold voltage				0.4	V
R_{EN}	EN Pull down resistance			2		MΩ
R_{DIS}	Output Discharge resistance			240		Ω
Switching Frequency						
F_{SW}	Switching frequency	Vin=3.3V, Vout=1.2V, CCM		2.2		MHz
t_{ON_MIN}(2)	Minimum on-time			60		ns
t_{OFF_MIN}(2)	Minimum off-time			100		ns
Protection						
T_{SD}(2)	Thermal shutdown threshold			160		°C
	Hysteresis			20		°C

(1) Guaranteed by over-temperature correlation. Not tested in production.
(2) Guaranteed by design. Not tested in production.

TYPICAL CHARACTERISTICS

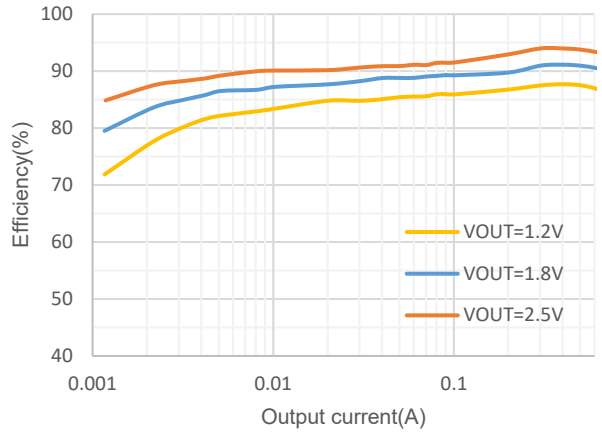


Figure 1. Efficiency vs Load Current, VIN=3.3V

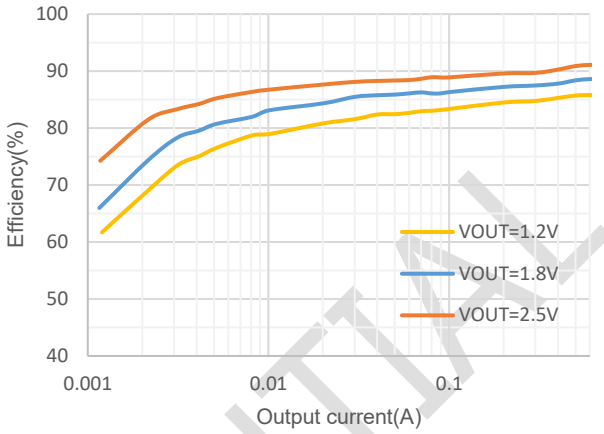


Figure 2. Efficiency vs Load Current, VIN=5V

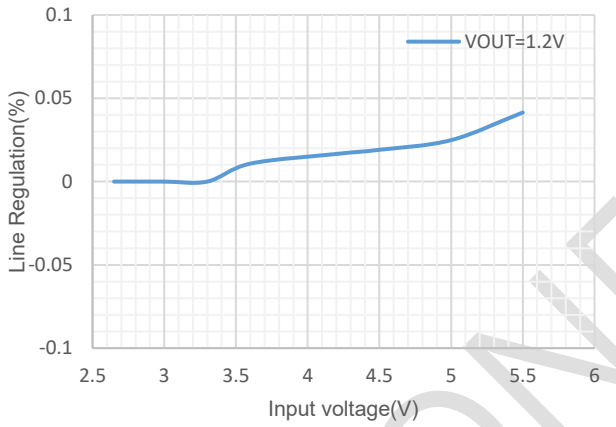


Figure 3. Line Regulation, Io=0.6A

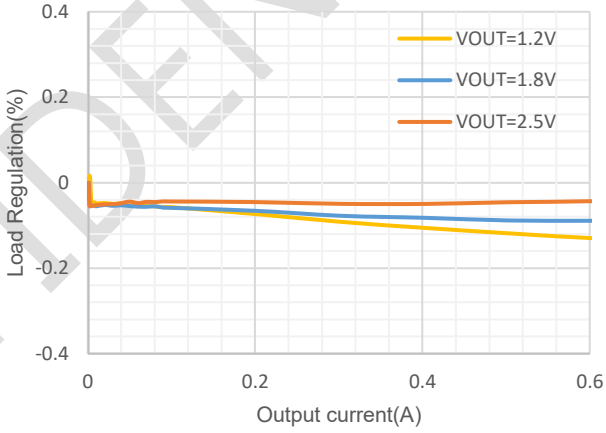


Figure 4. Load Regulation, VIN=3.3V

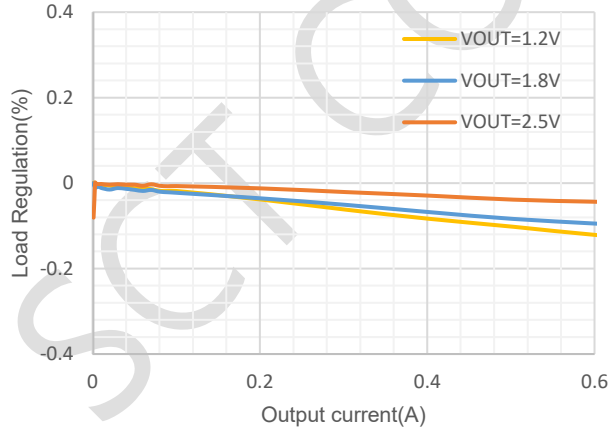
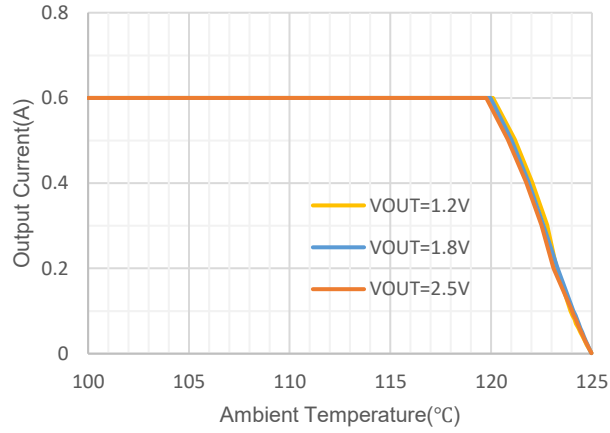


Figure 5. Load Regulation, VIN=5V



PCB=50mm*50mm, 4-Layer,
2oz top and bottom copper, 1oz inner copper
Figure 6. Thermal Derating

FUNCTIONAL BLOCK DIAGRAM

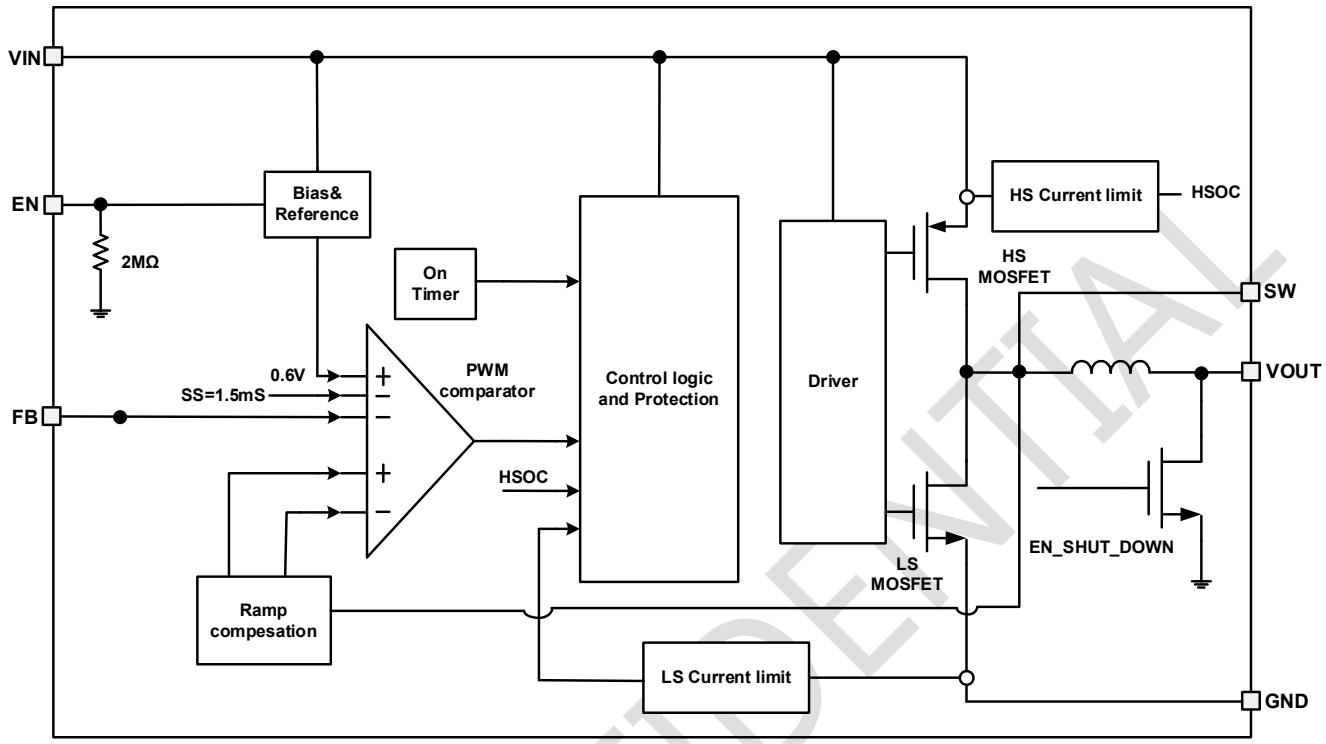


Figure 7. Functional Block Diagram

OPERATION

Overview

The SCT2113M is a 2.65V-5.5V input, 0.6A output, synchronous buck converter with built-in MOSFETs and inductor. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is fixed 2.2MHz. The SCT2113M features integrated soft start time to avoid large inrush current and output voltage overshoot during startup. The SCT2113M operates in Pulse Frequency Modulation (PFM) to achieve high efficiency in light load operation. The quiescent current is typically 35μA under no load and no switching. A 100% maximum duty cycle can be reached in dropout.

Constant On-time Control

Constant on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT2113M turns off high-side MOSFET after the fixed-on time and turns on the low-side MOSFET. SCT2113M turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following Equation 1:

$$t_{\mathrm{ON}} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}} \times f_{SW}} \quad (1)$$

Where:

- VOUT is the output voltage.
- VIN is the input voltage.
- fsw is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.6V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 100ns typically.

Pulse Frequency Modulation (PFM)

The SCT2113M is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.6V, the next ON cycle begins. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{\mathrm{Load}} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

- VOUT is the output voltage.

- VIN is the input voltage.
- Ton is on-time.
- L is the inductance of inductor, and the typical value is 0.47μH.

100% Duty Cycle Mode

The SCT2113M has a 100% duty cycle mode. When the input voltage gradually approaches the output voltage, the duty cycle is large and reaches the minimum turn off time (100nS), the switching frequency of the output voltage begins to decrease. When the input voltage drops to the same level as the output voltage, the high side MOSFET remains constant on.

Under Voltage Lockout UVLO

The SCT2113M Under Voltage Lock Out (UVLO) default startup threshold is typical 2.55V with VIN rising and shutdown threshold is 2.44V with VIN falling.

Enable (EN) and VOUT discharge

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.4V), the chip shuts down. Force EN above its rising threshold voltage (1.2V) to turn the part on. Leave EN floating or pull it down to ground to disable the SCT2113M. There is an internal 2MΩ resistor connected from the EN pin to ground.

When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in VOUT pin provides a discharge path for the output capacitor.

Output Voltage

The SCT2113M regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Soft Start

The SCT2113M has a build in soft start that ramps up the output voltage at a controlled slew rate to avoid overshoot at startup. The soft start time is about 1.5ms typically.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (IL) reaches the high-side MOSFET peak current limit (typically 2.16A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on and stays on until IL drops below the low-side MOSFET valley current limit (typically 1.6A). If output loading continues to increase, output will drop below the V_{UVP}, and SS is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup

waiting time and restart normally after 7 cycles' soft-start period. If overload or hard short condition still exists during soft-start and make FB voltage lower than V_{UVP}, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

Thermal Shutdown

Once the junction temperature in the SCT2113M exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

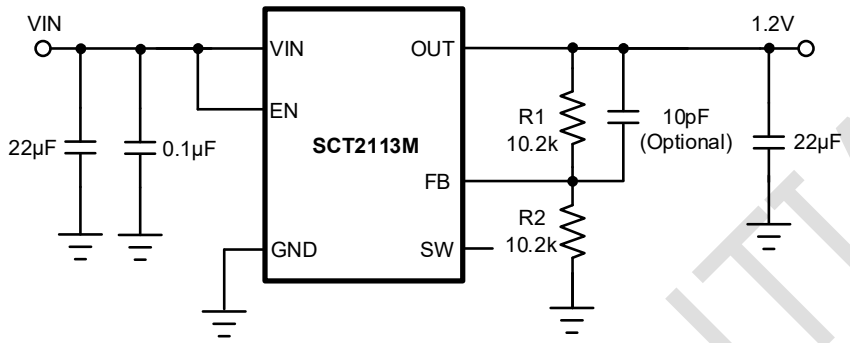


Figure 8. SCT2113M Design Example, 1.2V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.3V Normal 2.65V to 5.5V
Output Voltage	1.2V
Maximum Output Current	0.6A
Switching Frequency	2.2MHz
Output voltage ripple (peak to peak)	3.4mV
Transient Response 0.06A to 0.54A load step	ΔVout =51.2mV

Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2kΩ. Use Equation 4 to calculate R1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \quad (4)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.6V

Table 1. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
1.2 V	10.2 kΩ	10.2 kΩ
1.8 V	20 kΩ	10.2 kΩ
2.5V	32.4 kΩ	10.2 kΩ
3.3 V	68 kΩ	15 kΩ

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 5.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 7 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where:

- ΔV_{IN} is the input voltage ripple.
- F_{sw} is the switching frequency.
- C_{IN} is the input capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

For this example, 22μF, X7R ceramic capacitors rated for 16 V in parallel are used. And a 0.1μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 8 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (8)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor, and the typical value is 0.47μH.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, a 22μF ceramic output capacitors work for most applications.

Table 2: Component List with Typical Output Voltage BOM list

Vout	COUT	R1	R2
1.2V	22μF	10.2kΩ	10.2kΩ
1.8V	22μF	20kΩ	10.2kΩ
2.5V	22μF	32.4kΩ	10.2kΩ
3.3V	22μF	68kΩ	15kΩ

Application Waveforms

V_{IN}=3.3V, V_{OUT}=1.2V, unless otherwise noted

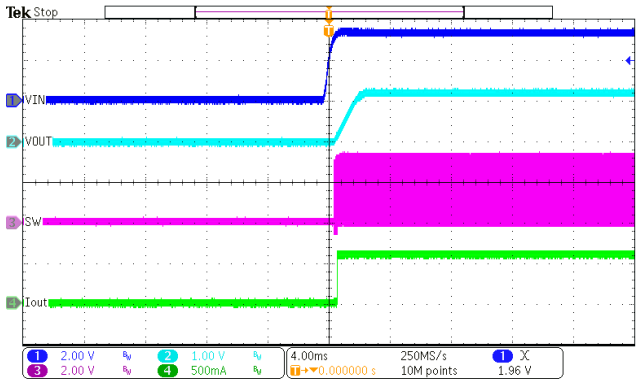


Figure 9. Power up (I_{LOAD}=0.6A)

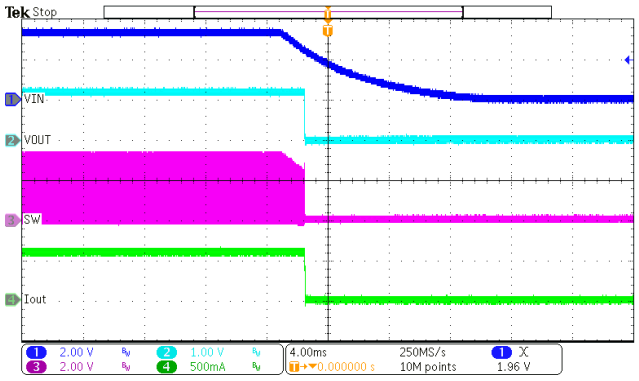


Figure 10. Power down (I_{LOAD}=0.6A)

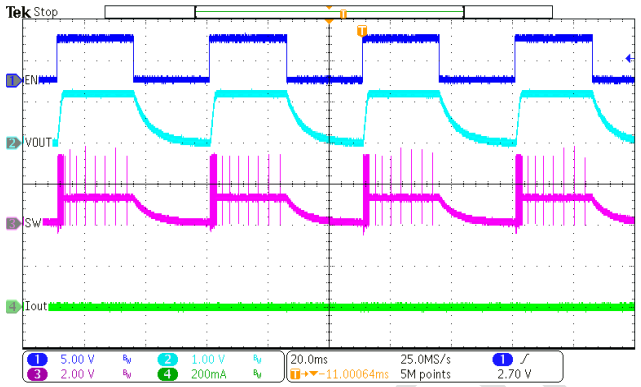


Figure 11. EN toggle (I_{LOAD}=0A)

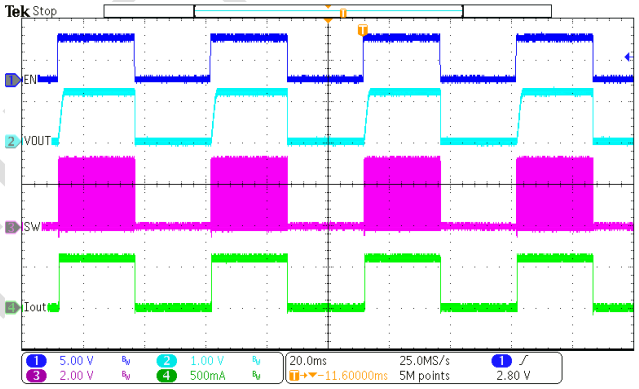


Figure 12. EN toggle (I_{LOAD}=0.6A)

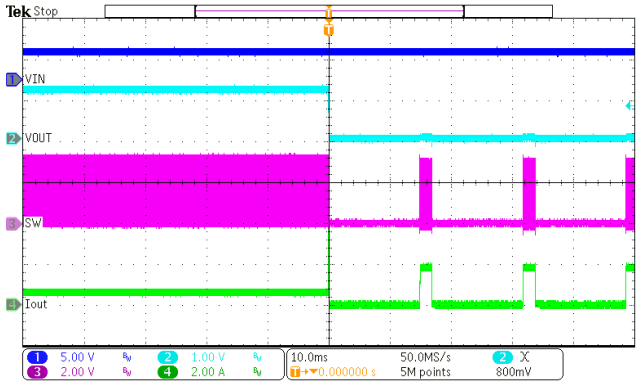


Figure 13. Over Current Protection (0.6A to hard short)

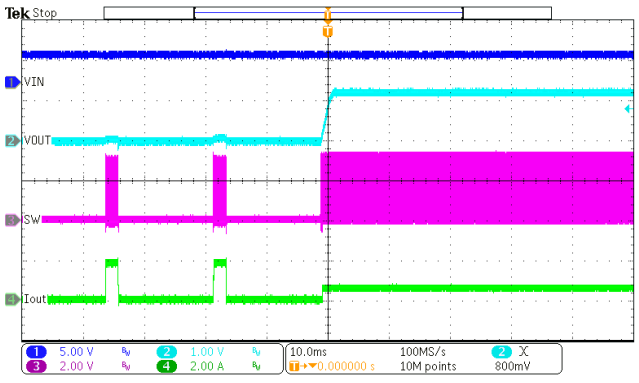


Figure 14. Over Current Release (hard short to 0.6A)

Application Waveforms

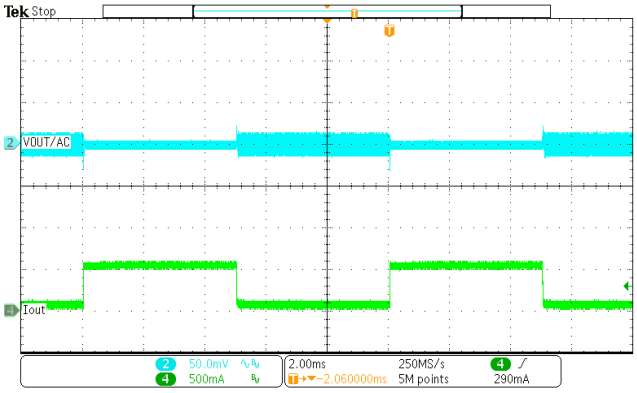


Figure 15. Load Transient (0.06A-0.54A, 1.6A/us)

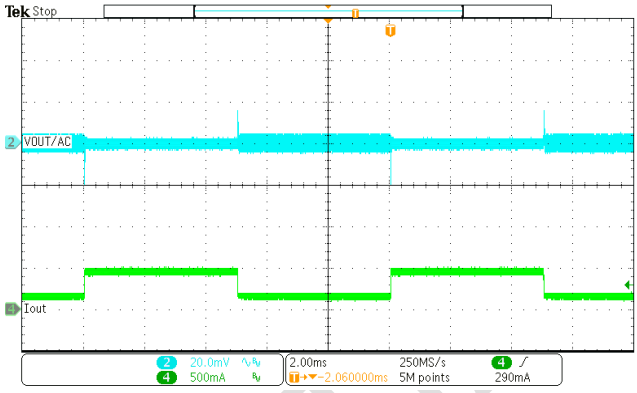


Figure 16. Load Transient (0.15A-0.45A, 1.6A/us)

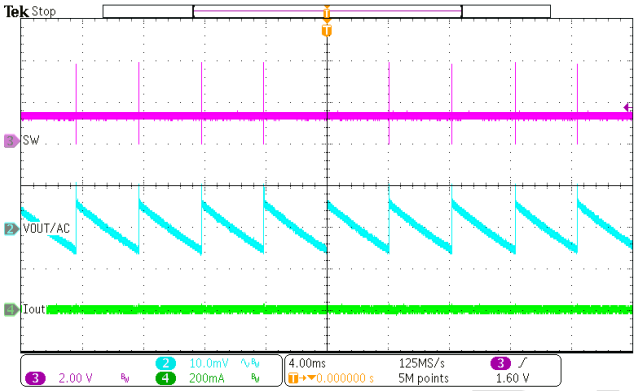


Figure 17. Output Ripple (I_{LOAD}=0A)

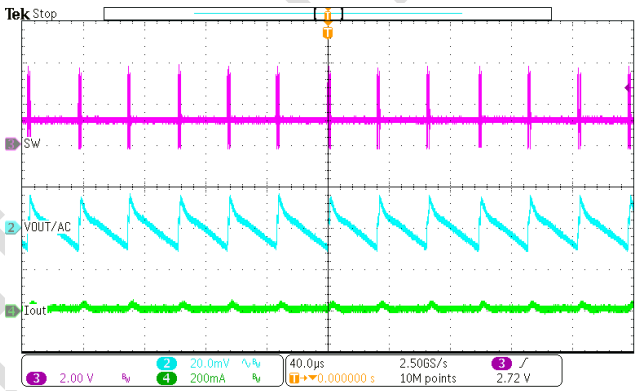


Figure 18. Output Ripple (I_{LOAD}=10mA)

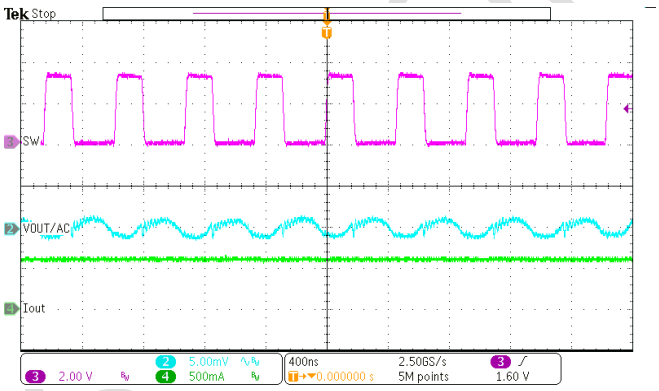


Figure 19. Output Ripple (I_{LOAD}=0.6A)

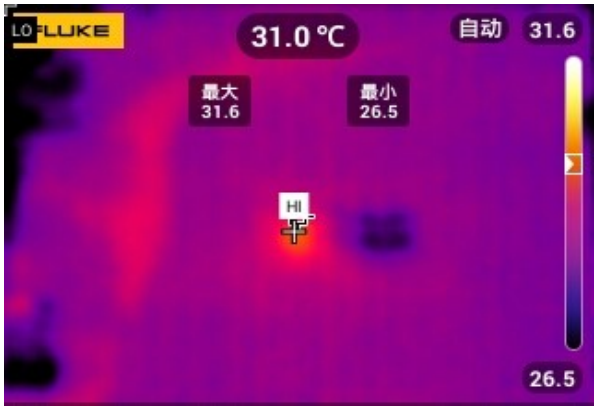


Figure 20. Thermal, VIN=3.3V, VOUT=1.2V, I_{LOAD}=0.6A

Layout Guideline

Proper PCB layout is critical for SCT2113M's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. The FB-bottom divider resistor should be placed as close as possible to the FB and GND pins to minimize the ground loop.

2. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

3. Place a low ESR ceramic capacitor as close as possible to the VIN pin and ground to minimize parasitic effects.

4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power has lower impendence of grounding.

5. Implement a large ground plane on the bottom layer and connect it to the top-layer ground plane using vias to improve thermal dissipation.

6. If testing on the SW is required, minimize the length and area of the SW trace as much as possible

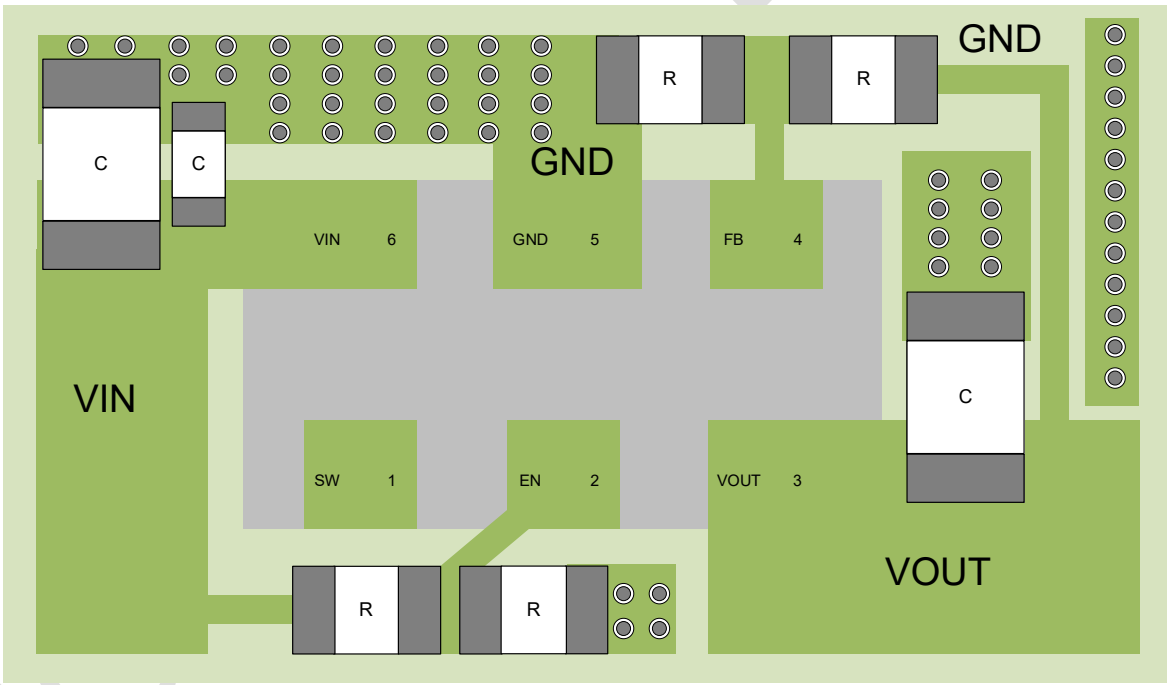
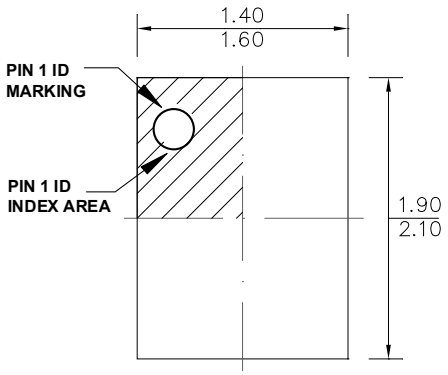
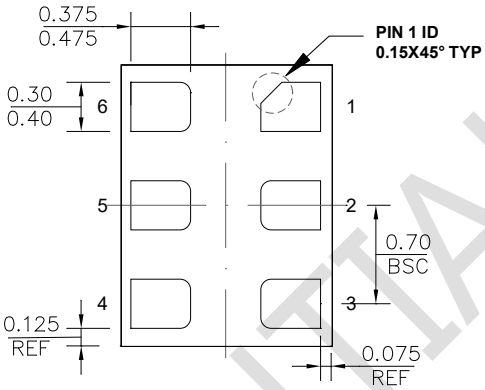


Figure 21. PCB Layout Example

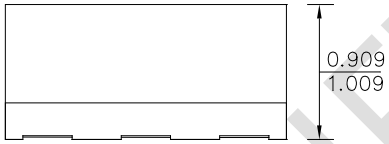
PACKAGE INFORMATION



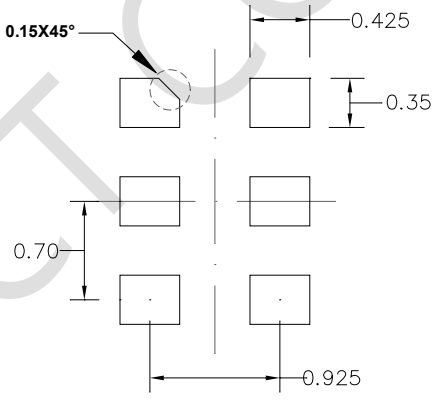
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION

TBD

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