8.5V Vin, 6A, Synchronous Step-down PPD Module™ with integrated inductor

FEATURES

- Wide 2.75V-8.5V Input Voltage Range
- 0.6V-7V Output Voltage Range
- 6A Continuous Output Current
- Programmable Soft-start Time
- Fixed 1.2MHz Switching Frequency
- Selectable PFM, USM and FCCM Operation Modes
- Selectable 8A, 10A and 14A Current Limit
- Cycle-by-Cycle Current Limiting
- Output Over-Voltage Protection
- Over-Temperature Protection
- Available in an ECLGA2.5X3.0-14L Package

APPLICATIONS

- Optical module
- UAV
- FPGA Power System
- Telecom & Networking
- Industrial Equipment

DESCRIPTION

The SCT2260M is a high efficiency synchronous step-down DCDC converter module with 2.75V-8.5V input voltage range and adjustable output voltage down to 0.6V. It offers a small saving ECLGA2.5X3.0-14L package that supplies continuous 6A output current.

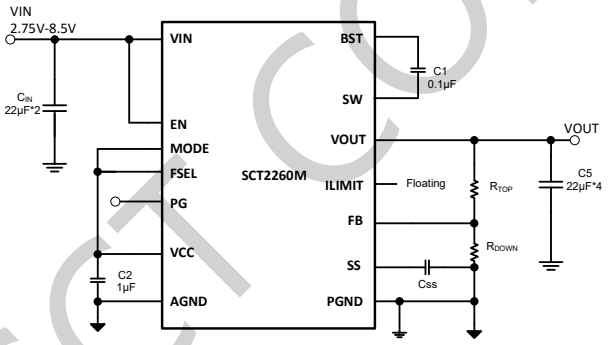
The SCT2260M adopts a Constant On-Time (COT) control to provide fast transient response and easy loop stabilization. With 1.2MHz switching frequency, low output voltage ripple and small capacitor size are achieved. The device offers programmable soft-start time and Power Good indicator with open drain output.

The SCT2260M has the MODE pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save, or Ultrasonic Mode (USM) to keep the switching frequency above audible frequency areas during light-load or no-load conditions, or the FCCM mode to achieve the small output ripple.

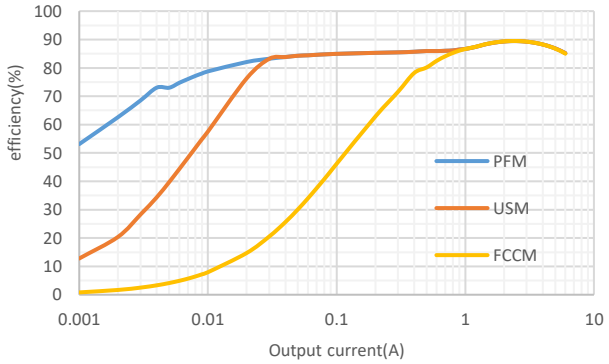
Full protection includes over current protection, under-voltage protection, over-voltage protection and thermal shutdown.

The module requires a minimum number of external components and is available in a ECLGA2.5X3.0-14L package.

TYPICAL APPLICATION



2.75V-8.5V, Synchronous Buck Converter Module



Vin=5V, Vout=1.2V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.6: Preliminary Specification

Revision 0.8: Customer Sample

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PINS	PACKAGE DISCRIPTION	MSL
SCT2260MLNBR	Tape & Reel	5000	14	ECLGA2.5X3.0-14L	3

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	19	V
BST	SW-0.3	SW+6	V
SW	-1	VIN+0.3	V
MODE	-0.3	6	V
FB	-0.3	6	V
FSEL	-0.3	6	V
VOUT	-0.3	VIN+0.3	V
ILIM	-0.3	6	V
SS	-0.3	6	V
PG	-0.3	6	V
Operating junction temperature T_J(2)	-40	125	°C
Storage temperature T_{STG}	-55	125	°C

PIN CONFIGURATION

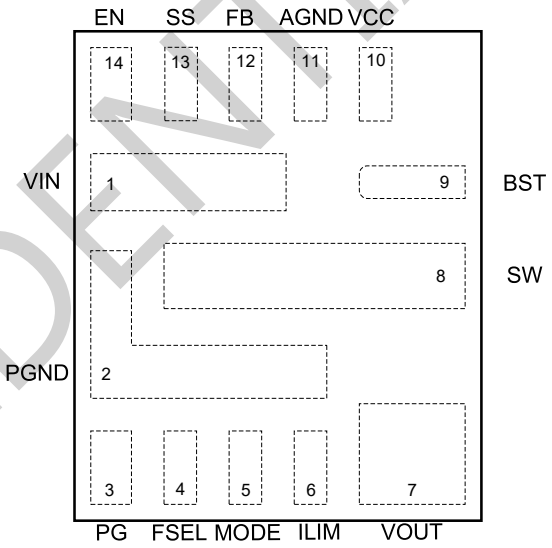


Figure 1. ECLGA-14L
(Top view: 2.5mmx3mm)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
VIN	1	Input voltage. Decouple the input rail with at least 0.1μF input ceramic capacitor. Place the capacitor as close as to VIN and PGND pins as possible. Use wide PCB traces and multiple vias to make the connection. SCT2260M is a high efficiency power converter with 2-3ns fast turning on and turning off power MOSFETs for the best efficiency. If not placing the input capacitor close to VIN and GND pin, the voltage spike caused by trace parasitic inductance might EOS damage the device.
PGND	2	Power ground. Using wide PCB traces and multiple vias large enough to handle the load current.
PG	3	Power good open-drain output. PG is high if the output voltage is higher than 95% or lower than 105% of the nominal voltage.
FSEL	4	Switching frequency configuration. Connecting to VCC sets clock frequency to 1.2MHz.
MODE	5	PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM.
ILIMIT	6	Overcurrent limit selection. The current limit is 8A when the pin is connected to ground, 10A when the pin is floating, and 14A when the pin is pulled up to VCC.
VOUT	7	Power output, please use as large an output capacitor as possible to reduce output voltage ripple.
SW	8	Connect SW to the bootstrap capacitor.
BST	9	Bootstrap. Must connect a 0.1μF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET.
VCC	10	Internal VCC LDO output. The driver and control circuits are powered by VCC. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
AGND	11	Signal logic ground. AGND is the Kelvin connection to PGND.
FB	12	Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical.
SS	13	Place a ceramic cap from this pin to ground to program soft-start time.
EN	14	Enable logic input. EN is a digital input that controls the converter on or off. EN high turns on the device and EN low turns off the device. Connecting to VIN with a 100kΩ pull-up resistor can enable the device.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.75	8.5	V
V_{OUT}	Output voltage range	0.6	7	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2	+2	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins (1)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ECLGA2.5X3-14L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (1)	44.27	°C/W
$R_{\theta JCtop}$	Junction to case thermal resistance (1)	17.69	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	16.69	
$R_{\theta JA\_EVM}$	Junction to ambient thermal resistance (EVM) (2)	33.67	

(1) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(2) Simulated on SCT standard EVM: SCT2260M Demo Board, 1oz top and bottom copper thickness, 0.5 oz inner copper thickness, 75mm x 72.5mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=7V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.75		8.5	V
V_{INUVLO} $V_{INUVLO\ HYS}$	Vin UVLO rising threshold VIN UVLO Hysteresis		2.3	2.4 155	2.7	V mV
I_{SD}	Shutdown current	EN=0V, Measured on VIN pin		1	3	μA
I_Q	Quiescent current from VIN	EN=2V, Vout=5V, No load, No switching. Measured on VIN pin.		160		μA
V_{CC}	V_{CC} internal LDO regulator voltage	I_{VCC}=0mA	4.5	4.7	5	V
V_{CC_LR}	V_{CC} internal LDO load regulation	I_{VCC}=5mA		0.5		%
I_{VCC_LIM}	V_{CC} internal LDO current limit	VCC short to ground		30		mA
Reference and Control Loop						
V_{REF}	Reference voltage of FB	2.75V<Vin<8.5V at Temp=25°C	0.594	0.6	0.606	V
I_{FB}	FB pin leakage current	V_{FB}=1.2V			150	nA
Enable and Soft-start						
V_{EN_H} V_{EN_L}	Enable high threshold Enable low threshold		 1.03	1.2 1.1		V V
I_{EN}	Enable pin pull-up current	EN=1V	0.8	1.2	1.6	μA
T_{SS}	Soft-start time	VOUT 10% to 90%, SS is float		0.8		ms
Operation Mode						
V_{MD_PWM}	FCCM mode with logic high threshold	VCC=5V	4.15			V
V_{MD_USM}	PFM mode with USM logic threshold		1.5		3.5	V
V_{MD_PFM}	PFM mode input logic low threshold				1	V
Switching Frequency						
F_{SW}	Switching frequency	FSEL=VCC		1200		kHz
T_{ON_TIME}	Minimum On-time			60		ns
T_{OFF_TIME}	Minimum Off-time			120		ns
Power Good						
$PG_{Rising(in)}$	V_{FB} rising, percentage of V_{REF} (Good)			95		%
$PG_{Falling(in)}$	V_{FB} falling, percentage of V_{REF}			85		%
$PG_{Rising(out)}$	V_{FB} rising, percentage of V_{REF}			115		%
$PG_{Fallng(out)}$	V_{FB} falling, percentage of V_{REF} (Good)			105		%
PG_{TD}	PG low to high delay			0.5		ms
V_{PG}	Power Good PG pull-down strength	I_{PG} =4mA		0.4		V
I_{PG_LEAK}	Power Good PG leakage current	VPG=5V			5	μA

Protection				
I_{LIM_P}	LS MOSFET positive current limit	From source to drain，ILIMIT connects to GND	8	A
		From source to drain，ILIMIT floating	10	A
		From source to drain，ILIMIT connects to VCC	14	A
I_{LIM_N}	LS MOSFET negative current limit	From drain to source, MODE connects to VCC	5	A
V_{OVP_R}	V_{FB} OVP threshold % of V_{REF}	V_{FB} rising	122	%
V_{OVP_F}	V_{FB} OVP threshold % of V_{REF}	V_{FB} falling	117	%
V_{UVP_F}	V_{FB} UVP threshold % of V_{REF}	V_{FB} falling	75	%
T_{SD}	Thermal shutdown threshold	T_J rising	160	°C
	Hysteresis		30	°C

TYPICAL CHARACTERISTICS

Unless otherwise noted, the following conditions are VIN=5V, Temperature=25°C.

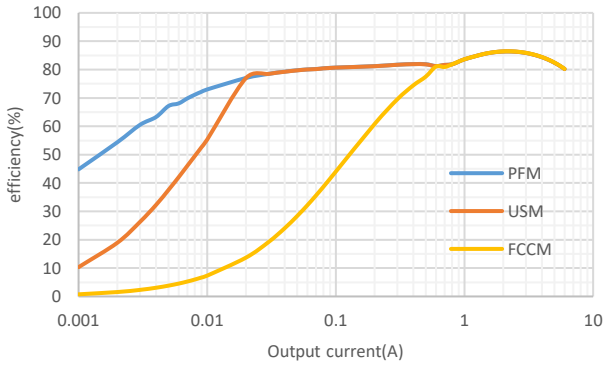


Figure 2. Efficiency, Vout=0.8V

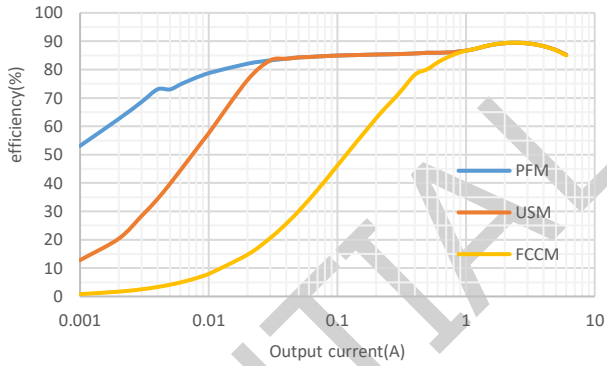


Figure 3. Efficiency, Vout=1.2V

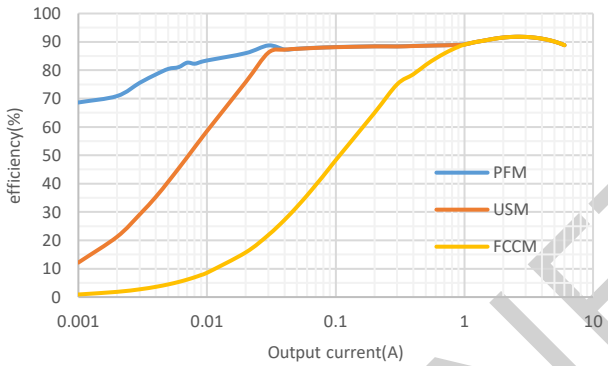


Figure 4. Efficiency, Vout=1.8V

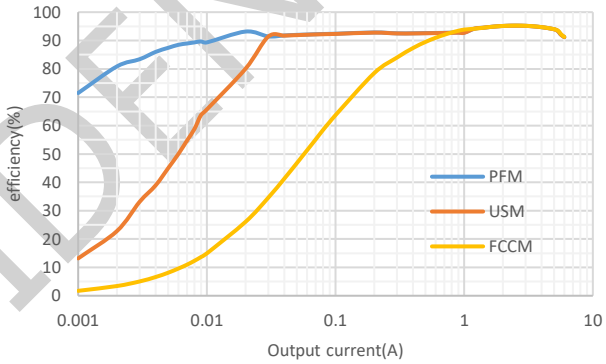


Figure 5. Efficiency, Vout=3.3V

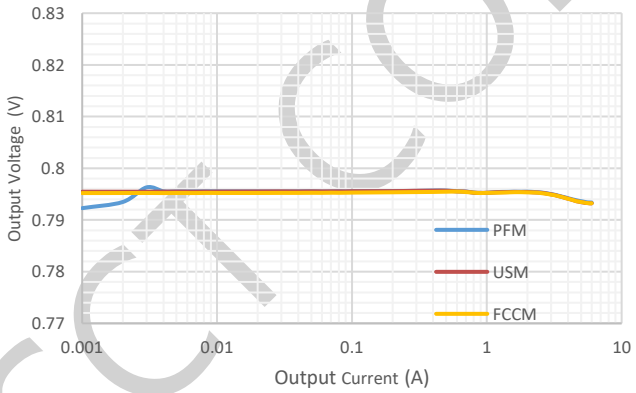


Figure 6. Load Regulation, Vout=0.8V

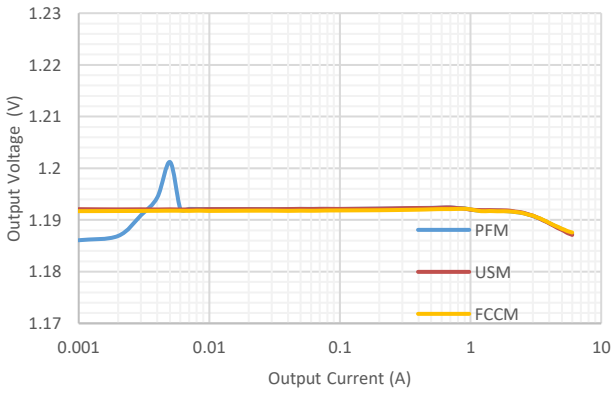


Figure 7. Load Regulation, Vout=1.2V

TYPICAL CHARACTERISTICS

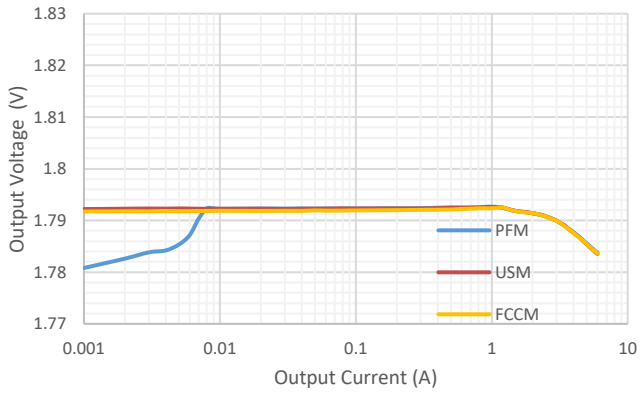


Figure 8. Load Regulation, Vout=1.8V

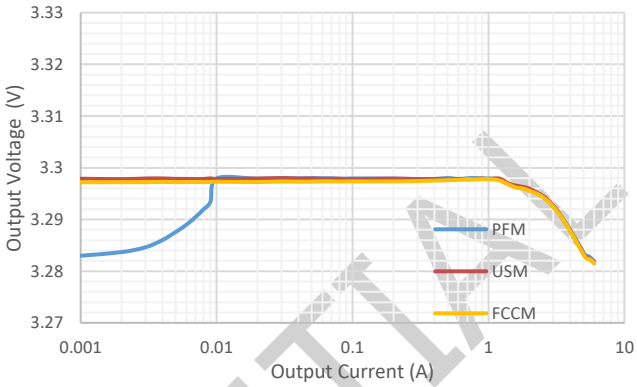


Figure 9. Load Regulation, Vout=3.3V

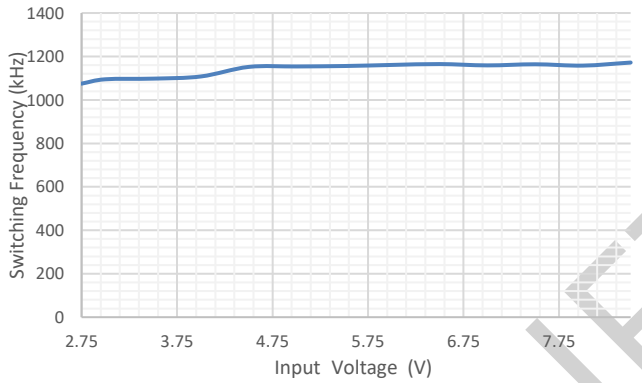


Figure 10. Switching Frequency VS Input Voltage

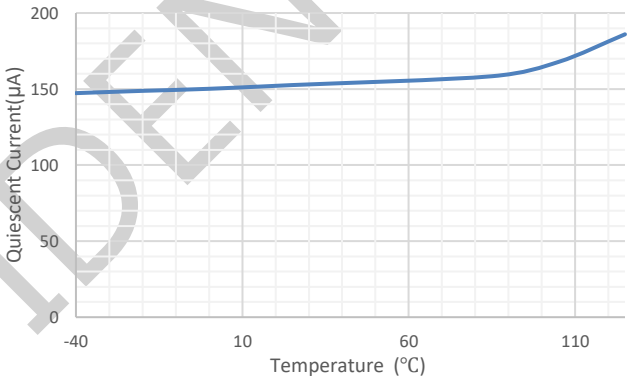


Figure 11. Quiescent Current VS Temperature

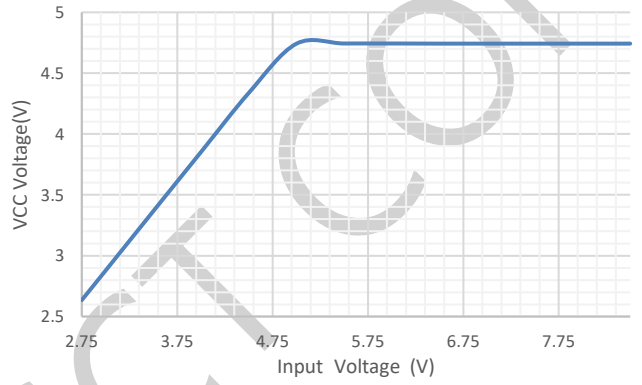
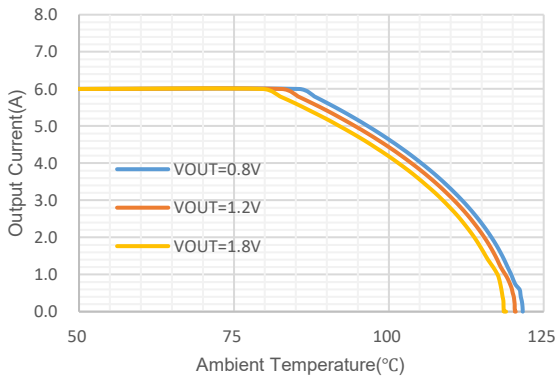


Figure 12. VCC Voltage vs Input Voltage



PCB=75mm*72.5mm, 4-Layer,
1 oz top and bottom copper, 0.5 oz inner copper
Figure 13. Thermal Derating

FUNCTIONAL BLOCK DIAGRAM

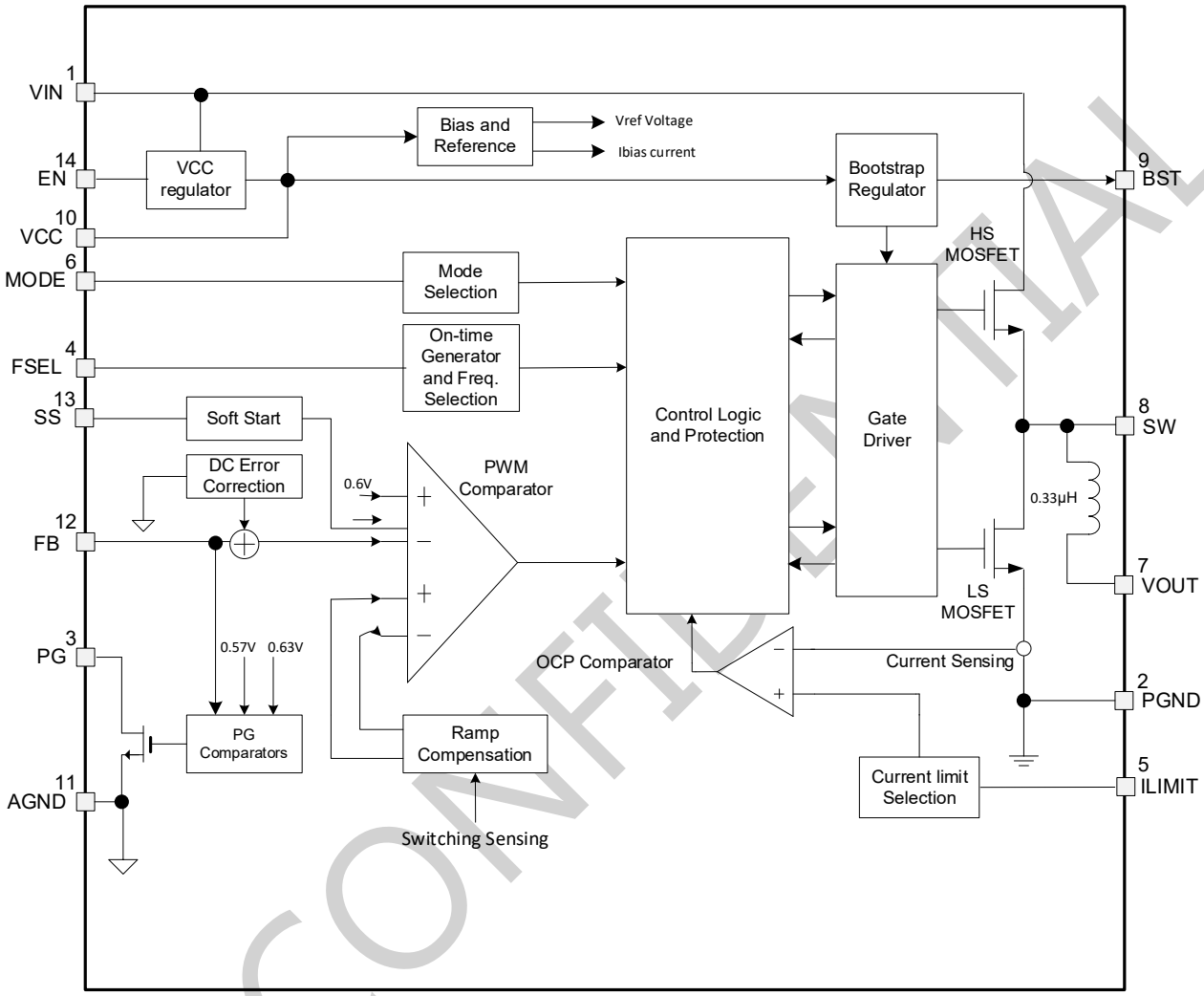


Figure 14. Functional Block Diagram

OPERATION

Overview

The SCT2260M is a 2.75V-8.5V input, 6A continuous synchronous step-down converter module with a shielded inductor. It implements the Constant on-time (COT) mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

Frequency Modulation (PFM) mode, Ultra-Sonic Modulation (USM) mode and Force Pulse Width Modulation (FCCM) mode. The quiescent current is typically 130μA under no load and sleep mode condition to achieve high efficiency at light load.

The SCT2260M has a default input start-up voltage of 2.4V with 155mV hysteresis. The EN function features with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN with a 100kΩ resistor starts up the device automatically.

The SCT2260M full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant on-time (COT) Mode Control

The SCT2260M employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and output voltage. After the on-time, the Q1 turns off and the low-side MOSFET (Q2) turns on after dead time duration. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreased below the VFB, the Q1 turns during one on-time after another dead time duration. This repeats on cycle-by-cycle based.

The SCT2260M works with an internal compensation for optimizing the loop stability and transient response.

Pulse Frequency Modulation (PFM) and Ultra-sonic Modulation (USM) Modes

Grounding the MODE pin makes the SCT2260M works at Pulse Frequency Modulation (PFM) mode to improve the power efficiency in light load. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current.

Floating the MODE pin makes the device working at PFM with Ultra-Sonic Modulation (USM) mode to keep the switching frequency out of the acoustic audible frequency. The USM mode block monitors the state of both high-side and low-side MOSFETs. When both high-side and low-side MOSFETs are off for 40us, the low-side MOSFET forces to turn on until the negative current limit is triggered or the feedback voltage (VFB) drops below the internal reference voltage (VRFE).

Forced Pulse Width Modulation (FCCM) Mode

Connecting MODE pin to VCC, the SCT2260M forces the device operating at Forced Pulse Width Modulation (FCCM) mode with pseudo-fixed switching frequency regardless of loading current. Operating in PWM mode can achieve smaller output voltage ripple compared with PFM or USM at light load. When the load current approaches zero, the low-side MOSFET current crosses zero and sinks current from output to maintain the constant output. Hence power efficiency in light load is much lower than heavy load.

Enable and Under Voltage Lockout Threshold

The SCT2260M is enabled when the VIN pin voltage rises above 2.75V and the EN pin voltage exceeds the enable

threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 2.345V or when the EN pin voltage is below 1.1V. An internal 1.5μA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 15 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.2 * \left(1 + \frac{R1}{R2}\right) - 1.5\mu A * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 1.5\mu A * R1 \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

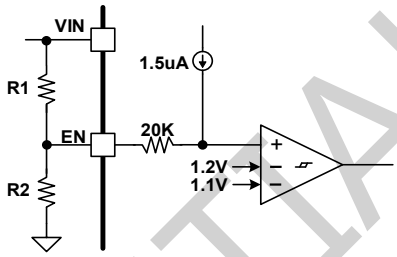


Figure 15. System UVLO by enable divide

Output Voltage

The SCT2260M regulates the internal reference voltage at 0.6V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Programmable Soft-Start

The SCT2260M features programmable soft-start time to prevent inrush current during start-up stage. The soft-start time can be programmed easily by connecting a soft-start capacitor C_{ss} from SS pin to ground.

The SS pin sources an internal 5μA current charging the external soft-start capacitor C_{ss} when the EN pin exceeds turn-on threshold. The device adopts the lower voltage between the internal voltage reference 0.6V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 0.6V.

The soft-start capacitor value can be calculated going with following Equation (4). Attention should be taken here that the programmed soft-start time should be larger than 0.8ms.

$$C_{soft-start} = t_{ss} * \frac{5uA}{0.6V} \quad (4)$$

Where:

- C_{SS} is the soft-start capacitor connected from SS pin to the ground
- t_{ss} is the soft-start time

Overcurrent Limit Selection

The current limit of the SCT2260M is selectable to be one of three options: 8A, 10A and 14A. The current limit selection is programmed by LIMIT pin. The selection information shown in following table. The current limit setting

is latched in at each power up and not be able to be modified during operation. Cycling the input power or the EN pin can reselect the current limit.

Table 1. LIMIT Pin Set-up for Current limit Selection

LIMIT Set-up	Connect to GND	Floating	Connect to VCC
Current Limit	8A	10A	14A

Mode Selection

The SCT2260M features three different operation modes at light load by easily programming the MODE pin. The programming information is listed in following table. The mode setting is latched in at each power up and is not able to be modified during operation. Cycling the input power or the EN pin can reselect the switching frequency.

Table 2. MODE Pin Set-up for Mode Selection

MODE Set-up	Connect to GND	Floating	Connect to VCC
Mode	PFM	PFM with USM	FCCM

Power Good (PG)

The Power Good (PG) pin is the output of an open drain output. When the FB pin is typically between 95% and 105% of V_{REF} the PG is de-asserted and floats after a 500μs de-glitch time. A pull-up resistor of 10 kΩ to 100 kΩ is recommended to pull it up to VCC. The PG pin is pulled low when the FB pin voltage falls under 85% or rises over 115% of V_{REF}, including UVP and OVP; or, in an event of thermal shutdown or during the soft-start period.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from 5V VCC power when high-side power MOSFET is off and low-side power MOSFET is on.

Over Current Limit and Hiccup Mode

The output over-current limit (OCL) is implemented in SCT2260M by using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state of the high-side FET (Q1) by measuring the low-side FET(Q2) drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current IOUT.

If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. When the current is limited, the output voltage tends to drop because the load demand is higher than what the converter can support. After soft start end with 0.8ms waiting time, when the output voltage falls below 75% of the target voltage, the UVP comparator detects it and shuts down the device immediately. The device re-starts after a hiccup delay of 13*t_{ss}(13 times the soft-start time). When the overcurrent condition is removed, the output voltage returns to the regulated value.

The hiccup protection mode above makes the average short circuit current lower to alleviate thermal issues and protect the regulator.

Under-voltage Protection

The SCT2260M features the Under-voltage Protection (UVP) by monitoring the output voltage to detect the under-voltage voltage. When the feedback voltage falls below 75% of V_{REF}, the SCT2260M enters hiccup mode until the under-voltage scenario released.

Over-voltage Protection

The SCT2260M implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When the feedback voltage rises higher than 122% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on until trigger negative current limit or FB below reference voltage. Then HS-FET turns on with normal ON-time and turn off, following with a LS-FET on until negative current limited triggered or FB lower than reference voltage. The device exits this regulation period when the feedback voltage falls below 117% of the reference voltage.

Thermal Shutdown

The SCT2260M protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 160°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 130°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

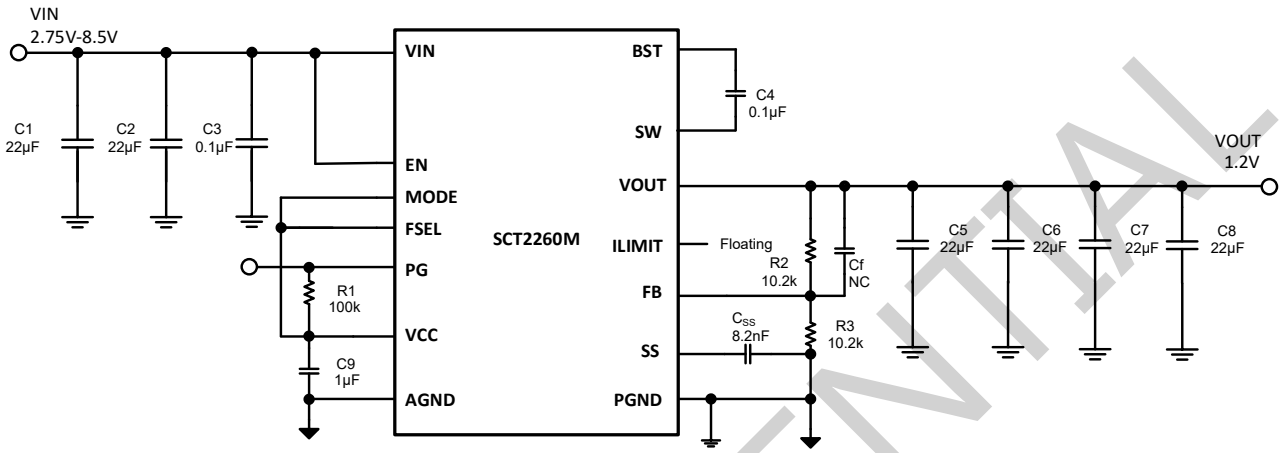


Figure 16. SCT2260M Design Example, 1.2V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal, 2.75V to 8.5V
Output Voltage	1.2V
Maximum Output Current	6A
Switching Frequency	1200kHz
Output voltage ripple (peak to peak)	6mV

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2260M.

Use Equation 5 to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, two 25V/22uF input ceramic capacitors are recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance. The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 6 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^{\ 2} * L * C_{OUT} * V_{IN}} \quad (6)$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications.

Output Feedback Resistor Divider Selection

The SCT2260M features external programmable output voltage by using a resistor divider network R2 and R3 as shown in the typical application circuit Figure 16. Use Equation 7 to calculate the resistor divider values.

$$R_2 = \frac{(V_{OUT} - V_{ref}) \times R_3}{V_{ref}} \quad (7)$$

Table 3 Recommended Component Values for Typical Output Voltage (Vin=5V)

Fsw (kHz)	Vout (V)	Cout (μF)	R2 (kΩ)	R3 (kΩ)	Cf (pF)
1200	0.8	88	3.4	10.2	N/A
	1.2	88	10.2	10.2	100
	3.3	88	45.9	10.2	220

Application Waveforms

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.2V, Temperature=25°C.

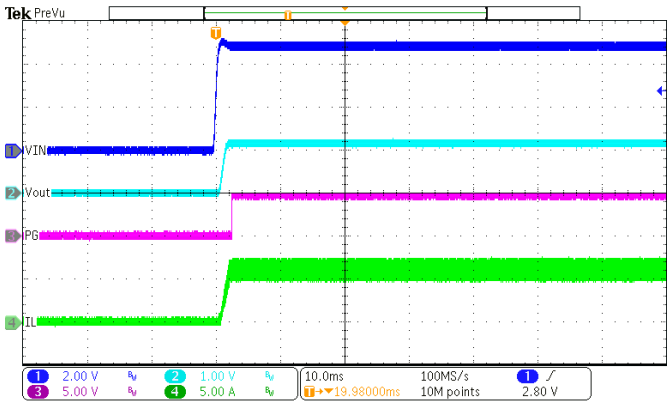


Figure 17. Power up

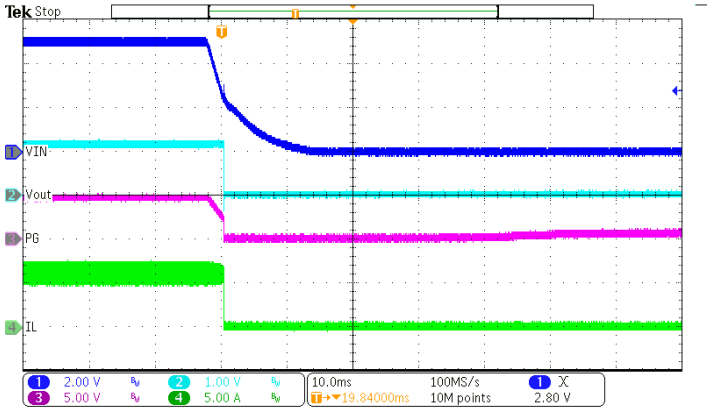


Figure 18. Power down

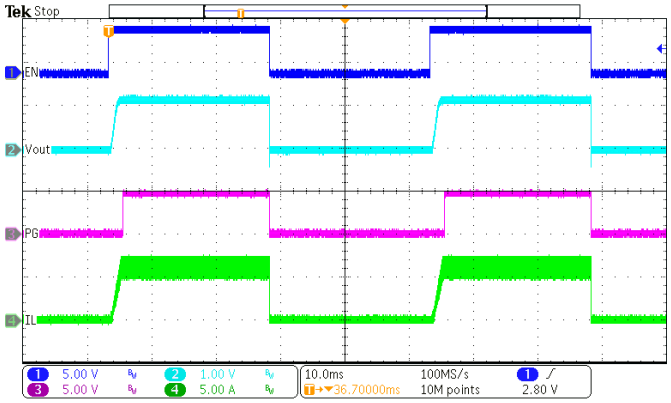


Figure 19. EN toggle (Iload=6A)

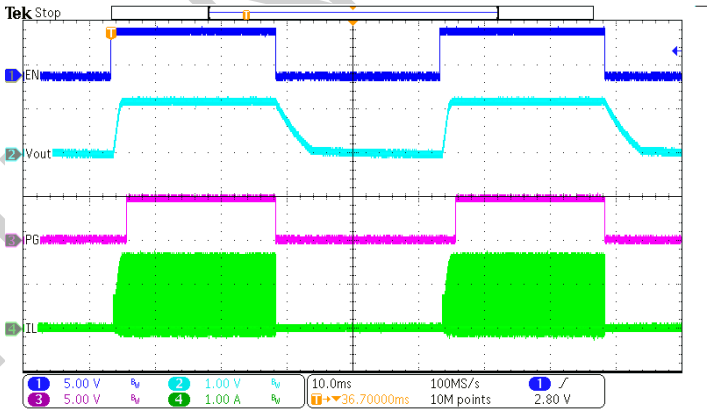


Figure 20. EN toggle PFM (Iload=10mA)

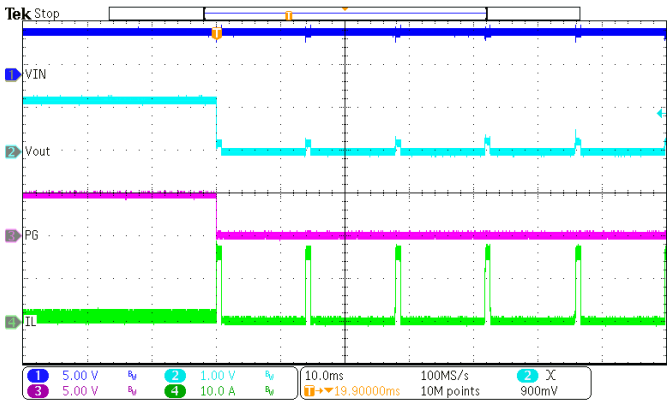


Figure 21. Over Current Protection(1A to hard short) ILIMIT=14A

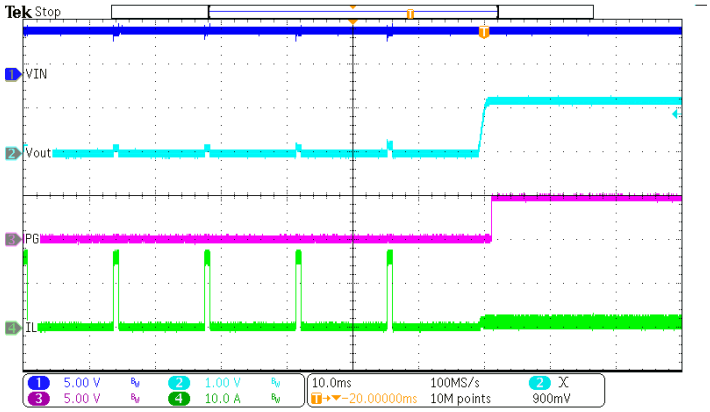


Figure 22. Over Current Release (hard short to 1A)

Application Waveforms(Continued)

Unless otherwise noted, the following conditions are VIN=5V, VOUT=1.2V, Temperature=25°C.

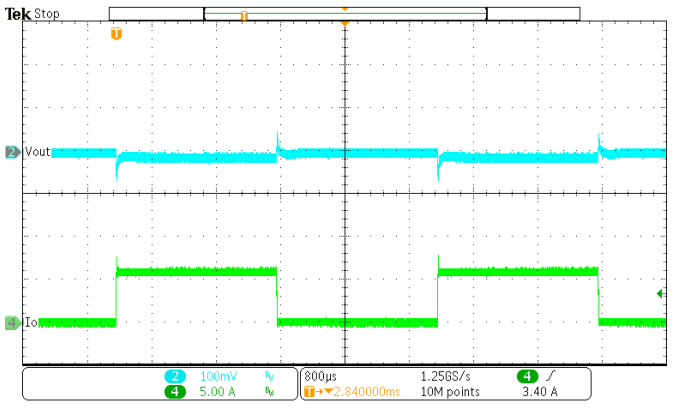


Figure 23. Load Transient (0A-6A, 1.6A/µs)

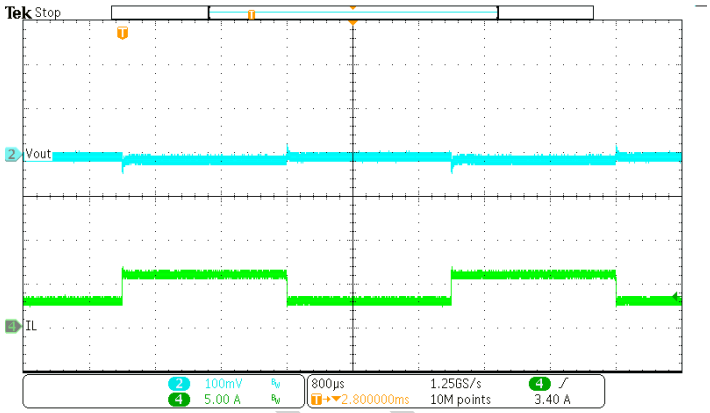


Figure 24. Load Transient (3A-6A, 1.6A/µs)

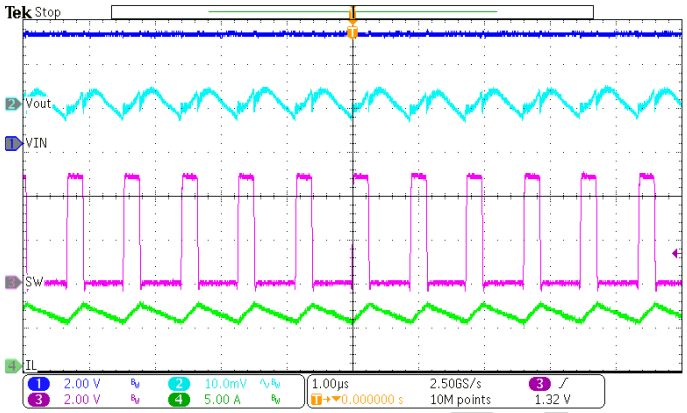


Figure 25. Output Ripple (Iload=6A) 1200kHz

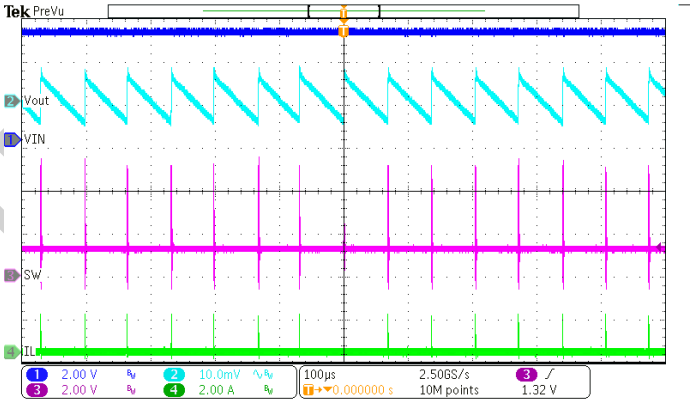


Figure 26. Output Ripple (Iload=10mA, PFM)

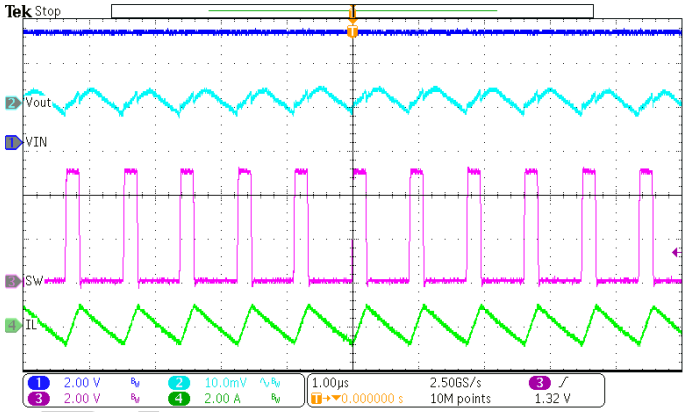


Figure 27. Output Ripple (Iload=10mA, FCCM)

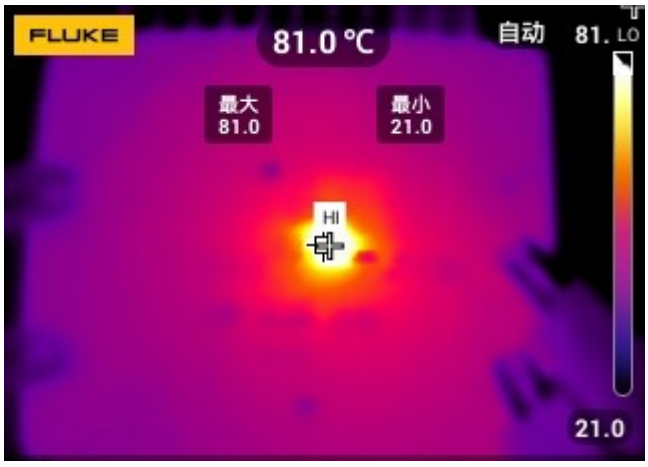


Figure 28. Thermal, 5 VIN, 1.2 Vout, 6A

Layout Guideline

Proper PCB layout is a critical for SCT2260M's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. For operation at full rated load, the top side ground area must provide adequate heat dissipating area.
3. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
4. UVLO adjust and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
5. Route BST resistor and capacitor with a minimized length between the BST PIN and SW PIN.

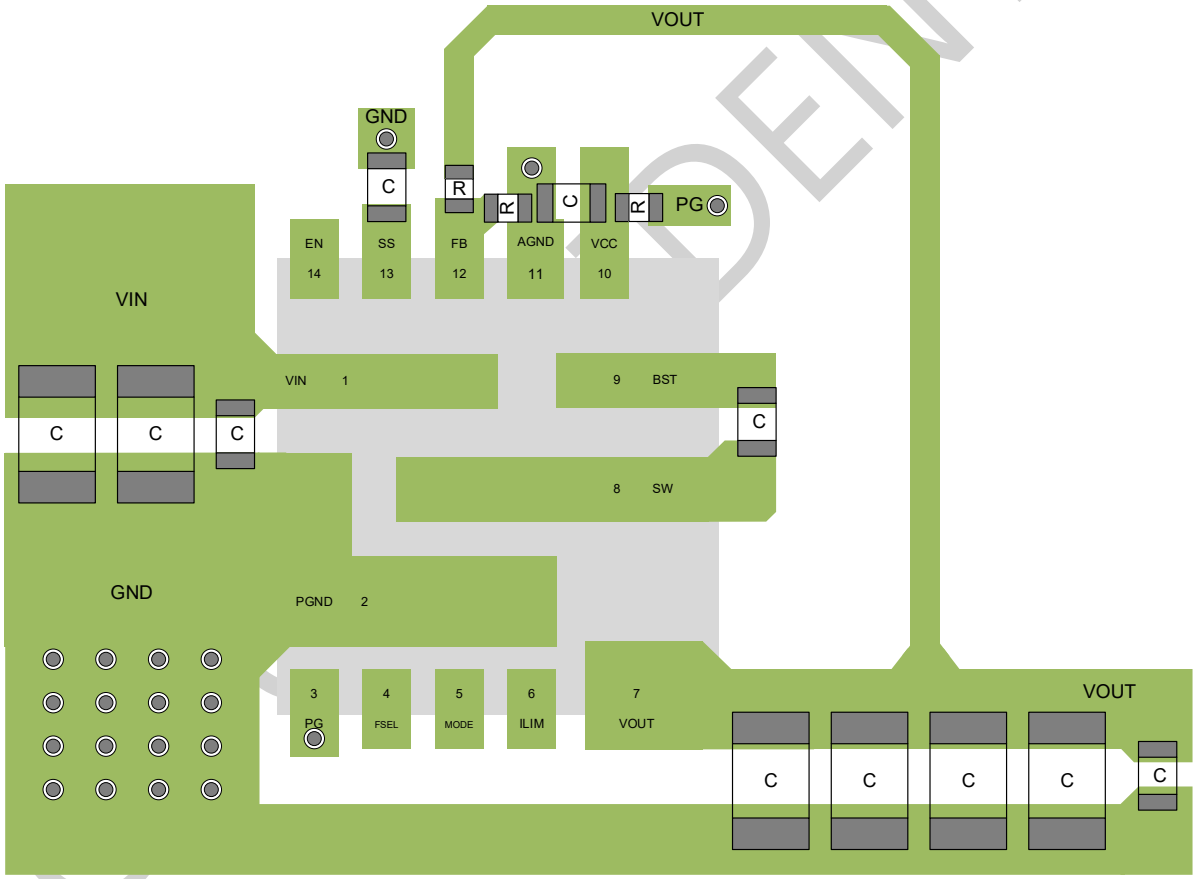
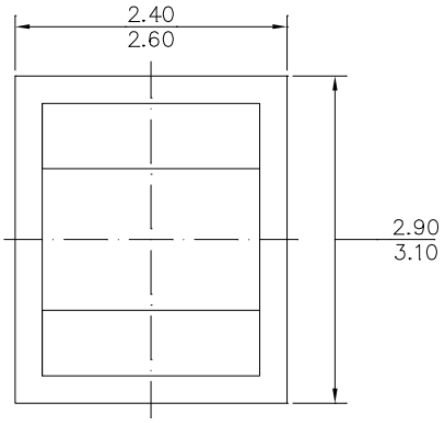
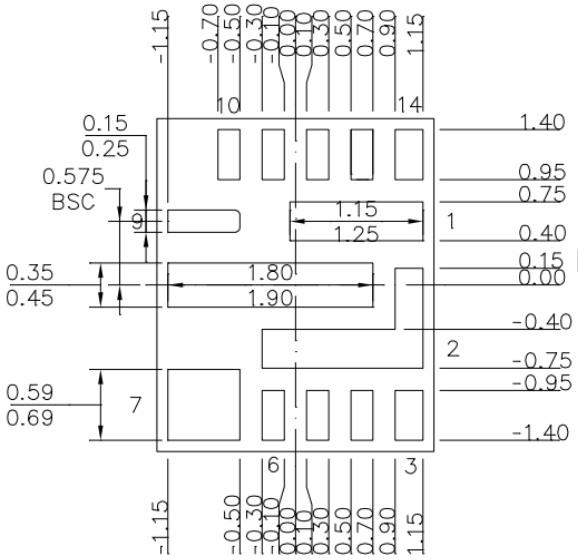


Figure 29. PCB Layout Example

PACKAGE INFORMATION

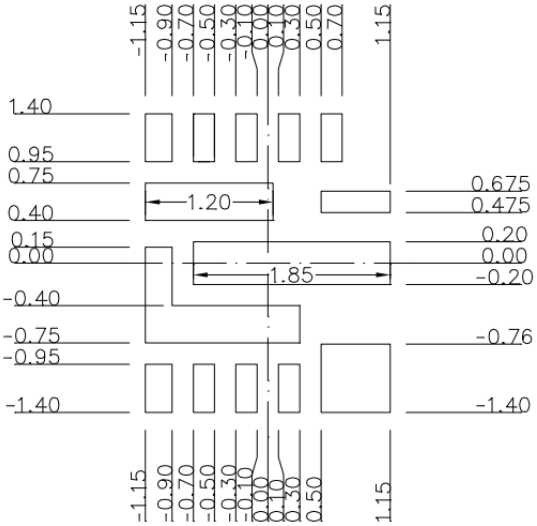


TOP VIEW



BOTTOM VIEW

SIDE VIEW

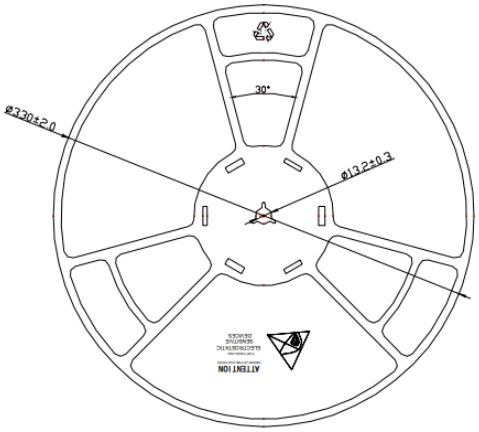


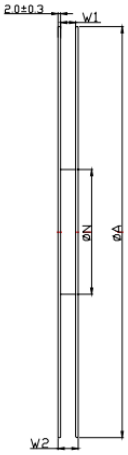
RECOMMENDED LAND PATTERN

NOTE:

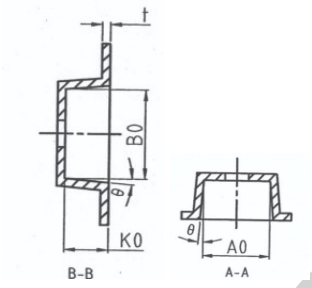
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3. JEDEC REFERENCE IS MO-220.
4. DRAWING IS NOT TO SCALE.

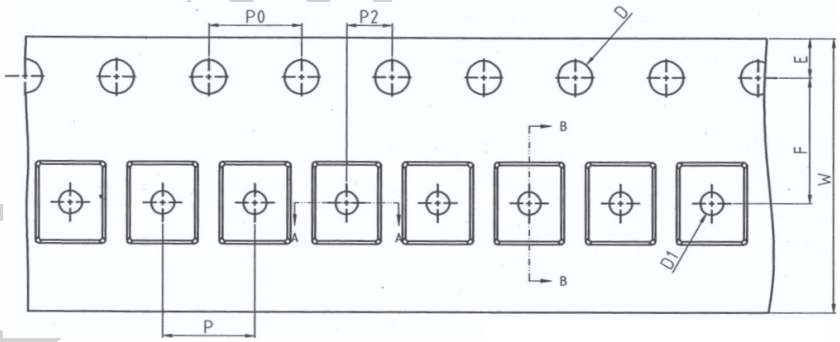
TAPE AND REEL INFORMATION





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
W1	12.4	-	-
W2	-	-	19.4
ØA	328	330	332
ØN	99	100	101





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
E	1.65	1.75	1.85
F	5.45	5.50	5.55
P_2	1.95	2.00	2.05
D	1.50	1.50	1.60
D_1	0.90	1.00	1.10
P_0	3.90	4.00	4.10
$10P_0$	39.80	40.00	40.20
W	11.90	12.00	12.30
P	3.90	4.00	4.10
A_0	2.70	2.80	2.90
B_0	3.20	3.30	3.40
K_0	1.57	1.62	1.67
T	0.25	0.30	0.35
θ	-	5°	-

