4.6V-28V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction

FEATURES

- EMI Reduction with Switching Node Ringing-free
- 410kHz Switching Frequency with ±6% Frequency Spread Spectrum (FSS)
- Pulse Skipping Mode PSM with 40uA Quiescent Current in Light Load Condition
- 4.6V-28V Wide Input Voltage Range
- Up to 3A Continuous Output Load Current
- 0.605V Feedback Reference Voltage
- Fully Integrated 110mΩ R_{dson} High Side MOSFET and 60mΩ R_{dson} Low Side MOSFET
- 1.5uA Shut-down Current
- Low Drop-out Function
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- 3ms Built-in Soft Start Time
- Output Over Voltage and Over Current Protection
- Thermal Shutdown Protection at 160°C
- Available in FCSOT23-6L Package

APPLICATIONS

- White Goods, Home Appliance
- Surveillance
- Audio, Wi-Fi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

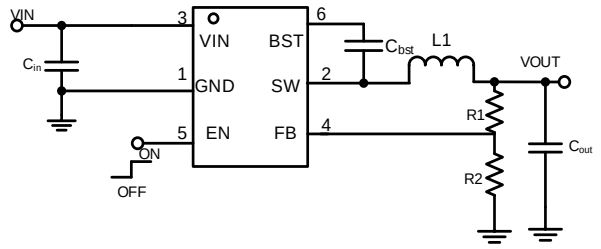
DESCRIPTION

The SCT2330D is 3A synchronous buck converters with up to 28V wide input voltage range, which fully integrates an 110mΩ high-side MOSFET and a 60mΩ low-side MOSFET to provide high efficiency step-down DC-DC conversion. The SCT2330D adopts peak current mode control with the integrated compensation network, which makes SCT2330D easily to be used by minimizing the off-chip component count. The SCT2330D supports the Pulse Skipping Modulation (PSM) with typical 40uA Low Quiescent.

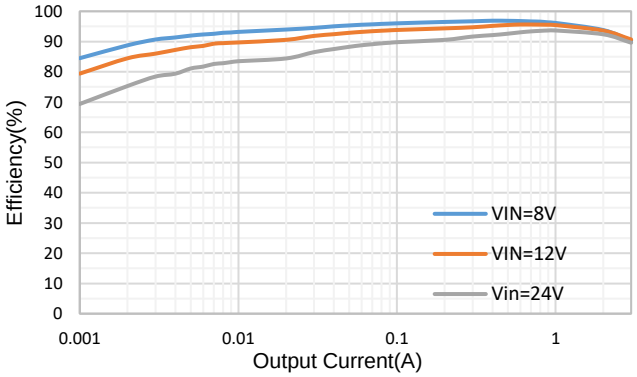
The SCT2330D is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2330D features Frequency Spread Spectrum FSS with ±6% jittering span of the 410kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The SCT2330D offers output over-voltage protection, cycle-by-cycle peak current limit, hiccup protection, and thermal shutdown protection. The device is available in a low-profile FCSOT23-6L package.

TYPICAL APPLICATION



4.6V-28V, synchronous Buck Converter



Efficiency, Vout=5V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

DEVICE ORDER INFORMATION

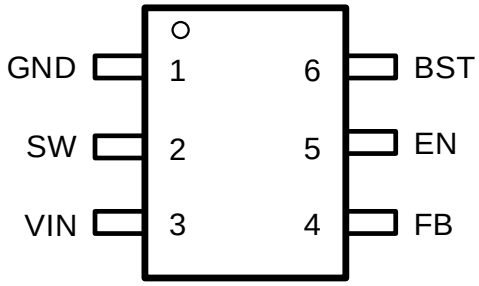
ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2330DTVDR	Tape & Reel	3000	330D	6	FCSOT23-6L	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
BST	-0.3	38	V
VIN (2)	-0.3	32	V
SW	-0.3	32	V
SW (<10ns) (3)	-3	32	V
BST-SW	-0.3	5.5	V
EN, FB	-0.3	5.5	V
Operating junction temperature (4)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: FCSOT23-6L, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
GND	1	Power ground. Must be soldered directly to ground plane.
SW	2	Switching node of the buck converter. Connect SW to an external power inductor.
VIN	3	Power supply input. Must be locally bypassed.
FB	4	Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage
EN	5	Enable logic input. Floating the pin enables the device.
BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.6	28	V
V_{OUT}	Output voltage range	0.6	20	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	- 2.5	+ 2.5	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	- 2	+ 2	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCSOT23-6L	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	91.86	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	12.73	
Ψ_{JB} (2)	Junction-to-board characterization parameter	24.25	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	103.16	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	24.5	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	65.61	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	8.83	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2330D is mounted. The PCB board is a heat sink that is soldered to the leads of the SCT2330D. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(3) Measured on SCT standard EVM: SCT2330D Demo Board, Outer layer 1oz and inner layer 0.5oz copper thickness, 55mm x 40mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.6		28	V
V_{IN_UVLO}	Input UVLO Hysteresis	V_{IN} rising		4.3 300	4.6	V mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V		1.5	5	uA
I_Q	Quiescent current	EN=floating, No load, No switching. VIN=12V. BST-SW=5V		40	100	uA
Enable						
V_{EN_H}	Enable high threshold			1.25	1.4	V
V_{EN_L}	Enable low threshold		1.1	1.23		V
I_{EN}	Enable pin input current	EN=1V		0.7		uA
I_{EN_HYS}	Enable pin hysteresis current	EN=1.5V		1.55		uA
Power MOSFETs						
R_{DSON_H}	High side FET on-resistance			110	160	mΩ
R_{DSON_L}	Low side FET on-resistance			60	90	mΩ
Feedback and Error Amplifier						
V_{FB}	Feedback Voltage		580	605	630	mV
Current Limit						
I_{LIM_HSD}	HSD peak current limit		4.3	5.3	6.3	A
I_{LIM_LSD}	LSD valley current limit		2.8	3.8	5	A
T_{HIC_W}*	OCP hiccup wait time			16		cycle
T_{HIC_R}*	OCP hiccup restart time			40		ms
Switching Frequency						
F_{SW}	Switching frequency	V_{IN}=12V, V_{OUT}=5V	320	410	500	kHz
t_{ON_MIN}*	Minimum on-time			90		ns
t_{OFF_MIN}*	Minimum off-time			110		ns
t_{ON_MAX}*	Maximum on-time			10		us
F_{JITTER}	FSS jittering span			±6		%
Soft Start Time						
t_{SS}	Internal soft-start time		1	3	7	ms
Protection						
V_{OVP}	Output OVP threshold Hysteresis	V_{OUT} rising		110 5		% %
V_{BOOTUV}		BOOT-SW falling Hysteresis		2.4 250		V mV
T_{SD}*	Thermal shutdown threshold Hysteresis	T_J rising		160 25		°C

*Derived from bench characterization or design function.

TYPICAL CHARACTERISTICS

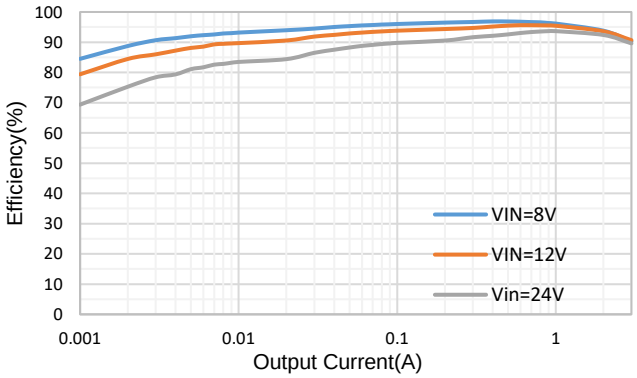


Figure 1. Efficiency vs Load Current, Vout=5V

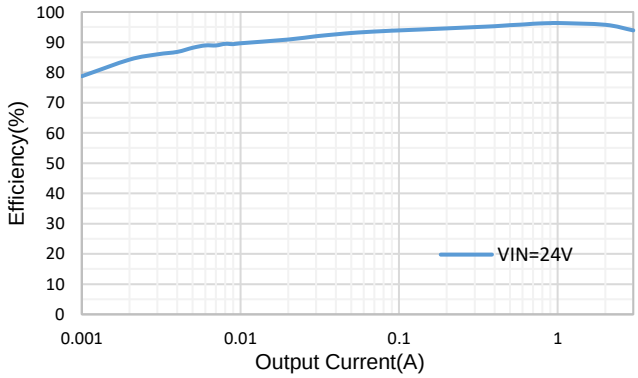


Figure 2. Efficiency vs Load Current, Vout=12V

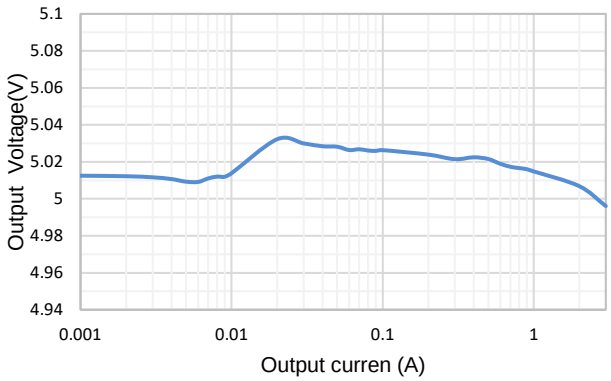


Figure 3. Load Regulation, Vin=12V, Vout=5V

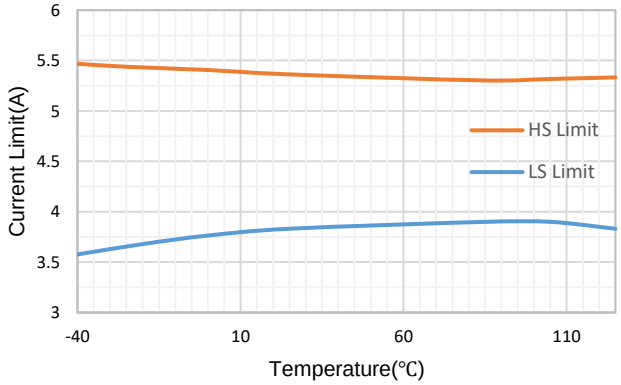


Figure 4. Current Limit VS Temperature

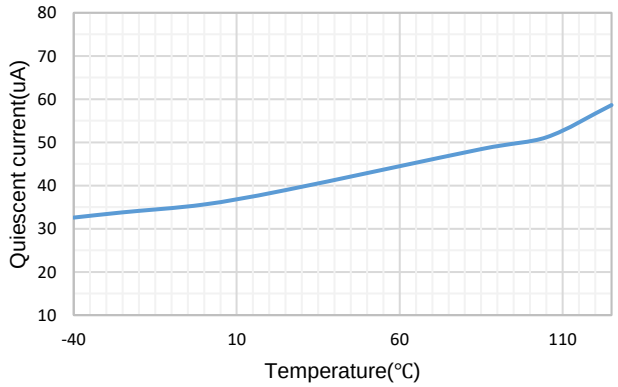


Figure 5. Quiescent Current VS Temperature

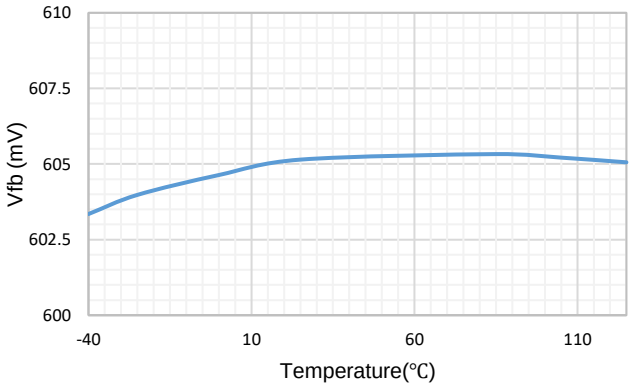


Figure 6. Reference voltage VS Temperature

FUNCTIONAL BLOCK DIAGRAM

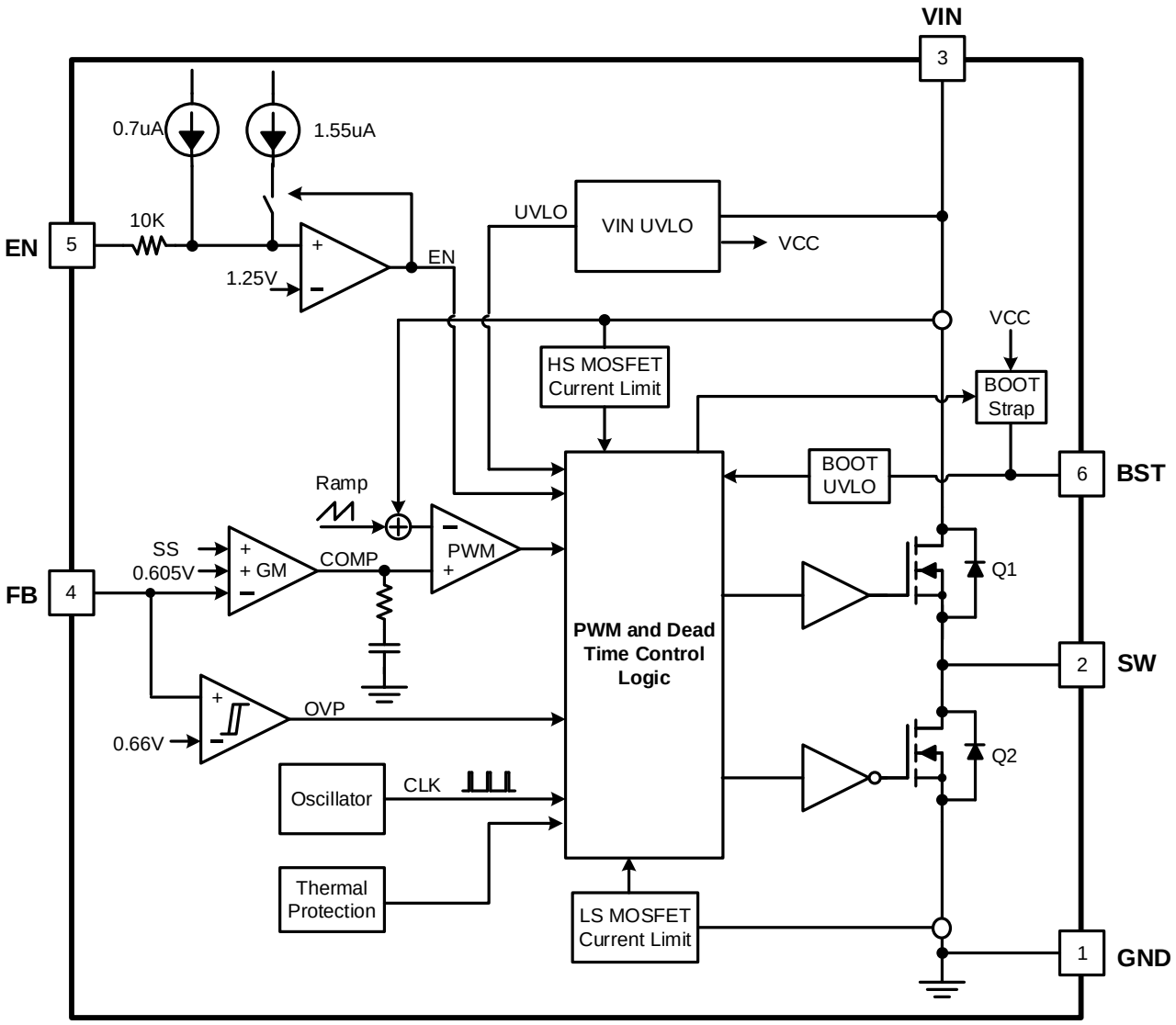


Figure7. Functional Block Diagram

OPERATION

Overview

The SCT2330D device is 4.6V-28V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 410kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 3ms soft-start simplify the SCT2330D footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.605V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT2330D is 40uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1.5μA. The SCT2330D works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition.

The SCT2330D implements the Frequency Spread Spectrum (FSS) modulation spreading of ±6% centered 410kHz switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 16 cycles and the hiccup restart time is 40ms. The SCT2330D device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2330D is designed to operate from an input voltage supply range between 4.6V to 28V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2330D Under Voltage Lock Out (UVLO) default startup threshold is typical 4.3V with VIN rising and shutdown threshold is 4V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.25V/rise), the SCT2330D enables all functions and the device starts soft-start phase. The SCT2330D has the built in 3ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.23V/fall).

An internal 0.7uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 1.55uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by Equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

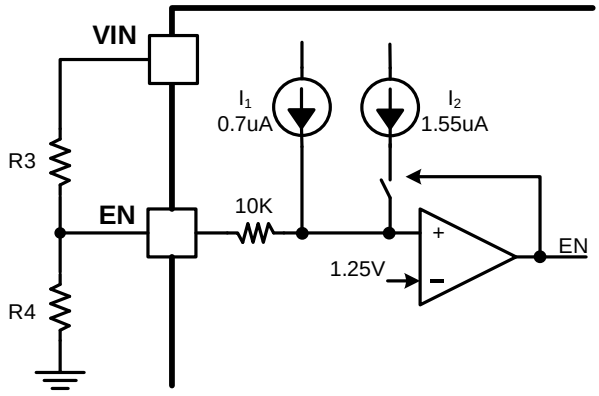


Figure 8. Adjustable VIN UVLO

$$R3 = \frac{V_{Start}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{Stop}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (1)$$

$$R4 = \frac{R_3 \times V_{ENF}}{V_{Stop} - V_{ENF} + R_3(I_1 + I_2)} \quad (2)$$

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=0.7uA
I_2=1.55uA
V_{ENR}=1.25V
V_{ENF}=1.23V

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

To improve EMI performance, SCT2330D adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT2330D features 410kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency. As a result, the harmonic wave amplitude is reduced, and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2330D implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the

converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

Peak Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2330D implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage. When COMP voltage is clamped for 16 switching cycles, the converter stops switching. After remaining OFF for 40ms，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high, after soft start time and COMP keep high for 16 switching cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over Voltage Protection and Minimum On-time

SCT2330D features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage (0.605V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 90ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

PSM Working Modes

In heavy load condition, the SCT2330D forces the device operating at forced Pulse Width Modulation (PWM) mode. When the load current decreasing, the internal COMP net voltage decreases as the inductor current down. With the load current further decreasing, the COMP net voltage decreases and be clamped at a voltage corresponding to the 500mA peak inductor current. When the load current approaches zero, the SCT2330D enter Pulse Skipping Mode (PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light, and converter works in PSM mode.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.65V rising and hysteresis of 250mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.4V, BST UVLO occurs. The SCT2330D intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT2330D. When VIN is close to output voltage and minimum off time is triggered, switching on time will be extended to avoid output voltage drops, switching frequency will decrease accordingly. After maximum On-time is triggered, SW will be in max duty cycle operation. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high.

During ultra-low voltage difference of input and output voltages, i.e., the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

The minimum operating frequency limit of about 85kHz can also effectively prevent audio noise interference caused by switching frequency when working with large duty cycle.

Thermal Shutdown

Once the junction temperature in the SCT2330D exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

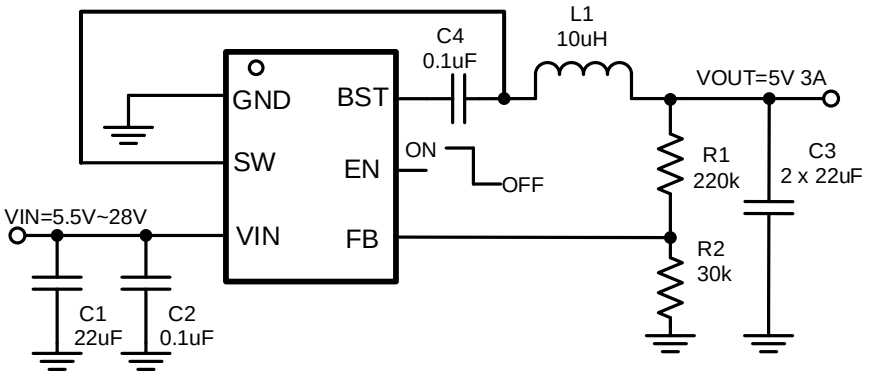


Figure 9. 12V Input, 5V/3A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V typical, 5.5~28V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	8mV
Switching Frequency	410kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 22μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2330D.

Use Equation (3) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where:

- C_{IN} is the input capacitor value
- f_{sw} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to minimize the input voltage ripple. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in Equation (4).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (4)$$

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as in Equation (5).

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (5)$$

Set the current limit of the SCT2330D higher than the peak current and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5.3A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5.3A. Because of the maximum ILPEAK limited by device, the maximum output current that the SCT2330D can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation (6) desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (6)$$

Where:

- ΔV_{OUT} is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

Output Feedback Resistor Divider Selection

The SCT2330D features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure10. Use Equation (7) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (7)$$

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

Table 1. Recommended External Components

Vout	L1	COUT	R1	R2
3.3V	6.5uH	2*22uF	135k	30k
5V	10uH	2*22uF	220k	30k
12V	15uH	3*22uF	570k	30k

Application Waveforms

V_{IN}=12V, V_{OUT}=5V, unless otherwise noted

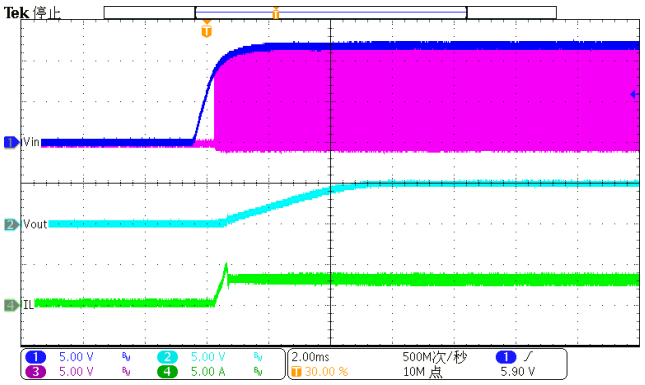


Figure 10. Power up (I_{LOAD}=3A)

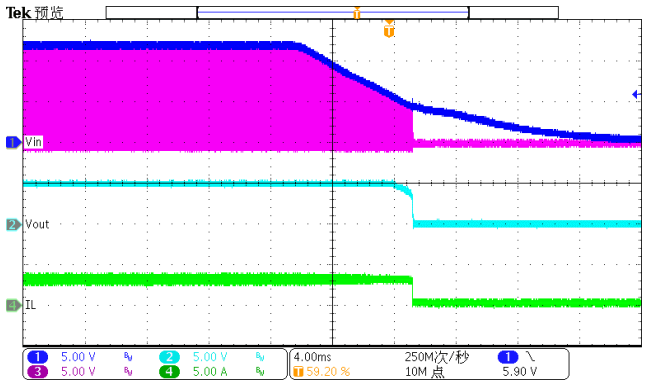


Figure 11. Power down (I_{LOAD}=3A)

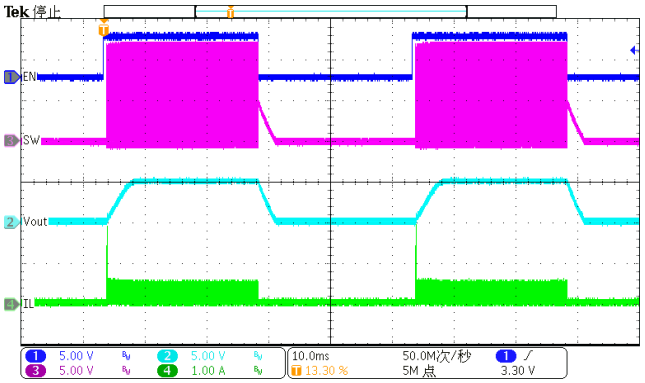


Figure 12. EN toggle (I_{LOAD}=0.1A)

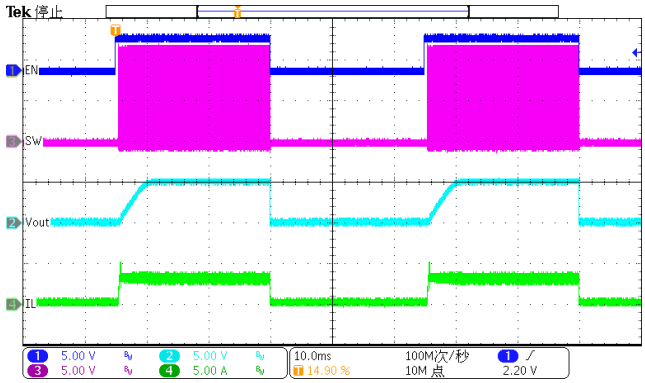


Figure 13. EN toggle (I_{LOAD}=3A)

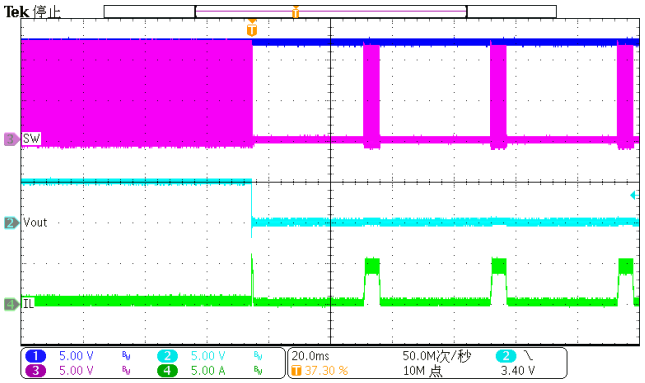


Figure 14. Over Current Protection (0.1A to hard short)

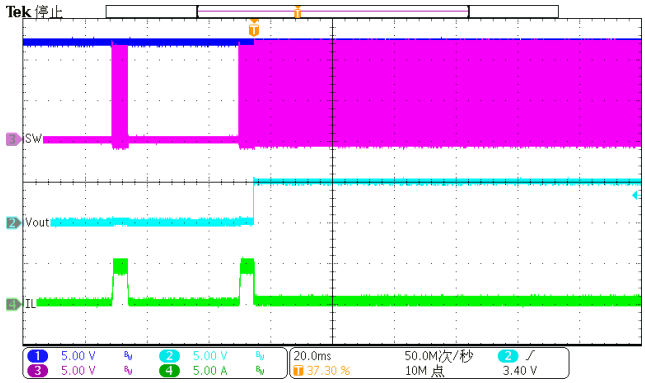


Figure 15. Over Current Release (hard short to 0.1A)

Application Waveforms

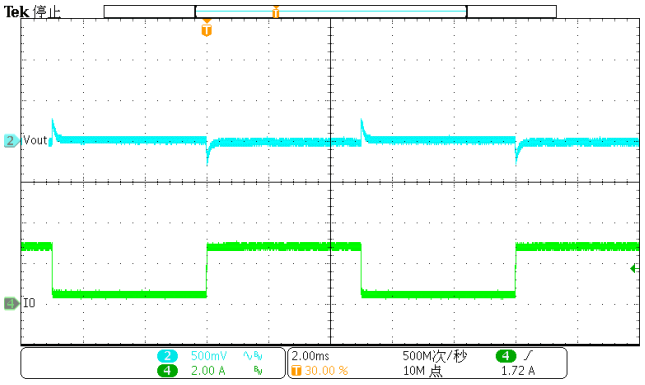


Figure 16. Load Transient (0.3A~2.7A, 1.6A/us)

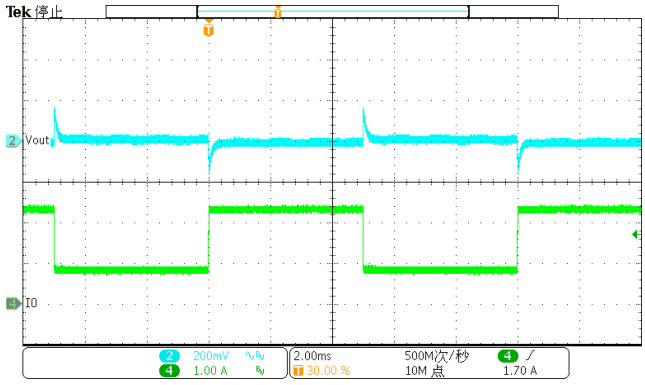


Figure 17. Load Transient (0.75A~2.25A, 1.6A/us)

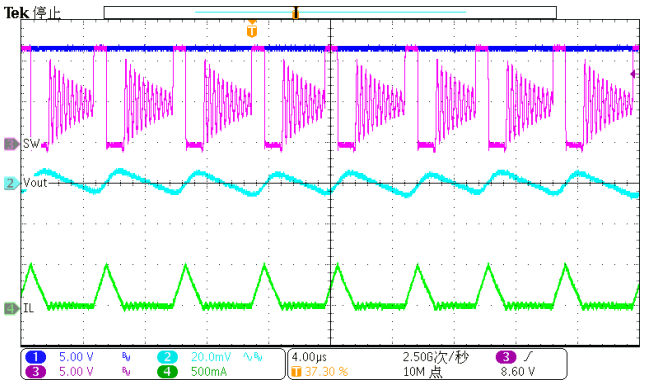


Figure 18. Output Ripple (I_{LOAD}=0.1A)

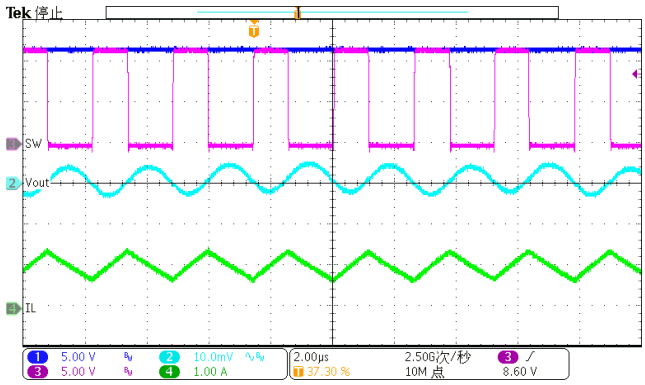


Figure 19. Output Ripple (I_{LOAD}=1A)

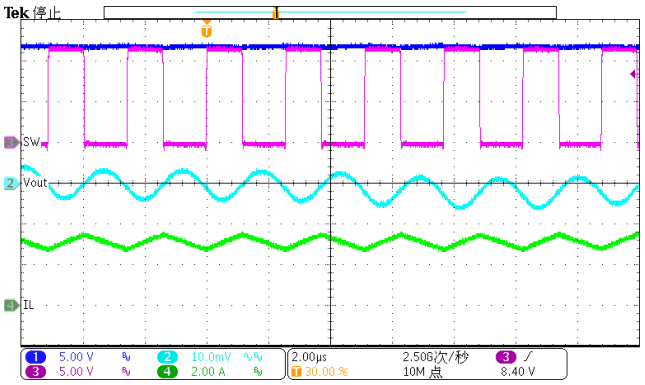


Figure 20. Output Ripple (I_{LOAD}=3A)

Figure 21. Thermal, 12V_{IN}, 5V_{OUT}, 3A

Layout Guideline

Proper PCB layout is a critical for SCT2330D's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure the top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. It is recommended 10mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling. Do not drill vias in the path of SW.
6. The FB terminal is sensitive to noise so the FB resistor should be located as close as possible to the IC and routed with minimal lengths of trace. Do not drill vias in the path of FB.
7. UVLO adjust, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

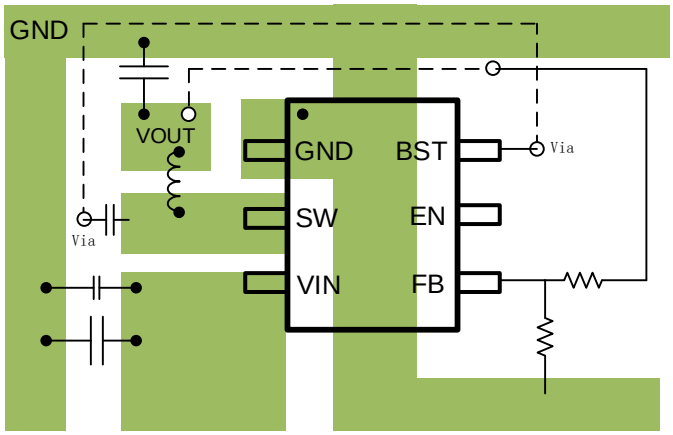
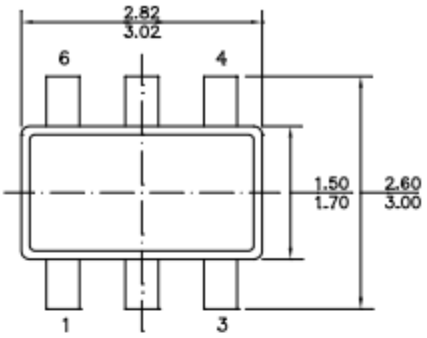
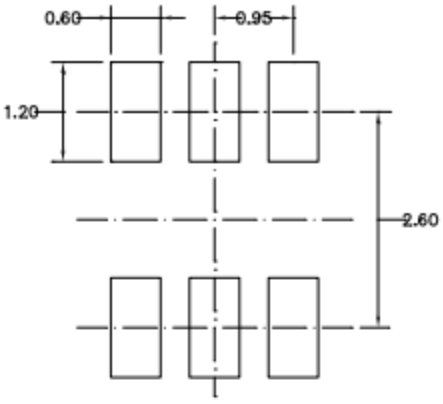


Figure 22. PCB Layout Example

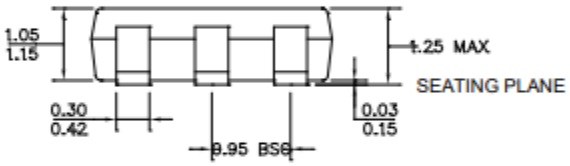
PACKAGE INFORMATION



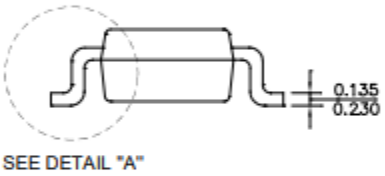
TOP VIEW



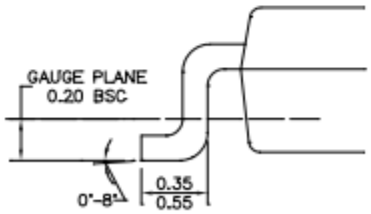
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

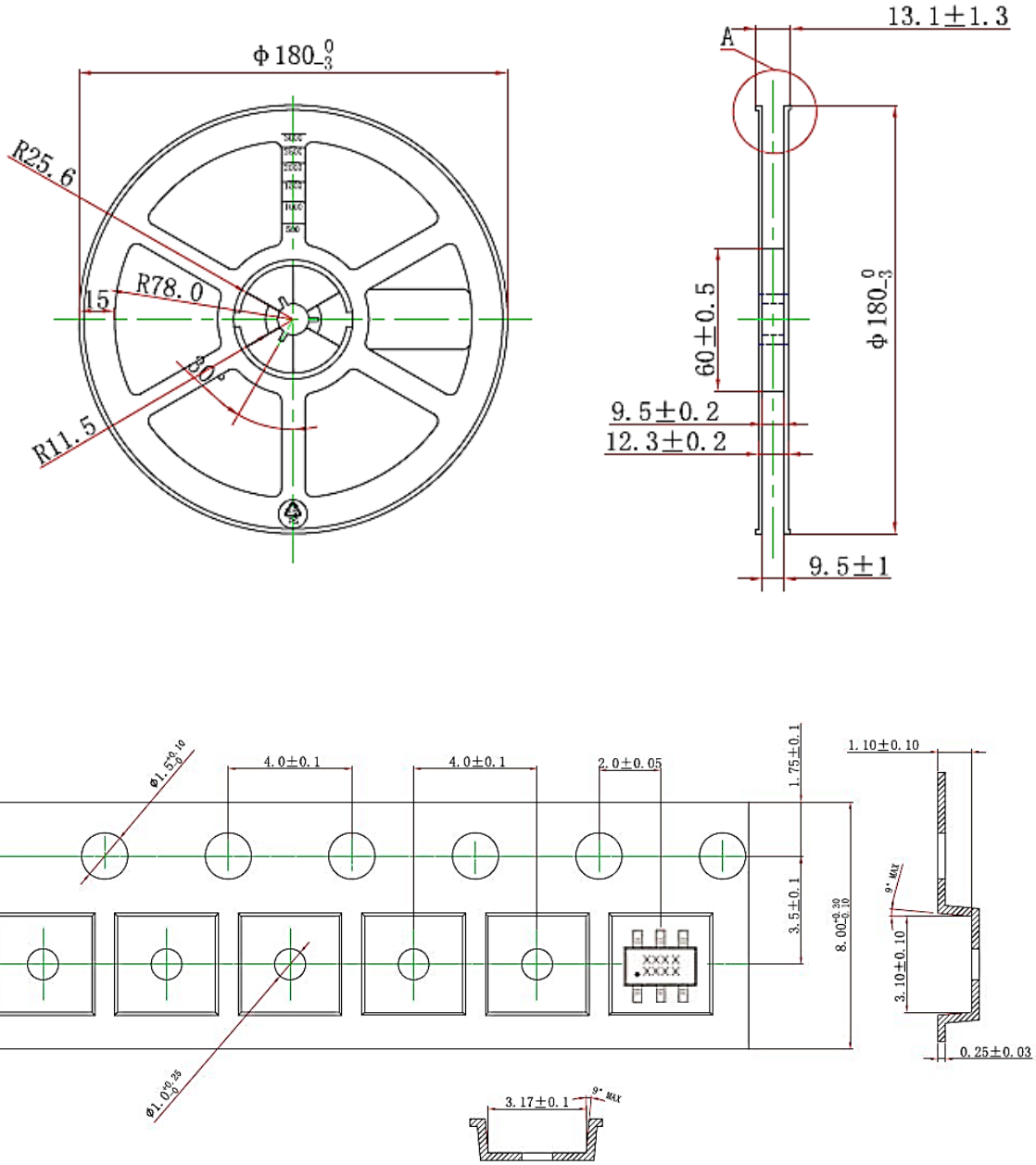


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

TAPE AND REEL INFORMATION



Feeding Direction

