3.5V-36V Vin, 6A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Range: 3.5V-36V
- Up to 6A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 30mΩ High-Side and 18mΩ Low-Side Power MOSFETs
- 13uA Quiescent Current with VBIAS Connected to an auxiliary power supply to 5V
- 60ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Frequency 200KHz to 2.1MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- External bias option for improved efficiency
- Parallel input path to minimize switch node ringing
- Low Dropout Mode Operation
- Over-voltage and Over-Temperature Protection
- Available in 4mm*4mm FCQFN-14L Package

APPLICATIONS

- Automotive infotainment and ADAS
- USB Type-C Power Delivery, USB Charging
- Industrial and Medical Distributed Power Supplies

DESCRIPTION

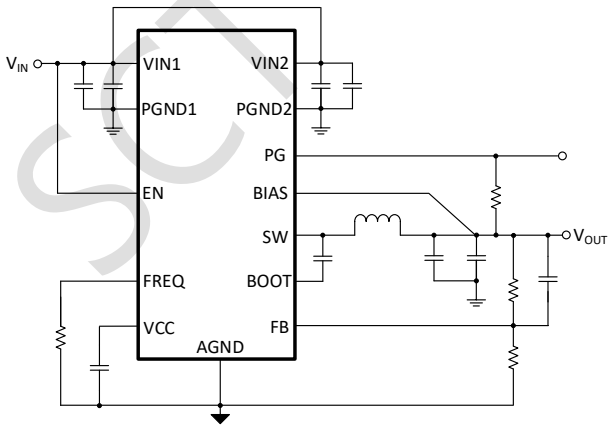
The SCT2461Q is 6A synchronous buck converters with wide input voltage, ranging from 3.5V to 36V, which integrates a 30mΩ high-side MOSFET and a 18mΩ low-side MOSFET. The SCT2461Q, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 13uA (VBIAS=5V) low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2461Q features adjustable switching frequency from 200 kHz to 2.1MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 200kHz to 2.1MHz. The SCT2461Q allows power conversion from high input voltage to low output voltage with a minimum 60ns on-time of high-side MOSFET.

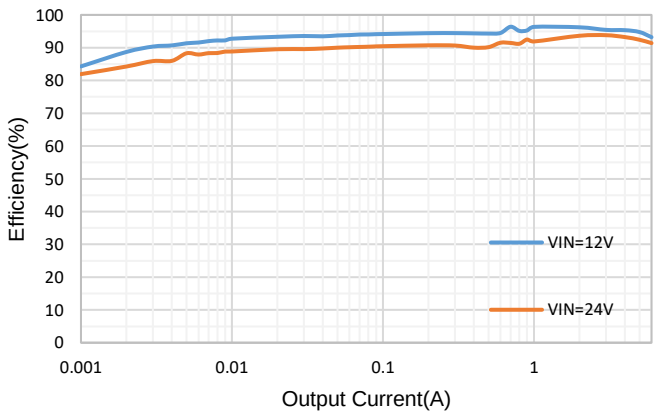
The SCT2461Q is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2461Q features Frequency Spread Spectrum FSS with ±6% jittering span of switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT2461Q offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in 4mm*4mm FCQFN-14L package.

TYPICAL APPLICATION



3.5V-36V, Syncronous Buck Converter



Efficiency, V_{OUT}=5V, Fsw=400KHz

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.8: Customer Samples.

Revision 0.81: Update THERMAL INFORMATION.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2461QFNFR	Tape & Reel	5000	2461Q	14	FCQFN4x4-14L	TBD

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN1, VIN2 (2)	-0.3	42	V
EN	-0.3	42	V
BOOT	-0.3	48	V
SW	-0.3	42	V
SW (<10ns) (3)	-3	42	V
BOOT-SW	-0.3	6	V
BIAS, PG	-0.3	24	V
VCC, FB, FREQ	-0.3	6	V
Operating junction temperature TJ (4)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

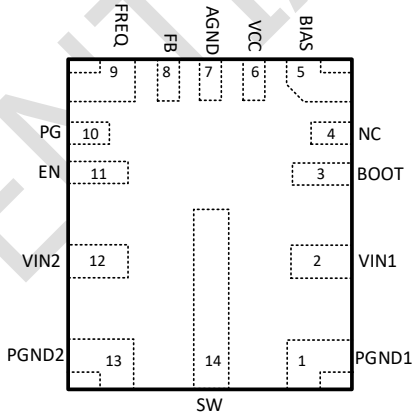


Figure1. 14-Lead FCQFN 4mm×4mm (Sketch Map)

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
PGND1	1	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
VIN1	2	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
BOOT	3	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on, or SW voltage is low.
NC	4	Not connected.
BIAS	5	Input to internal LDO. Connect to output voltage point to improve efficiency. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity. If output voltage is above 20 V, connect this pin to ground.

VCC	6	Internal LDO output. Used as supply to internal control circuits. Decouple with 1μF ceramic capacitor placed as close to VCC as possible.
AGND	7	Analog ground.
FB	8	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
FREQ	9	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to this pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor adjusted frequency.
PG	10	Power good open-drain output. PGOOD is high if the output voltage is higher than 95% and lower than 105% of the nominal voltage.
EN	11	Enable pin to the regulator with internal pull-up current source. Pull below 0.9V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN2	12	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
PGND2	13	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
SW	14	Regulator switching output. Connect SW to an external power inductor

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT}	Output voltage range	1	16	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM)	-1.5	+1.5	kV
	Charged Device Model (CDM)	-1	+1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCQFN-14L	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	44.57	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	2.73	
Ψ_{JB} (2)	Junction-to-board characterization parameter	4.82	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	35.52	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	4.93	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	31.08	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	1.72	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2461Q is mounted and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT2461Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual RθJA and RθJC.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
(3) Measured on SCT standard EVM: SCT2461Q Demo Board, Outer layer 1oz and inner layer 0.5oz copper thickness, 75mm x 65mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_A=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.5		36	V
I_{SHDN}	Shutdown current from VIN pin	EN=0		1.8		μA
I_{Q_BIAS}	Quiescent current from VIN pin	EN floating, non-switching, VBIAS=5V, BOOT-SW=5V		13		μA
I_Q	Quiescent current from VIN pin	EN floating, non-switching, BOOT-SW=5V		45	63	μA
I_{BIAS}	Quiescent Current into BIAS pin	non-switching, VBIAS=5V		25		uA
I_{Active_EVM}*	Active current from VIN pin	VIN=12V, VOUT=5V, no-load		110		uA
$I_{Active\_BIAS\_EVM}$*	Active current from VIN pin	VIN=12V, VOUT=5V, no-load, VBIAS=VOUT		75		uA
VCC LDO						
V_{CC}	V_{CC} voltage			4.2		V
V_{CC_UVLO}	V_{CC} UVLO Threshold	V_{CC} rising		3.3	3.5	V
	Hysteresis			400		mV
I_{VCC_LIM}	V_{CC} internal LDO current limit	VCC short to ground			60	mA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=4.2V		30	43	mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			18	28	mΩ
Reference						
V_{REF}	Reference voltage of FB	T_J=25℃	0.792	0.8	0.808	V
		T_J=-40~125℃	0.784		0.816	V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold	T_J=25℃	7.7	8.5	9.5	A
		T_J=-40~125℃	7.2		10	
I_{LIM_LSSRC}	Low-side power MOSFET souring current limit threshold	T_J=25℃	7.1	8	9.1	A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.07	1.13	V
V_{EN_L}	Enable low threshold		0.76	0.9		V
I_{EN}	Enable pin pull-up current			250		nA
t_{ss}	Internal soft start time			4		ms
Switching Frequency and External Clock Synchronization						
F_{RANGE_RT}	Frequency range using RT mode		200		2100	kHz
F_{SW}	Switching frequency	R_{FREQ}=53.2kΩ	360	400	440	kHz
F_{RANGE_CLK}	Frequency range using CLK mode		200		2100	kHz
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%
t_{ON_MIN}*	Minimum on-time	V_{IN}=36V		60		ns

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Good						
V_{PG_UV}	Power-good flag under voltage tripping threshold	POWER GOOD (% of FB voltage)		96		%
		POWER BAD (% of FB voltage)		94		%
V_{PG_OV}	Power-good flag over voltage tripping threshold	POWER BAD (% of FB voltage)		110		%
		POWER GOOD (% of FB voltage)		105		%
I_{PG}	PWRGD leakage current at high level output	VPull-Up = 5V			200	nA
V_{PG_LOW}	PWRGD low level output voltage	IPull-Up = 1 mA		0.05		V
$t_{PGDFLT(rise)}$	Delay time to PGOOD high signal			2		ms
$t_{PGDFLT(fall)}$	Glitch filter time constant for PGOOD function			100		us
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising		110		%
		V_{FB}/V_{REF} falling		105		%
V_{BOOTUV}	BOOT-SW UVLO Threshold	BOOT-SW falling		2.35		V
		Hysteresis		250		mV
T_{SD}*	Thermal shutdown threshold	T_J rising		172		°C
		Hysteresis		12		°C

*Derived from bench characterization or design values.

TYPICAL CHARACTERISTICS

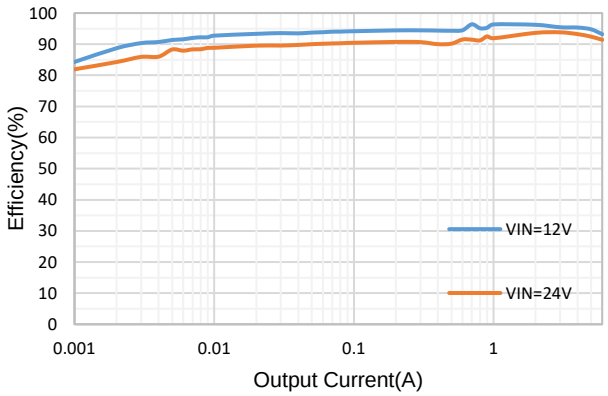


Figure 2. Efficiency, F_{SW}=400KHz, V_{OUT}=5V (BIAS)

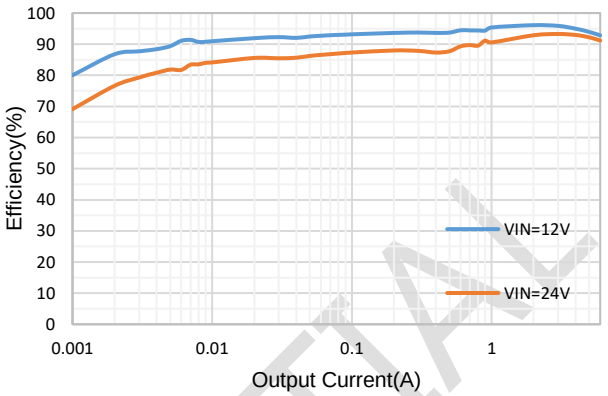


Figure 3. Efficiency, F_{SW}=400KHz, V_{OUT}=5V (NO BIAS)

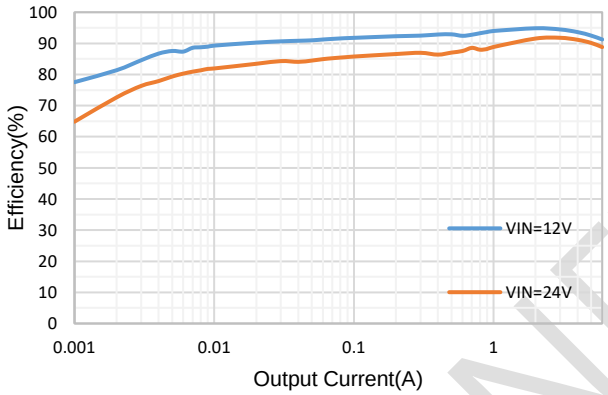


Figure 4. Efficiency, F_{SW}=400KHz, V_{OUT}=3.3V

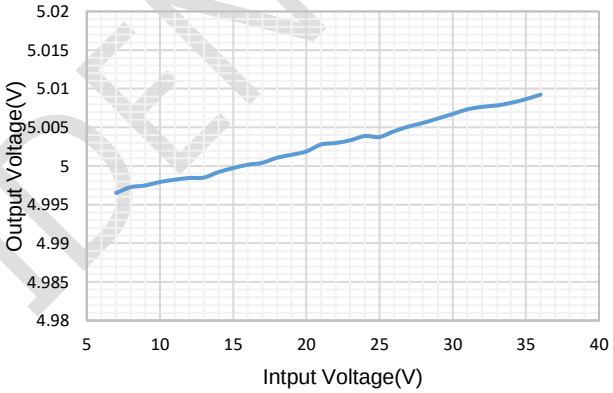


Figure 5. Line Regulation, I_{OUT}=3A

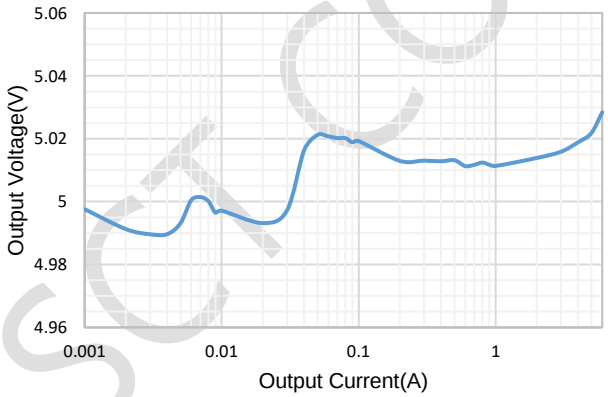


Figure 6. Load Regulation, V_{IN}=5V

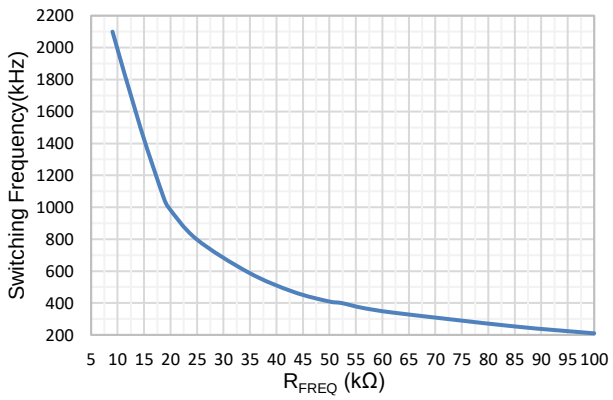


Figure 7. Clock Frequency vs FREQ Resistor

FUNCTIONAL BLOCK DIAGRAM

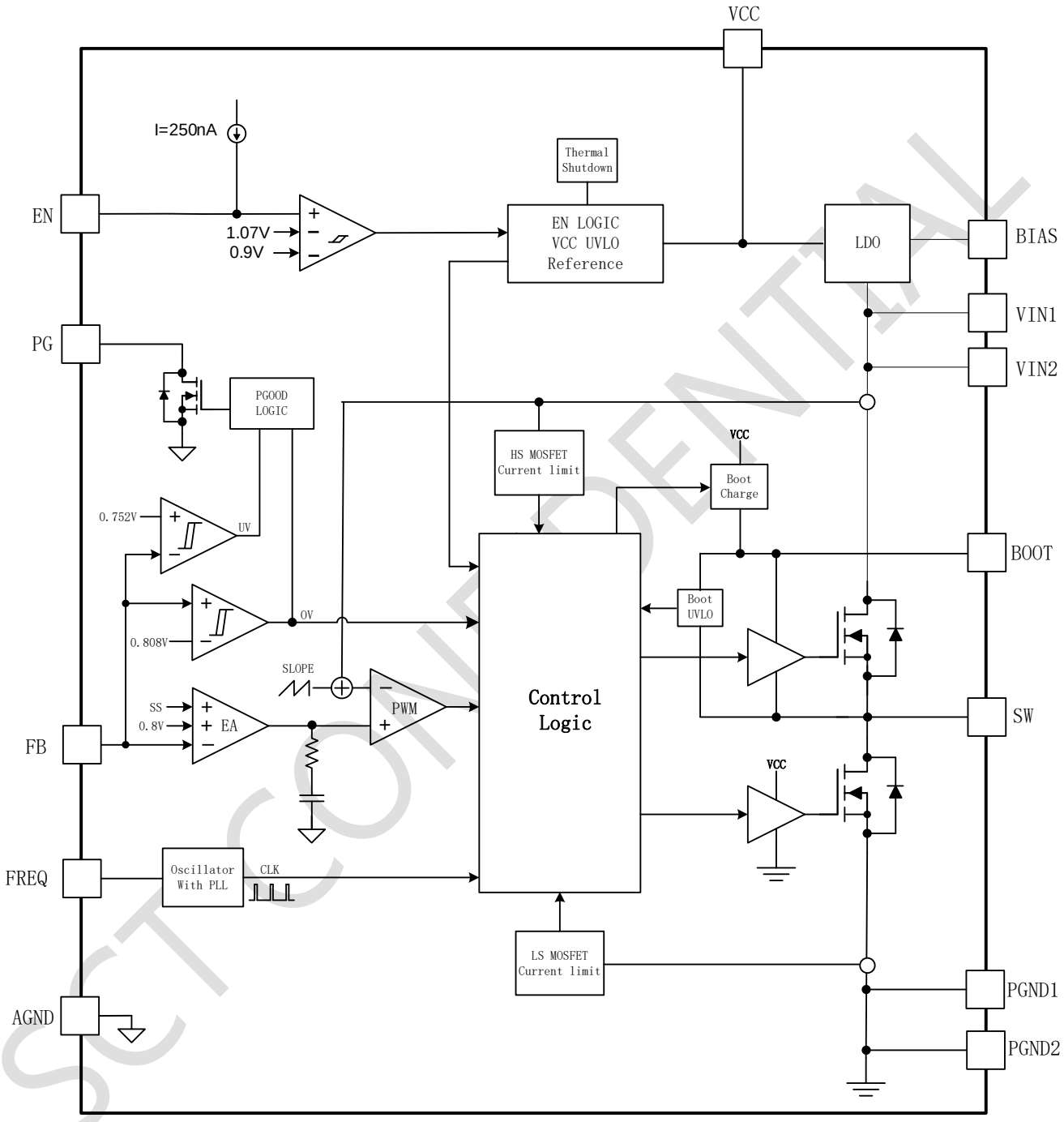


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2461Q is a 3.5V-36V input, 6A output, EMI friendly synchronous buck converter with built-in 30mΩ Rdson high-side and 18mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 2.1MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The SCT2461Q features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 13uA (VBIAS=5V) under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2461Q implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time.

The SCT2461Q full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2461Q employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The SCT2461Q operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (415mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 1.2A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 13uA (VBIAS=5V) during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2461Q is enabled when the VCC pin voltage rises above 3.3V and the EN pin voltage exceeds the enable threshold of 1.07V. The device is disabled when the VCC pin voltage falls below 2.9V or when the EN pin voltage is below 0.9V. An internal 250nA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = (\frac{R1}{R2} + 1) \times V_{ENR} \quad (1)$$

$$V_{fall} = (\frac{R1}{R2} + 1) \times V_{ENF} \quad (2)$$

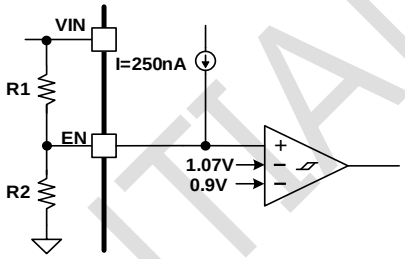


Figure 9. System UVLO by enable divide

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- V_{ENR}=1.07V, V_{ENF}=0.9V

Output Voltage

The SCT2461Q regulates the internal reference voltage at 0.8V with ±2% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2461Q integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 0.9V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2461Q is set by placing a resistor between FREQ pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between FREQ pin to the ground sets the switching frequency over a wide range from 200KHz to 2.1MHz. The FREQ pin voltage is typical 0.3V. FREQ pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 7 to determine the resistance for a switching frequency needed.

$$R_{FREQ}(K\Omega) = \left(\frac{1}{f_{SW}(KHz)} - 3.3 \times 10^{-5}\right) \times 2.04 \times 10^{4} \quad (4)$$

Where, fsw is switching clock frequency.

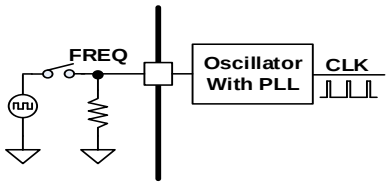


Figure 10. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to FREQ pin. The synchronization frequency range is from 200KHz to 2.1MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at FREQ pin with typical 66ns time delay. A square wave clock signal to FREQ pin must have high level no lower than 3V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 10. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the SCT2461Q implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the adjusted switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency adjusted by resistor placed at FREQ pin and an external clock synchronization application.

VCC LDO, VCC UVLO, and BIAS Input

The VCC pin is the output of the internal LDO used to supply the control circuits of the SCT2461Q and the typical output voltage is 4.2V. The BIAS pin is the input of the internal LDO. This input can be connected to V_{OUT} to save the power loss from V_{IN}. If the BIAS voltage is larger than 4.8V, LDO is powered by BIAS pin. If the BIAS voltage is less than 4.6 V, VIN1 and VIN2 directly powers the internal LDO. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low.

Bootstrap Voltage Regulator and Low Drop-out Operation

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.6V and hysteresis of 250mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, the duty cycle is large and reaches the minimum-off time(200nS), SCT2461Q operates in Low Drop-Out LDO mode. The switching frequency starts to decrease, and the minimum decreases to 80kHZ. To ensure that the output voltage can better follow the change of input voltage.

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value.

Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2461Q LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

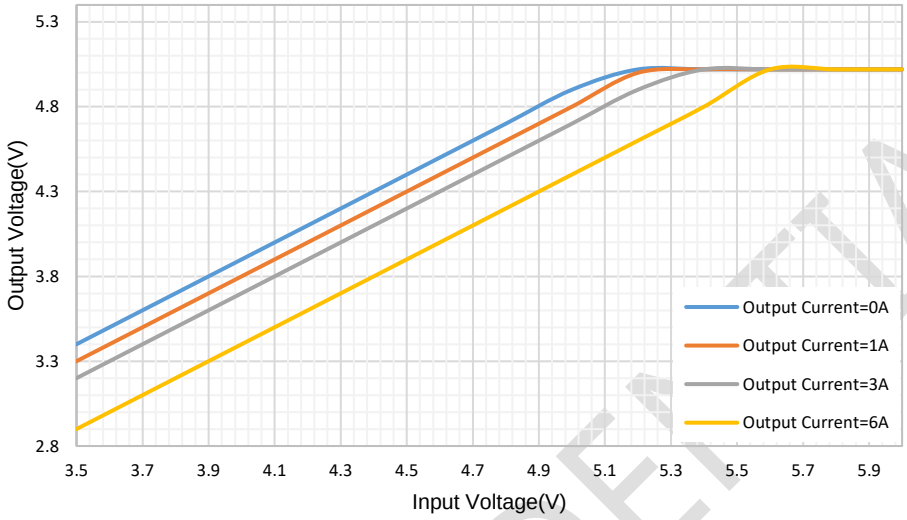


Figure 11. LDO Operation Characteristic (Vout =5V)

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2461Q implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage 1.7V typical. When COMP voltage is clamped for 16 cycles of low side OC, the converter stops switching. After remaining OFF for 33.6ms，the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high ，after soft start time and COMP still keep high for 16 cycles of low side OC，the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2461Q implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Power Good

The PGOOD pin is an open-drain output. A pull up resistor between the values of 10KΩ and 100KΩ to a voltage source that is 5V or less is recommended.

Once the FB pin is between 96% and 105% of the internal voltage reference the PGOOD pin is de-asserted and the pin floats with 2ms delay. The PGOOD pin is pulled low when the FB is lower than 94% or greater than 110% of the nominal internal reference voltage with 100us deglitching time, PG_OVP only work in the close-loop state. Also, the PG is pulled low if VIN UVLO or thermal shutdown are asserted or the EN pin pulled low, Output voltage excursions that are shorter than 100us deglitching time do not trip the PGOOD flag.

Thermal Shutdown

The SCT2461Q protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 172°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 160°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

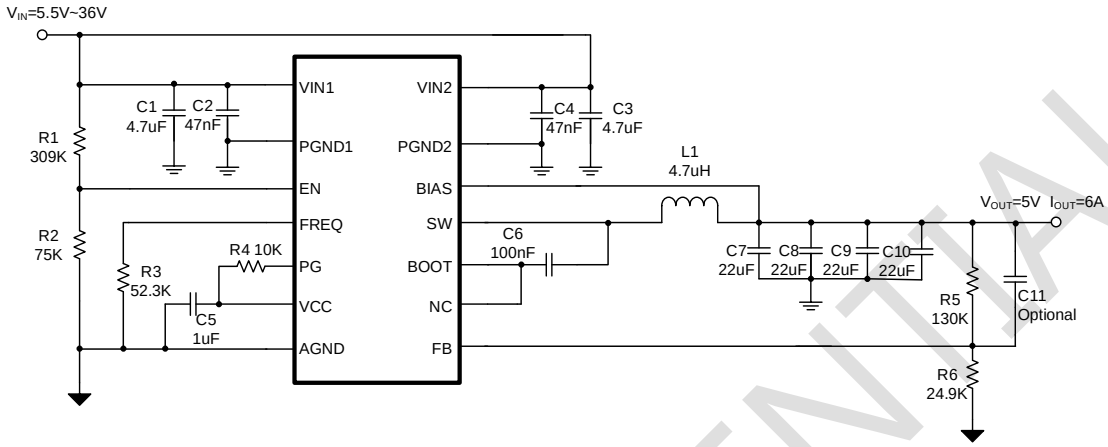


Figure 12. SCT2461Q Design Example, 5V Output with Adjustable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 3.5V to 36V
Output Voltage	5V
Maximum Output Current	6A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	6.2mV
Start Input Voltage (rising VIN)	5.5V
Stop Input Voltage (falling VIN)	4.6V

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 24.9KΩ. Use Equation 5 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V.

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
3.3 V	76.8 KΩ	24.9 KΩ
5 V	130 KΩ	24.9 KΩ
12 V	348 KΩ	24.9 KΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The 60ns minimum on-time limitation also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 400 kHz is selected to achieve both small solution size and high efficiency operation.

The resistor connected from FREQ to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using Equation 6 or determined from Figure 7.

$$R_3(\mathrm{K\Omega}) = \left(\frac{1}{fsw(KHz)} - 3.3 \times 10^{-5}\right) \times 2.04 \times 10^4 \quad (6)$$

where:

- f_{SW} is the desired switching frequency

Table 2. R_{FSW} Value for Common Switching Frequencies (Room Temperature)

Fsw	R_3 (R_{FSW})
210 KHz	100 KΩ
400 KHz	52.3 KΩ
590 KHz	34.8 KΩ
1000 KHz	19.6 KΩ
1500 KHz	14.3 KΩ
2100 KHz	9.09 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 5.5V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 4.6V (stop or disable). Use Equation 7 and Equation 8 to calculate the values 309 kΩ and 75 kΩ of R1 and R2 resistors.

$$V_{rise} = \left(\frac{R1}{R2} + 1\right) \times V_{ENR} \quad (7)$$

$$V_{fall} = \left(\frac{R1}{R2} + 1\right) \times V_{ENF} \quad (8)$$

where:

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

- V_{ENR}=1.07V, V_{ENF}=0.9V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

$$I_{LPP} = \frac{V_{OUT}*(V_{IN}-V_{OUT})}{V_{IN}*L*f_{SW}} \quad (9)$$

Where:

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 10 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW}*LIR*I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (10)$$

Where:

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 11 and Equation 12.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (11)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (12)$$

Where:

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 8.5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 8.5A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the

SCT2461Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst-case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, two 4.7μF, X7R ceramic capacitors rated for 50 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where:

- $\Delta V_{OUT}$is the output voltage ripple

- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 22μF ceramic output capacitors work for most applications.

Table 3: Typical External Component Values

VOUT	R5	R6	FREQUENCY	R_3	L1	COUT
3.3V	76.8 KΩ	24.9 KΩ	400KHz	52.3 KΩ	3.3uH	4*22uF
5V	130 KΩ	24.9 KΩ	400KHz	52.3 KΩ	4.7uH	4*22uF
12V	348 KΩ	24.9 KΩ	400KHz	52.3 KΩ	10uH	6*22uF

Application Waveforms

Vin=24V, Vout=5V, unless otherwise noted

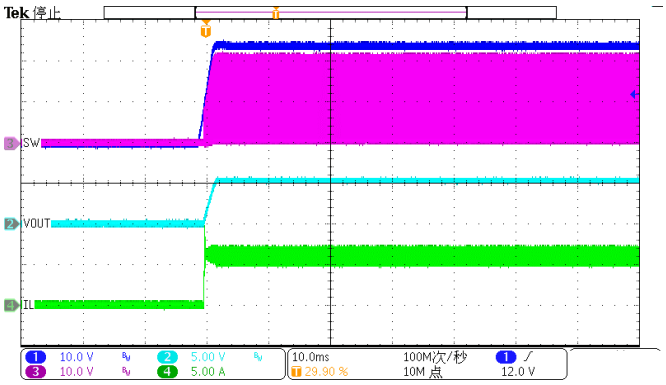


Figure 13. Power up (Iload=6A)

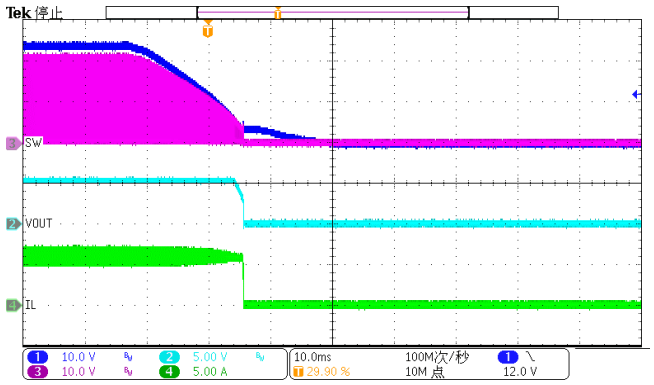


Figure 14. Power down (Iload=6A)

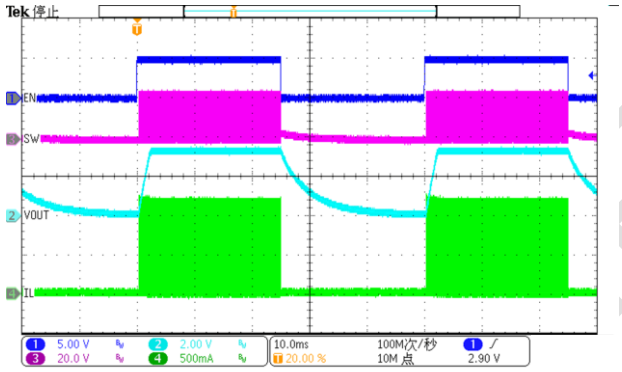


Figure 15. EN toggle (Iload=0.1A)

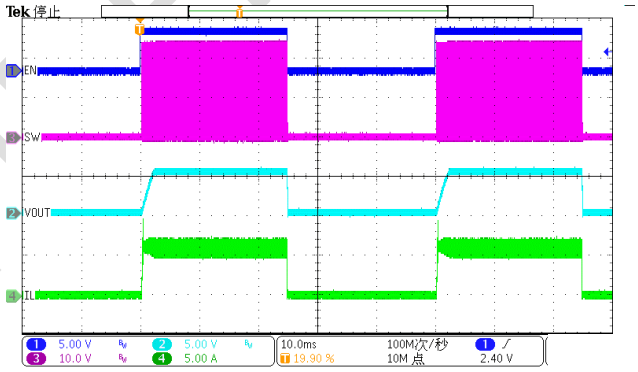


Figure 16. EN toggle (Iload=6A)

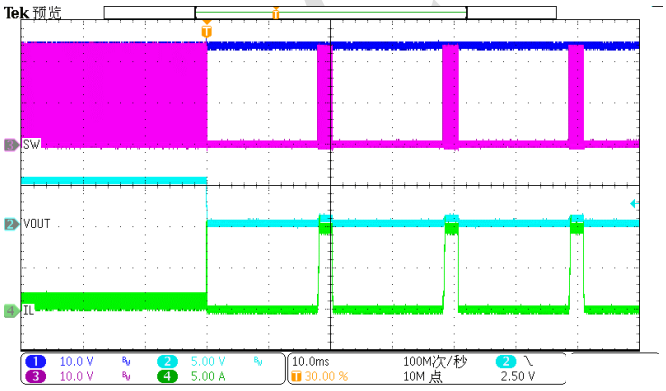


Figure 17. Over Current Protection (1A to hard short)

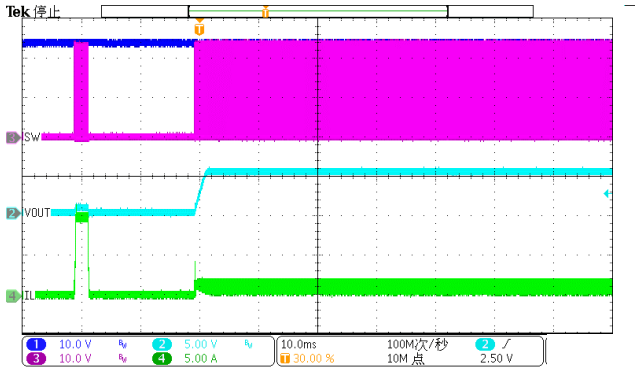


Figure 18. Over Current Release (hard short to 1A)

Application Waveforms

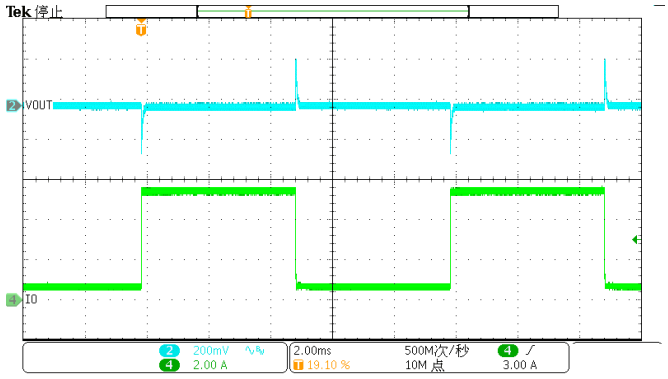


Figure 19. Load Transient (0.6A-5.4A, 1.6A/us)

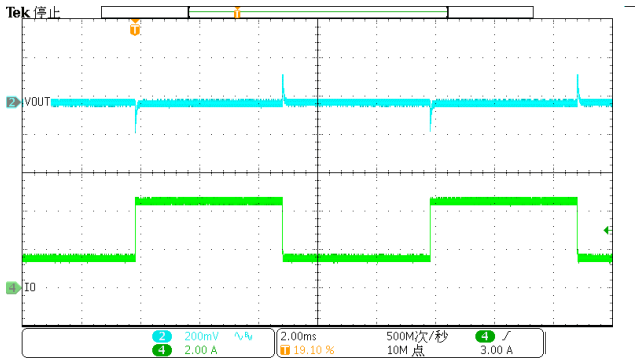


Figure 20. Load Transient (1.5A-4.5A, 1.6A/us)

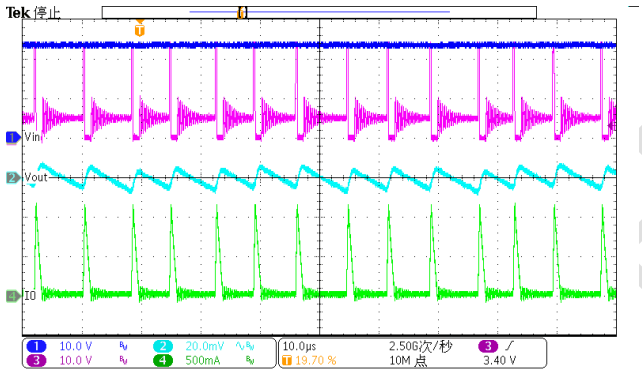


Figure 21. Output Ripple (Iload=100mA)

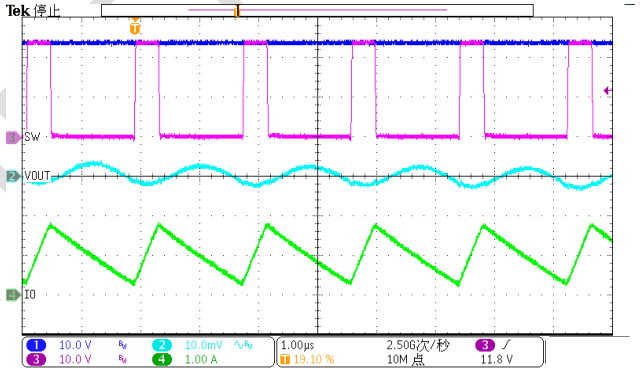


Figure 22. Output Ripple (Iload=1A)

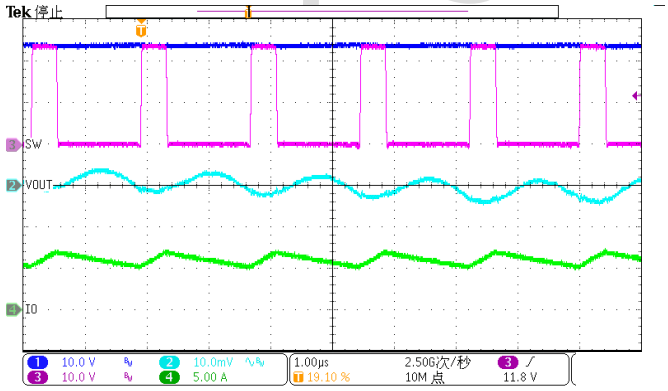


Figure 23. Output Ripple (Iload=6A)

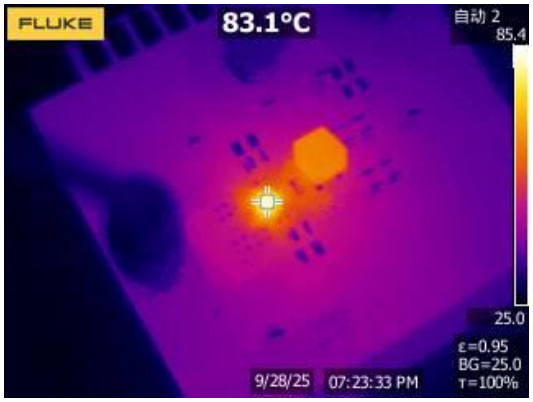


Figure 24. Thermal, 12Vin, 5Vout, 6A

Layout Guideline

Proper PCB layout is a critical for SCT2461Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and PGND as possible to reduce parasitic effect.
3. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
4. The FREQ terminal is sensitive to noise so the FREQ resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
5. UVLO adjust and FREQ resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
6. For achieving better thermal performance, a four-layer layout is strongly recommended.

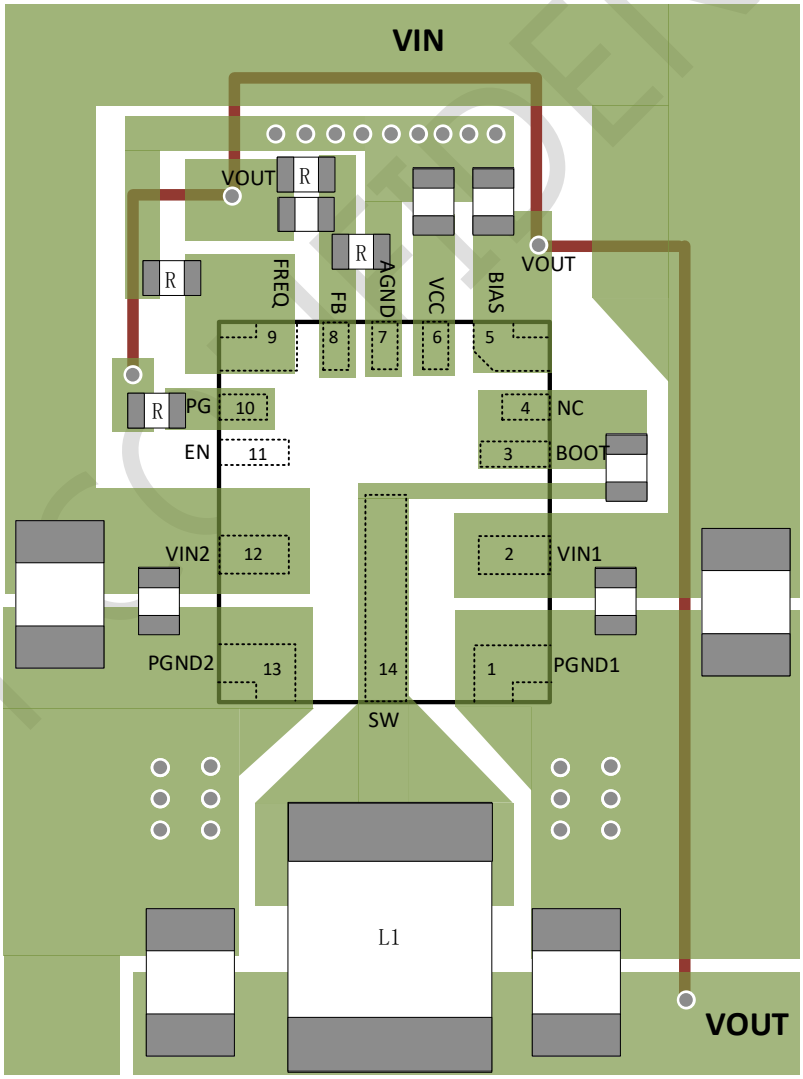
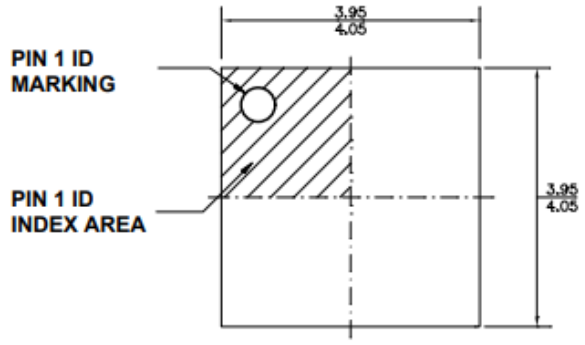
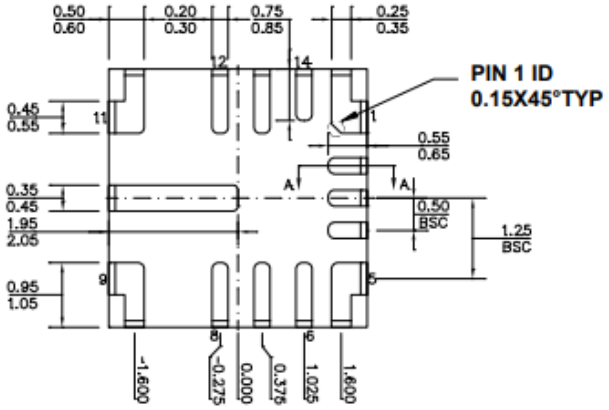


Figure 25. PCB Layout Example (Sketch Map)

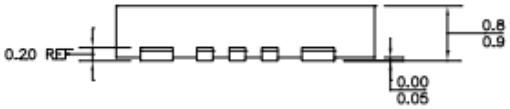
PACKAGE INFORMATION



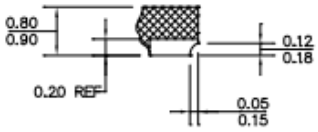
TOP VIEW



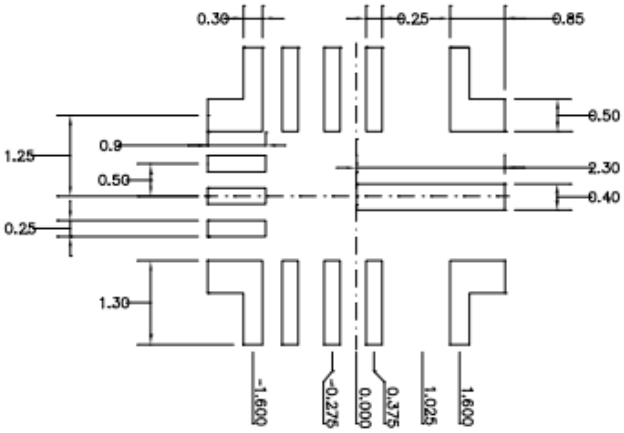
BOTTOM VIEW



SIDE VIEW



SECTION A-A

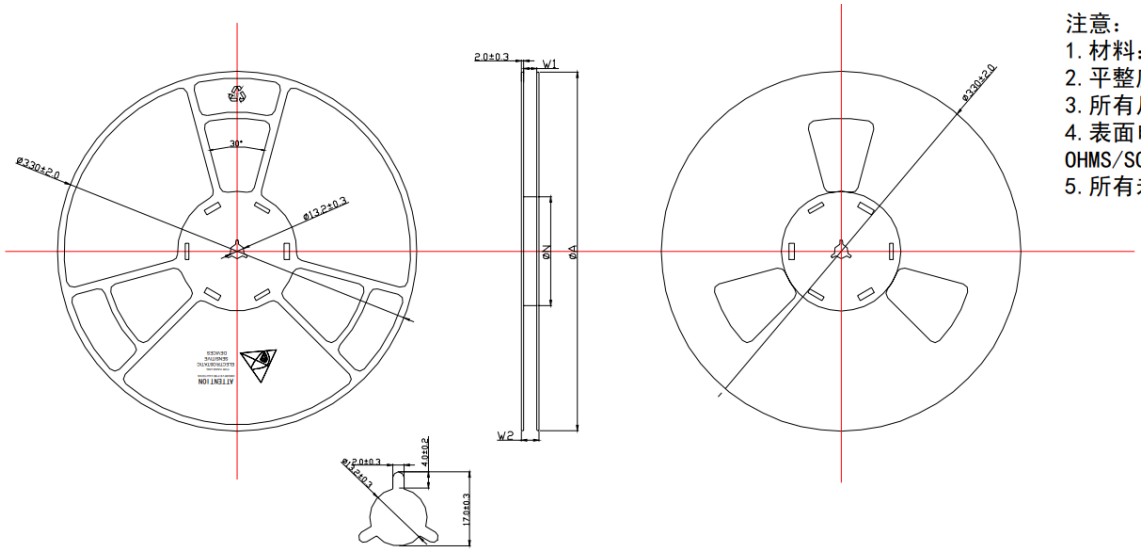


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.

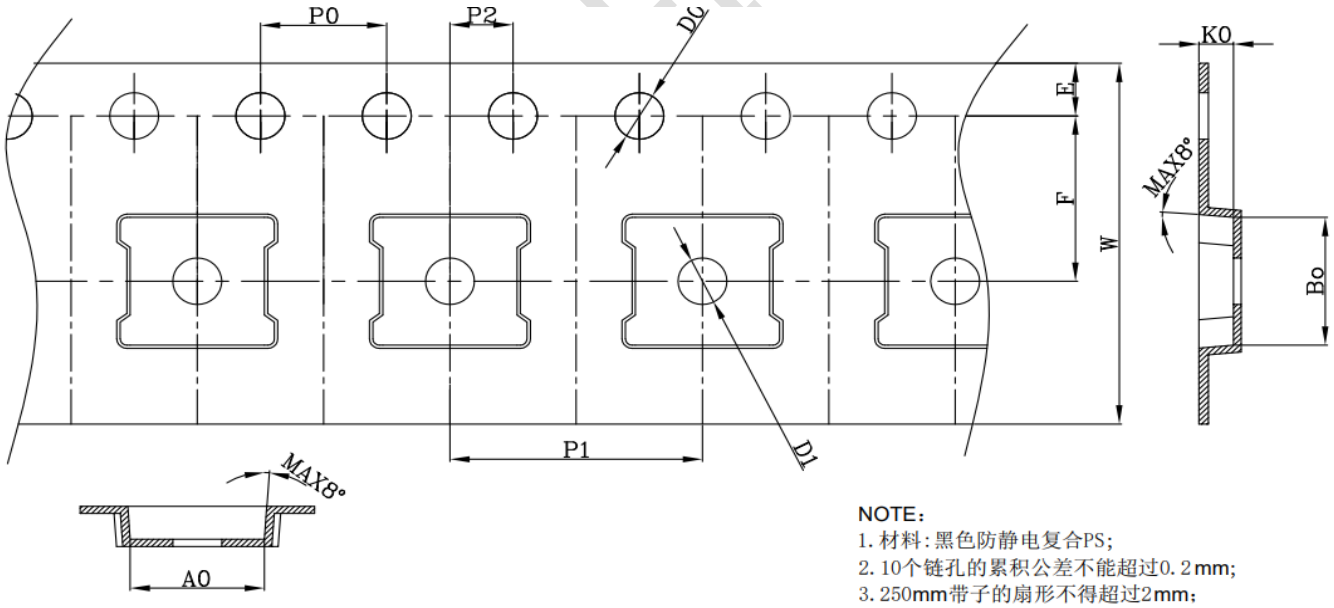
TAPE AND REEL INFORMATION



注意：
1. 材料：聚苯乙烯；
2. 平整度：最大允许3毫米；
3. 所有尺寸为毫米；
4. 表面电阻：10E5~10E11 OHMS/SQ以下
5. 所有未标注公差：±0.5

PRODUCT SPECIFICATIONS				
TYPE WIDTH	∅A	∅N	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	4.30±0.10	4.30±0.10	1.10±0.10	4.00±0.10	8.00±0.10	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.30±0.05	1.75±0.10	5.50±0.05	1.55±0.05	1.55±0.10	12.00±0.30



NOTE：
1. 材料：黑色防静电复合PS；
2. 10个链孔的累积公差不能超过0.2mm；
3. 250mm带子的扇形不得超过2mm；
4. 所有尺寸符合EIA-481-E的要求。