3.8V-30V Vin, 3A, High Efficiency Synchronous Step-down DCDC Converter

FEATURES

- Wide Input Range: 3.8V-30V
- Up to 3A Continuous Output Current
- 0.8V Feedback Reference Voltage
- Integrated 90mΩ High-Side MOSFET and 36mΩ Low-Side MOSFET
- Ultra Low Quiescent Current: 10uA
- Shutdown Current: 1uA
- Peak current mode control
- Pulse Skipping Mode (PSM) in light load
- 80ns Minimum On-time
- Programmable Soft-start Time
- Random Spread Spectrum option for reduced EMI
- Adjustable Frequency: 200kHz~2.2MHz
- Support start-up with pre-biased output
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout and Minimum On Time Function
- Hiccup Mode for Over current Protection
- Over-voltage and Over-Temperature Protection
- Available in an FCSOT583 Package

APPLICATIONS

- Building automation, appliances, industrial PC
- Multifunction printers, enterprise projectors
- Portable electronics, connected peripherals
- Smart speakers, monitors
- Distributed power systems with 5V, 12V, 19V, and 24V input

DESCRIPTION

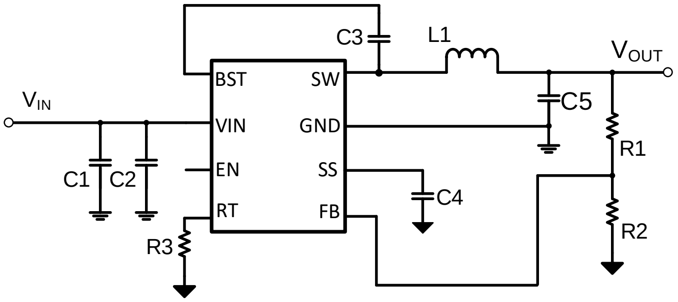
The SCT2333 is a 3A synchronous buck converter with wide input voltage, ranging from 3.8V to 30V, which integrates a 90mΩ high-side MOSFET and a 36mΩ low-side MOSFET. The SCT2333, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load or standby condition.

The switching frequency can be programmed from 200kHz to 2.2MHz through external resistors to optimizes either the power efficiency or the external components' sizes. The SCT2333 allows power conversion from high input voltage to low output voltage with a minimum 80ns on-time of high-side MOSFET. The SCT2333 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2333 features Random Spread Spectrum ±6% jittering span of switching frequency to reduce the conducted EMI.

The device offers programmable soft start to prevent inrush current during the startup of output voltage ramping. The SCT2333 supports monotonic start with pre-biased output. The SCT2333 features internal loop compensation, which can provide stable output voltage and fast loop response, while reducing off chip configuration.

The SCT2333 provides cycle-by-cycle current limit, hiccup mode for over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an FCSOT583 package.

TYPICAL APPLICATION



3.8V-30V, Synchronous Buck Converter
Simplified schematic diagram

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2333TTAR	Tape & Reel	5000	2333	8	FCSOT583	1

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted (1)

DESCRIPTION	MIN	MAX	UNIT
VIN (2)	-0.3	32	V
BOOT	-0.3	38	V
SW	-0.3	32	V
SW (<20ns) (3)	-3	33	V
BOOT-SW	-0.3	6	V
EN, FB, RT, SS	-0.3	6	V
Operating junction temperature TJ (4)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

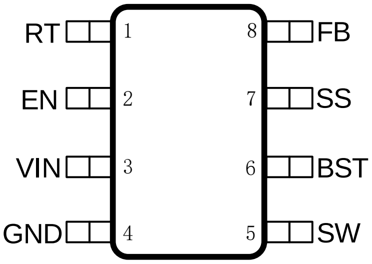


Figure 1. 8-Lead FCSOT583

---

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The max VIN transient voltage is guaranteed by design and verified on bench.
(3) This applies to the ringing voltage generated by itself, not externally applied voltage.
(4) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous function above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
RT	1	Set the internal oscillator clock frequency. Float for 500kHz, tie to GND for 1.15MHz, or connect a resistor from this pin to ground to set switching frequency.
EN	2	Enable pin to the regulator with internal pull-up current source. Pull below 1.2V to disable the converter. Float or driven to high level to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
VIN	3	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
GND	4	Ground.
SW	5	Regulator switching output. Connect SW to an external power inductor
BST	6	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when SW voltage is low.
SS	7	Soft start setting pin. Connect an external capacitor to this pin to set the soft start time.
FB	8	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted.

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	30	V
V_{OUT}	Output voltage range	0.8	22	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins (1)	-2.5	2.5	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins (2)	-1	1	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	FCSOT583	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	105.65	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	3.15	
Ψ_{JB} (2)	Junction-to-board characterization parameter	21.36	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	64.66	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	21.75	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	71.12	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	2.69	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2333 is mounted and external environmental factors. The PCB board is a heat sink that is soldered to the leads of the SCT2333. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

(3) Measured on SCT standard EVM: SCT2333 Demo Board, Outer layer 1oz and inner layer 0.5oz copper thickness, 55mm x 40mm, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.8		30	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		3.6	3.8	V
	Hysteresis			300		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1	2.6	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		10	18	μA
$I_{Active\_EVM}^*$	Active current from VIN pin	V_{IN}=24V, EN floating, V_{OUT}=5V, no-load		28		uA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance		75	90	160	mΩ
R_{DSON_L}	Low-side MOSFET on-resistance		25	36	65	mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	Tj=25°C	0.792	0.8	0.808	V
		Tj=-40°C ~125°C	0.784	0.8	0.816	V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		3.2	5	6.5	A
I_{LIM_LS}	Low-side power MOSFET current limit threshold		2.5	3.8	5	A
I_{zc}^*	Zero cross detector threshold			42		mA
V_{Hiccup}	Hiccup trigger threshold voltage on FB pin		0.45	0.52	0.59	V
$t_{HIC\_W}^*$	Over current protection hiccup wait time			256		cycle
$t_{HIC\_R}^*$	Over current protection hiccup restart time			9* SS		ms
Enable and Soft Startup						
V_{EN_H}	Enable high threshold		1	1.3	1.6	V
V_{EN_L}	Enable low threshold		0.9	1.2	1.5	V
I_{EN_L}	Enable pin pull-up current	EN=1V	0.4	0.6	0.85	μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V	1.4	2.1	2.5	uA
I_{SS}	Soft start charging current		3	5.5	8.5	uA
Switching Frequency						
F_{SW_RANGE}	Frequency range using RT mode		200		2200	kHz
F_{SW}	Switching frequency	RT float	400	500	600	kHz
		RT connect to GND	850	1150	1350	kHz
F_{JITTER}^*	Frequency spread spectrum in percentage of Fsw			±6		%
$t_{ON\_MIN}^*$	Minimum on-time			80		ns
$t_{OFF\_MIN}^*$	Minimum off-time			200		ns
$t_{ON\_MAX}^*$	Max on-time			9		us
Protection						

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising	110	115	120	%
		V_{FB}/V_{REF} falling	108	113	118	%
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling	2.3	2.5	2.85	V
T_{SD}*	Thermal shutdown threshold	T_J rising		165		°C
		Hysteresis		30		°C

*Derived from bench characterization or design function.

TYPICAL CHARACTERISTICS

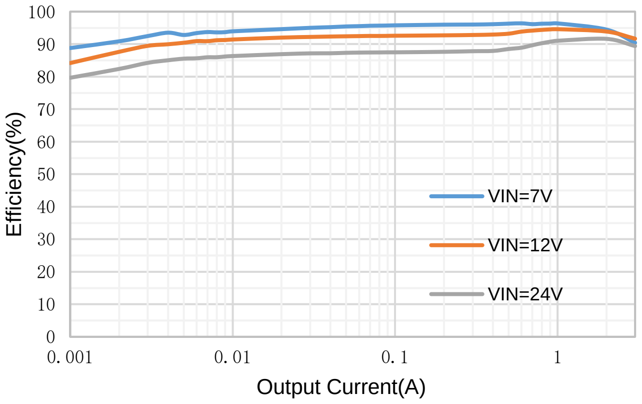


Figure 2. Efficiency, F_{SW}=500kHz, V_{OUT}=5V

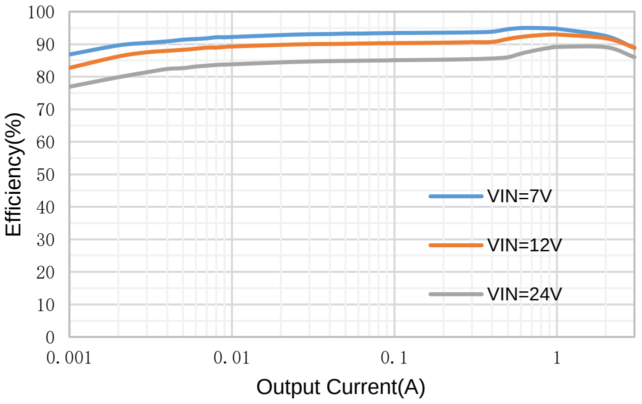


Figure 3. Efficiency, F_{SW}=500kHz, V_{OUT}=3.3V

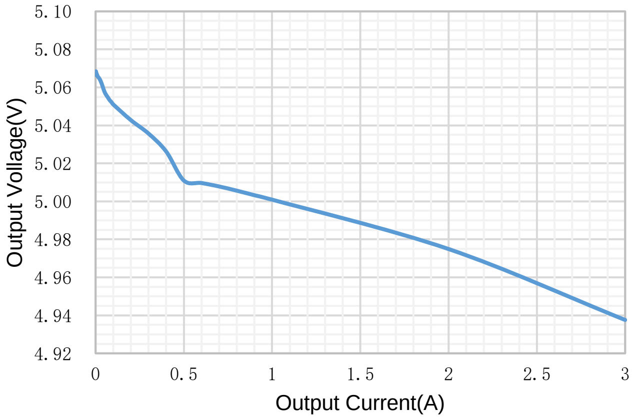


Figure 4. Load Regulation (VIN=12V, VOUT=5V)

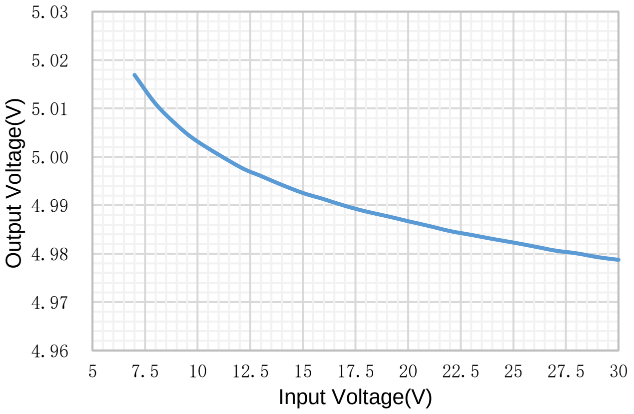


Figure 5. Line Regulation (V_{OUT}=5V, I_{LOAD}=2A)

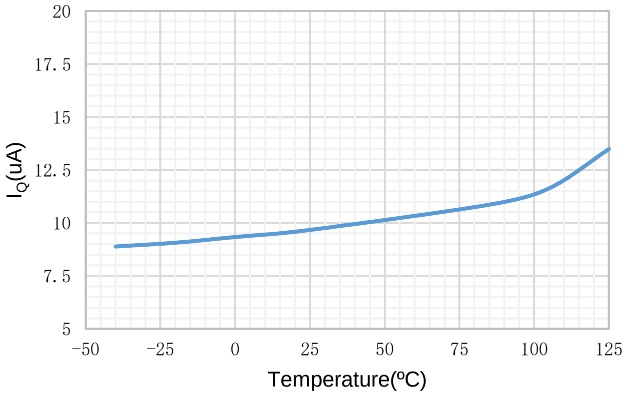


Figure 6. Quiescent current VS Temperature

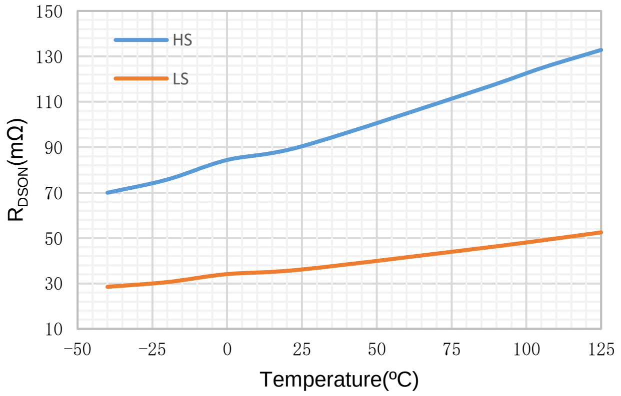


Figure 7. R_{DSON} VS Temperature

FUNCTIONAL BLOCK DIAGRAM

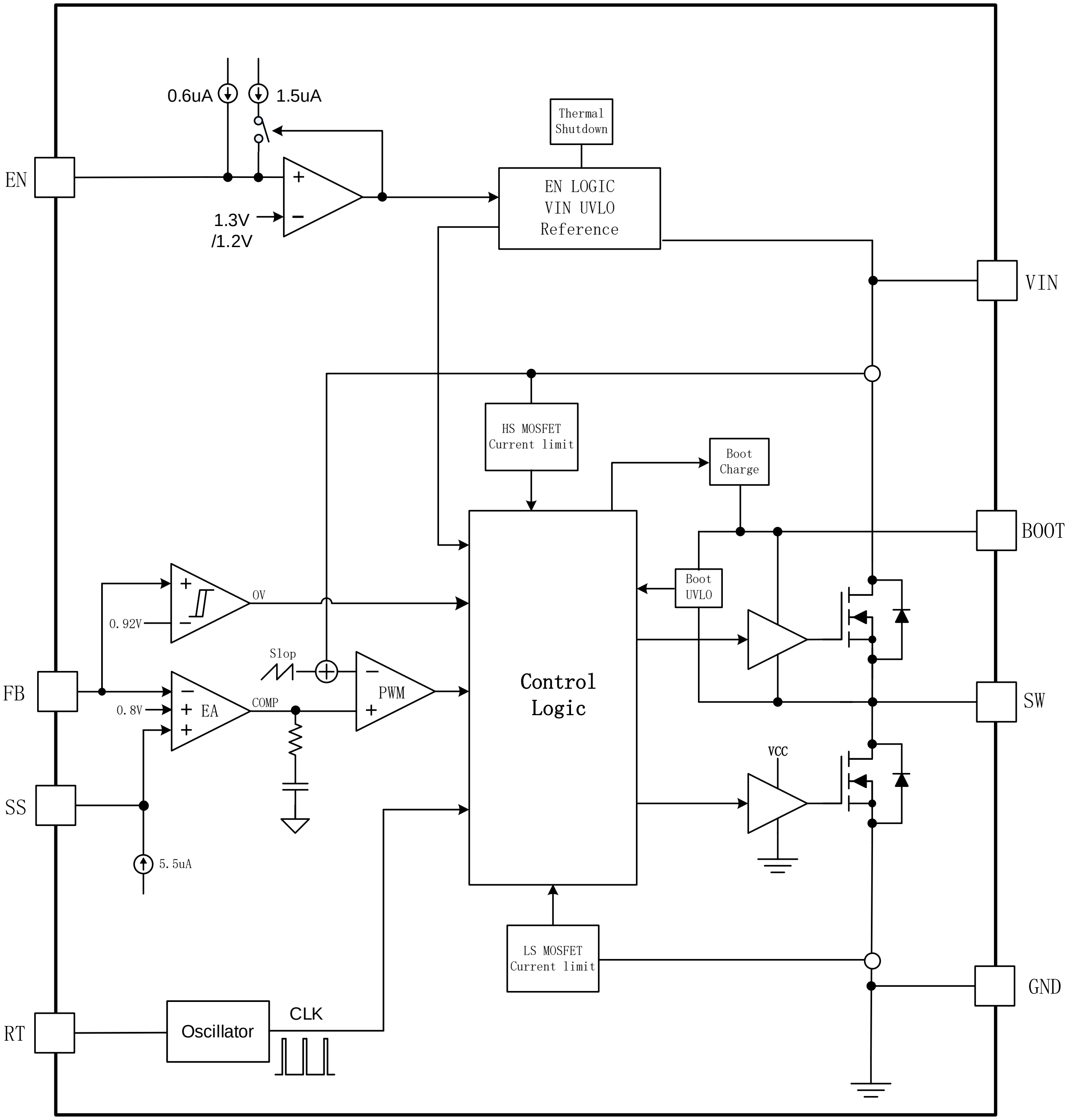


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2333 is a 3.8V-30V input, 3A output, EMI friendly synchronous buck converter with built-in 90mΩ Rdson high-side and 36mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is adjustable from 200kHz to 2.2MHz through resistor to optimize either the power efficiency or the external components' sizes. The SCT2333 features adjustable soft-start to avoid large inrush current. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 10uA under no load or sleep mode condition to achieve high efficiency at light load.

The EN pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements.

SCT2333 achieves ±6% random spread spectrum modulation expansion centered on the set switching frequency. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than apart with fixed frequency operation.

The SCT2333 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The SCT2333 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the high-side MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

Pulse Skipping Mode (PSM) Function

The SCT2333 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold, device enters PSM. The output voltage decays due to output capacitors discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold, then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical I_{peak} inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 10uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The SCT2333 is enabled when the VIN pin voltage rises above 3.6V and the EN pin voltage exceeds the enable threshold of 1.3V. The device is disabled when the VIN pin voltage falls below 3.3V or when the EN pin voltage is below 1.2V. In shutdown mode, the quiescent current drops to 1uA.

An internal 0.6uA pull up current source to EN pin allows the device enable when EN pin floats.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R1 = \frac{V_{rise} * 0.92 - V_{fall}}{1.5uA} \qquad (1)$$

$$R2 = \frac{R_1 \times 1.2}{V_{fall} - 1.2 + R_1 * 2.1uA} \qquad (2)$$

Where:

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

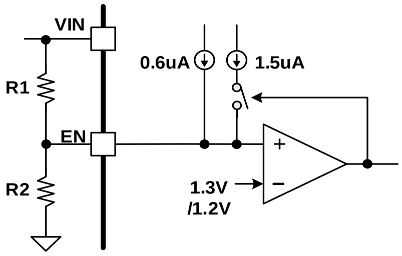


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2333 regulates the internal reference voltage at 0.8V with ±2% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \qquad (3)$$

Where:

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Programmable Soft Start and Soft Start Tracking

The SCT2333 features programmable soft-start time to prevent inrush current during start-up stage. The soft-start time can be programmed easily by connecting a soft-start capacitor C_{ss} from SS pin to ground.

Soft start is triggered by any of the following conditions:

• The device is activated through EN or VIN UVLO.

• Recovery from a hiccup waiting period or shutdown due to overtemperature protection.

The SS pin sources an internal 5.5μA current charging the external soft-start capacitor C_{ss}. The device adopts the lower voltage between the internal voltage reference 0.8V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 0.8V.

The soft-start capacitor value can be calculated going with following Equation 4. Attention should be taken here that the programmed soft-start time should be larger than 1ms.

$$C_{SS} = t_{ss} * \frac{5.5uA}{0.8V} \qquad (4)$$

Where:

- C_{SS} is the soft-start capacitor connected from SS pin to the ground
- t_{ss} is the soft-start time

During soft start, hiccup is disabled. These actions together provide start-up with limited inrush currents and allow the use of larger output capacitors and higher loading conditions that cause current to border on current limit during start-up without triggering hiccup. Hiccup is enabled once output reaches regulation or time exceeds t_{SS}, whichever happens first.

When the output voltage drops below the set value, the soft start voltage will track the decrease in output voltage in a certain proportion. This situation may occur under the following conditions:

- When the input voltage is too low to maintain the set output voltage.
- When overcurrent occurs causing a decrease in output voltage.

When the above conditions are removed, the output voltage will still increase under soft start. But it should be noted that if the output voltage drops below 65% due to overcurrent, hiccup will be triggered.

Switching Frequency

The switching frequency of the SCT2333 is set by placing a resistor between RT pin and the ground.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 200kHz to 2.2MHz. When RT is floating, the frequency is 500kHz, and when RT is connected to the ground, the frequency is 1.15MHz. Use Equation 5 or the plot in Figure 10. to determine the resistance for a switching frequency needed.

$$F_{SW}(\mathrm{kHz}) = 17293 \times R(\mathrm{k\Omega})^{-0.942} \qquad (5)$$

where, Fsw is switching clock frequency.

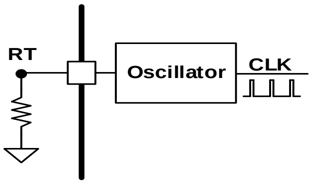


Figure 10. Setting Frequency

Frequency Spread Spectrum

To reduce EMI, the SCT2333 implements Frequency Spread Spectrum (FSS). The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these emissions across a wider range of frequencies rather than apart with fixed frequency function. In most systems containing the SCT2333, low frequency-conducted emissions from the first few harmonics of the switching frequency can be easily filtered.

The FSS circuit uses pseudo-random frequency hopping to vary the switching frequency within a specific range. The jittering span is ±6% of the switching frequency. The spread spectrum is only available while the clock of the SCT2333 devices is free running at their natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is reduced during LDO function.
- The clock is reduced at light load in PSM.
- The clock is reduced during minimum on time function.

Bootstrap Voltage Regulator and BOOT UVLO

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. A boot diode is integrated on the SCT2333 die to minimize external component count.

The UVLO of high-side MOSFET gate driver has a threshold of 2.5V. When the voltage across bootstrap capacitor drops below 2.5V, BST UVLO occurs, the voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter’s function.

Low Drop-out Function

At a given clock frequency, duty cycle is limited by minimum off time. During the condition of low voltage difference from the input to the output, to maintain the output voltage from falling, the SCT2333 extends on time past the end of the clock cycle until the required peak inductor current is achieved. The clock is allowed to start a new cycle once peak inductor current is achieved or once a predetermined maximum on time (t_{ON_max}) of approximately 9us passes. As a result, to ensure that the output voltage can better follow the changes in input voltage, when SCT2333 operates in LDO function, the switching frequency begins to decrease, with a minimum decrease to 108kHz. The minimum frequency limit avoids possible audio interference.

During slow power on and power off applications, due to the LDO function, the output voltage can closely track the slope changes of the input voltage. As the input voltage is reduced to near the output voltage, i.e., during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO function mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem, the SCT2333 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.

Minimum On Time Function

Even if the duty cycle at the set frequency is limited by the minimum on time, SCT2333 can still maintain stable adjustment of the output voltage during the transition from high input voltage to low output voltage.

If the input-output voltage ratio is too high, even if the current exceeds the compensation specified peak, the high side MOSFET cannot shut down quickly enough to adjust the output voltage. This will cause the output voltage to continuously increase until overvoltage protection is triggered. To avoid this situation, when the conduction time of the high side MOSFET touches the minimum on time due to the increase in input and output voltage difference, SCT2333 will switch to valley current control mode. After the high side MOSFET is turned off, the low side MOSFET will remain open until the inductor current drops below the required valley current. During this period, the next clock cycle will be blocked from starting, so the switching frequency will decrease. Since on time of high side MOSFET is fixed at its minimum value, this type of function resembles that of a device using a Constant On-Time (COT) control scheme.

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2333 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the inductor current is clamped at over current limitation, the converter cannot provide output current to satisfy loading requirement. Thus, the output capacitor is discharged, and the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP voltage ramps up to high clamp voltage. When FB voltage is below 65% of the reference voltage and after 256 cycles of low side current limit, the converter stops switching. After remaining OFF for 9*t_{ss}， the device restarts from soft start phase. If overload or hard short condition still exists during t_{SS} and make COMP voltage clamped at high, after t_{SS} and FB voltage keep below 65% of the reference voltage for 256 cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating function.

If the FB voltage drops below 65% of the reference voltage due to LDO function, hiccup mode will be disabled.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The SCT2333 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 115% of internal

0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 113% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2333 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 165°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 135°C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

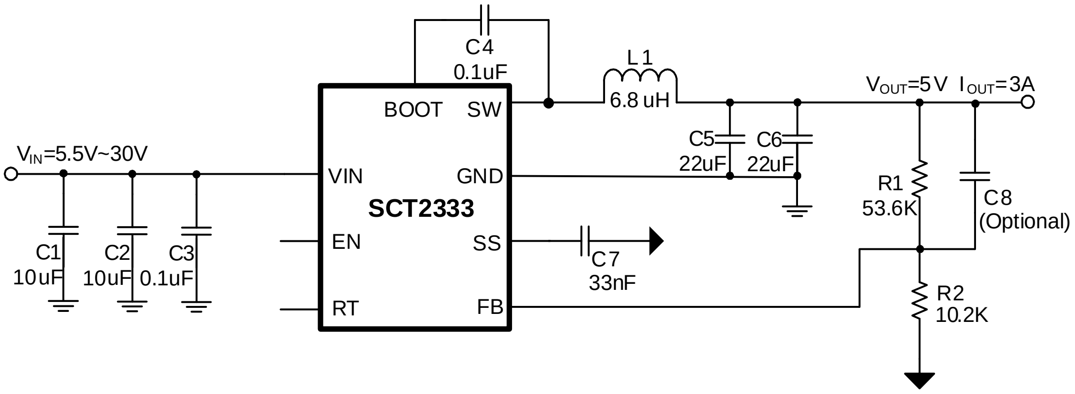


Figure 11. SCT2333 Design Example, 5V Output

Design Parameters

Design Parameters	**Example Value**
Input Voltage	24V Normal 5.5V to 30V
Output Voltage	5V
Maximum Output Current	3A
Switching Frequency	500kHz
Output voltage ripple (peak to peak)	11.6mV
Transient Response 0.7A to 2.3A load step	292mV

Output Voltage

The output voltage is set by an external resistor divider R_1 and R_2 in typical application schematic. Recommended R_2 resistance is 10.2kΩ. Use Equation 6 to calculate R_1.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_2 \tag{6}$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V.

Table 1. R_1, R_2 Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_1	R_2
3.3 V	31.6 KΩ	10.2 kΩ
5 V	53.6 KΩ	10.2 kΩ
12 V	143 KΩ	10.2 kΩ

Switching Frequency

Higher switching frequencies support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter’s overall power efficiency and thermal performance. In this design, a moderate switching frequency of 500kHz is selected to achieve both small solution size and high efficiency operation.

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 30%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 7.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \tag{7}$$

Where:

- I_{LPP} is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 8 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \tag{8}$$

Where:

- L_{MIN} is the minimum inductance required.
- f_{sw} is the switching frequency.
- V_{OUT} is the output voltage.
- $V_{IN\ (max)}$ is the maximum input voltage.
- $I_{OUT\ (max)}$ is the maximum DC load current.
- LIR is coefficient of I_{LPP} to I_{OUT}.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in Equation 9 and Equation 10.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \tag{9}$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \tag{10}$$

Where:

- I_{LPEAK} is the inductor peak current.
- I_{OUT} is the DC load current.
- I_{LPP} is the inductor peak-to-peak current.
- I_{LRMS} is the inductor RMS current.

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5A. Because of the maximum I_{LIM_HS} limited by device, the maximum output current that the SCT2333 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g., 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 11.

$$\mathrm{I_{CINRMS}} = \mathrm{I_{OUT}} * \sqrt{\frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} * (1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}})} \tag{11}$$

The worst-case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$\mathrm{I_{CINRMS}} = 0.5 * \mathrm{I_{OUT}} \tag{12}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 13 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta\mathrm{V_{IN}} = \frac{\mathrm{I_{OUT}}}{\mathrm{f_{SW}} * \mathrm{C_{IN}}} * \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} * (1 - \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}}) \tag{13}$$

For this example, two 10µF, X7R ceramic capacitors rated for 50V in parallel are used. And a 0.1µF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X7R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 14 desired.

$$\Delta \mathrm{V_{OUT}} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \tag{14}$$

Where:

- $\Delta V_{OUT}$is the output voltage ripple.
- f_{SW} is the switching frequency.
- L is the inductance of inductor.
- C_{OUT} is the output capacitance.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22µF ceramic output capacitors work for most applications.

Table 2: Typical External Component Values

VOUT	FREQUENCY	R1	R2	R_{RT}	L1	C8	COUT
5V	500kHz	53.6 kΩ	10.2 kΩ	Floating	6.8 uH	Optional	44uF
12V	500kHz	143 kΩ	10.2 kΩ	Floating	15 uH	Optional	44uF
5V	1.15MHz	53.6 kΩ	10.2 kΩ	GND	3.3 uH	Optional	33uF
12V	1.15MHz	143 kΩ	10.2 kΩ	GND	6.8 uH	Optional	33uF

Application Waveforms

V_{IN}=24V, V_{OUT}=5V, F_{SW}=500k, unless otherwise noted.

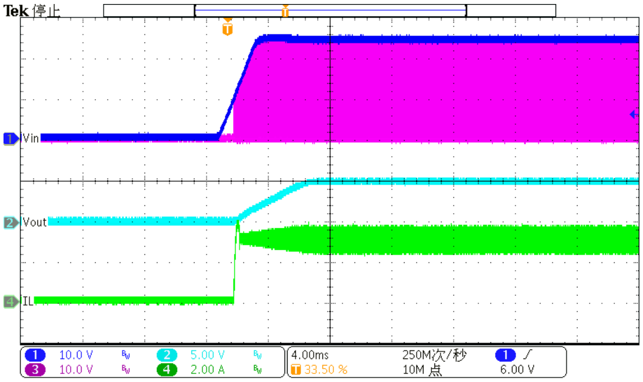


Figure 12. Power up (I_{LOAD}=3A)

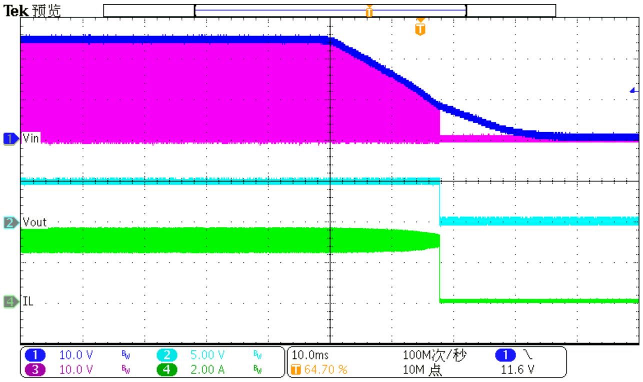


Figure 13. Power down (I_{LOAD}=3A)

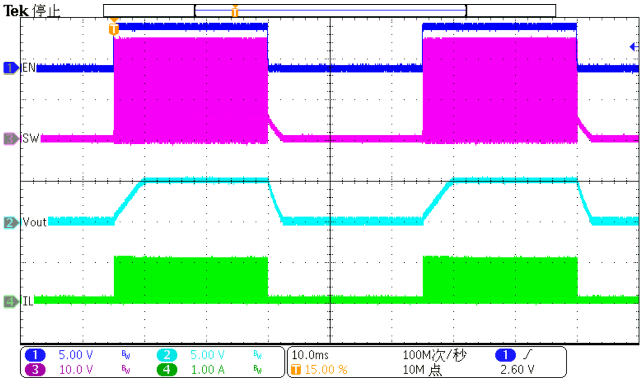


Figure 14. EN toggle (I_{LOAD}=0.1A)

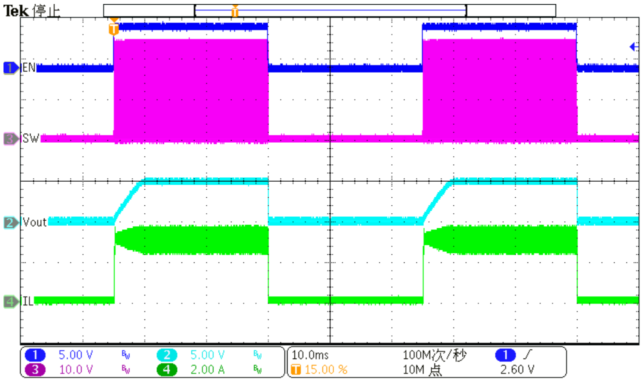


Figure 15. EN toggle (I_{LOAD}=3A)

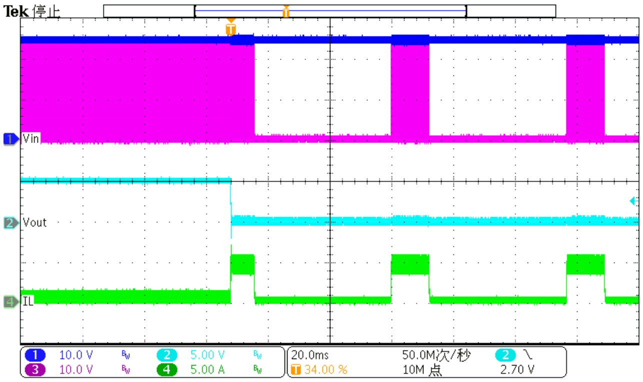


Figure 16. Over Current Protection (0.1A to hard short)

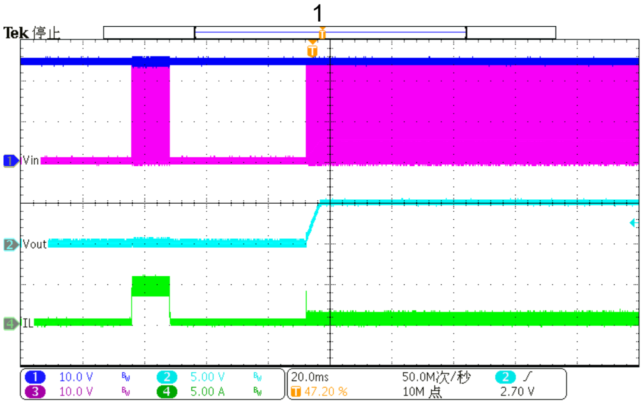


Figure 17. Over Current Release (hard short to 0.1A)

Application Waveforms

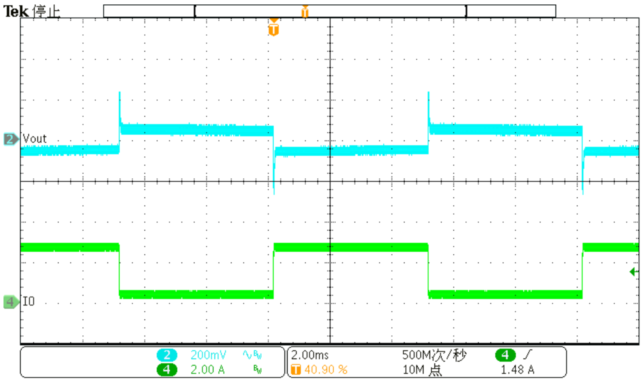


Figure 18. Load Transient (0.3A~2.7A, 1.6A/us)

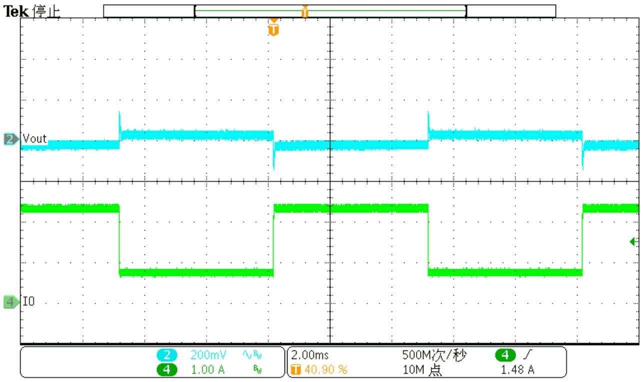


Figure 19. Load Transient (0.7A~2.3A, 1.6A/us)

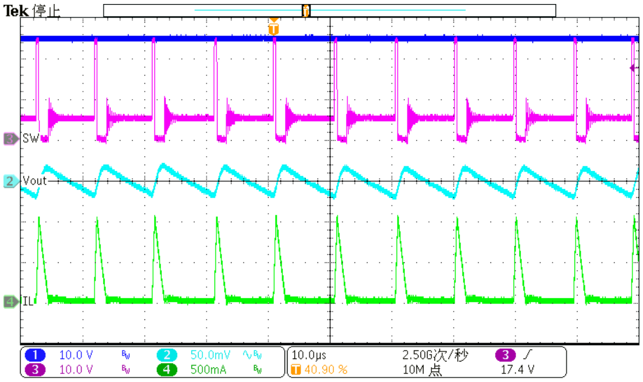


Figure 20. Output Ripple (I_{LOAD}=0.1A)

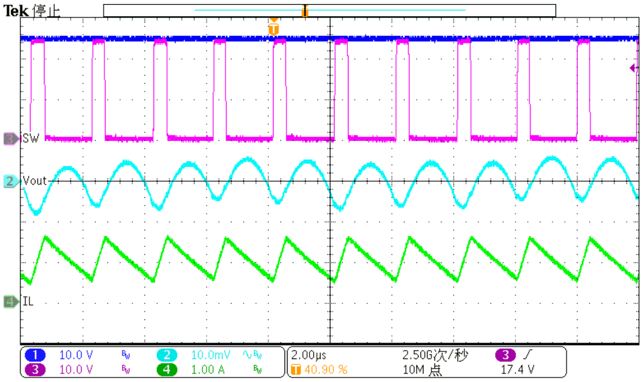


Figure 21. Output Ripple (I_{LOAD}=1A)

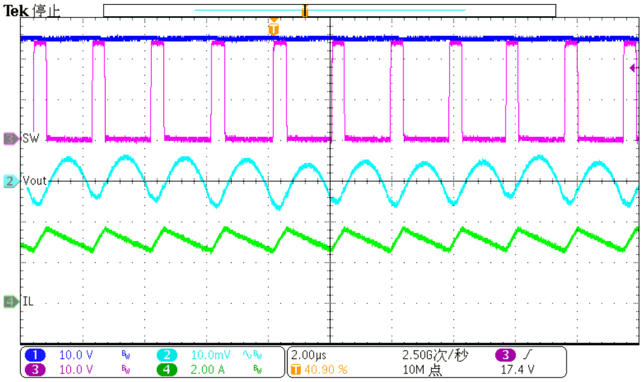


Figure 22. Output Ripple (I_{LOAD}=3A)

Figure 23. Thermal, 24V_{IN}, 5V_{OUT}, 2A

Layout Guideline

Proper PCB layout is a critical for SCT2333's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure the top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to the bottom PCB ground planes using multiple vias directly under the IC. It is recommended 10mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, SS and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

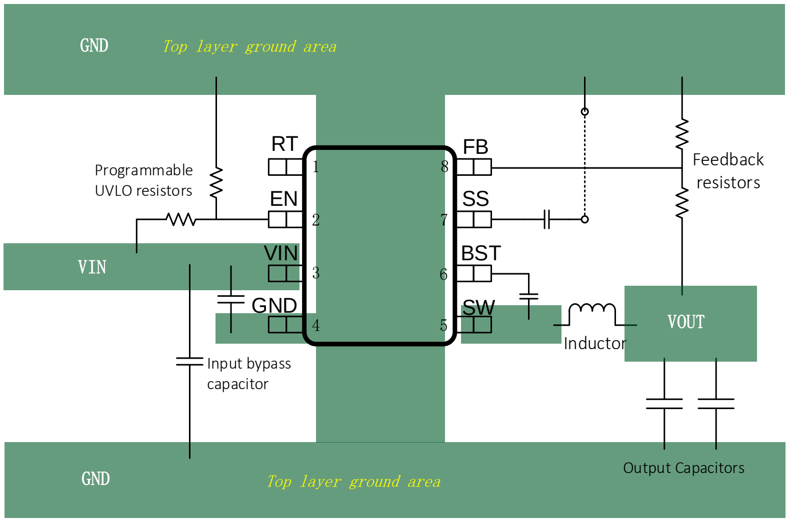
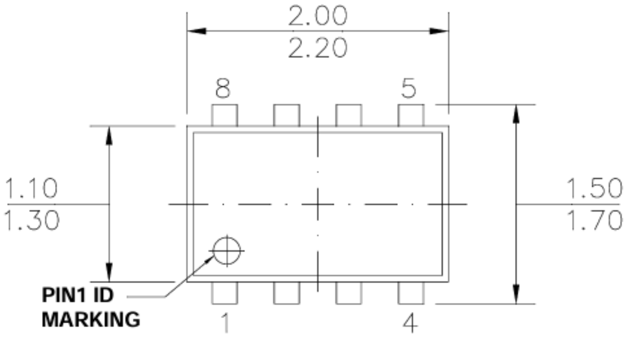
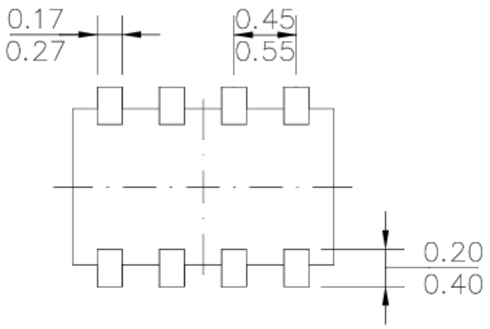


Figure 24. PCB Layout Example

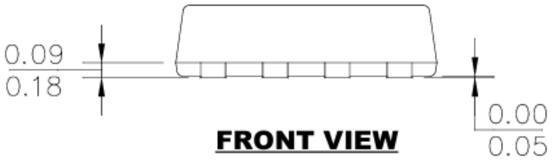
PACKAGE INFORMATION



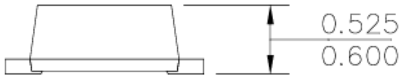
TOP VIEW



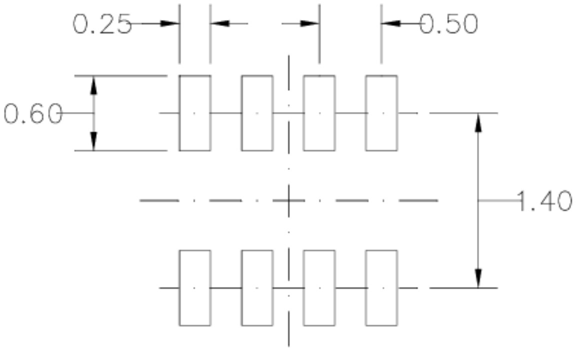
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-293, VARIATION UAAD.
6) DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION