5.5V-65V Wide Input Voltage Range Synchronous Buck Controller

FEATURES

- Synchronous DCDC Buck Controller
  - 5.5V-65V Wide Input Range
  - 0.8V-65V Adjustable Output Voltage
  - 0.8V±1% Reference Voltage
  - 40ns Minimum t_{ON} for low duty ratio
  - 150ns Minimum t_{OFF} for high duty ratio
- 100 KHz to 1.2 MHz Switching Frequency
  - Clock Synchronization In/Out capability
  - Selectable Diode Emulation or FPWM
  - Frequency Spread Spectrum Modulation
- 7.5-V Gate Drivers
  - 2.3-A Source and 3.5-A Sink Current
  - Low-side Soft Start for prebiased Start-up
- Fast Line and Load Transient Response
  - Voltage-mode control with line feedforward
  - High Gain Bandwidth Error Amplifier
- Protection Features for Robustness
  - Adjustable Soft Start time
  - Hiccup-mode Overcurrent Protection
  - Input UVLO with hysteresis
  - VCC and Gate-drive UVLO Protection
  - Precision Enable Input Threshold
  - Open-drain Power Good Indicator
  - Over Temperature Shutdown Protection
- External VCC Input for Bypassing Internal LDO
- Available in QFN-20L 3.5mmx4.5mm Package

APPLICATIONS

- High Current Distributed Power Systems
- Telecom, Datacom
- Non-isolated PoE and IP Camera
- Industrial Motor Control
- High Power Automotive DCDC

DESCRIPTION

The SCT82630 is a 65V voltage mode control synchronous buck controller with line feed forward. 40ns minimum on-time of controlled high side MOSFET supports high conversion ratio, enabling the direct step-down conversion from a 48V input to low-voltage rail reducing system complexity and solution cost. The device operates at nearly 100% duty cycle if needed during input voltage drops as low as 5.5V.

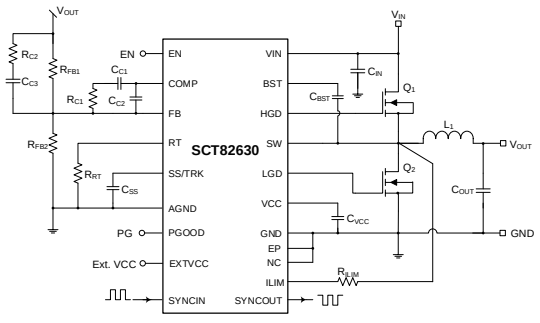
The SCT82630 support Forced-PWM (FPWM) and Diode Emulation Mode. FPWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition. The adjustable switching frequency as high as 1.2MHz can be synchronized to an external clock source to eliminate beat frequencies in noise sensitive applications.

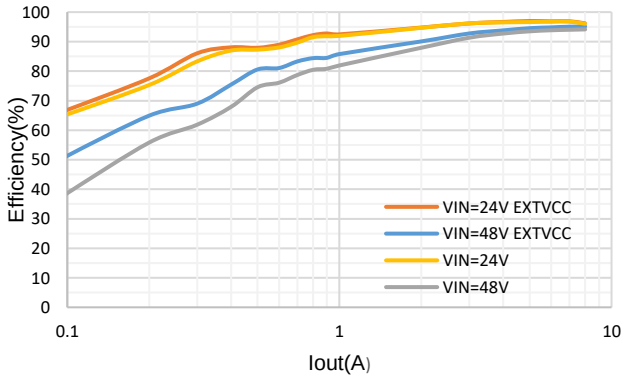
An external voltage or the output of the buck converter itself source can power internal VCC or EXTVCC helping to increase overall efficiency and decrease internal self-heating from power dissipated in the internal VCC LDO even with 5V output voltage.

The SCT82630 features additional features for flexible and robust design including a configurable soft start, an open-drain power-good monitor for fault reporting and output monitoring, monotonic start-up into pre-biased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line under voltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The device is available in a low-profile package QFN-20L 3.5mmx4.5mm with enhanced thermal power pad.

TYPICAL APPLICATION





Efficiency vs Load Current, Vout=12V, DCM

REVISION HISTORY

Revision 1.0: Released to Market

Revision 1.1: Updata Package information

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT82630DHK	2630	QFN-20L 4.5mmX3.5mm

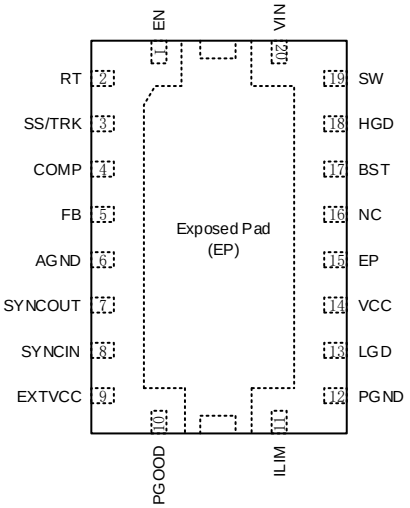
1) For Tape & Reel, Add Suffix R (e.g. SCT82630DHKR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN	-0.3	72	V
SW	-1	72	V
SW (20ns transient)	-5	80	V
ILIM	-1	72	V
EN	-0.3	72	V
VCC, EXTVCC,LO	-0.3	14	V
FB, COMP, SS/TRK, RT	-0.3	6	V
SYNCIN	-0.3	14	V
BST	-0.3	86	V
BST to VCC		72	V
BST to SW	-0.3	14	V
VCC to BST (20ns transient)		7	V
LO (20ns transient)	-3		V
PGOOD	-0.3	14	V
Junction temperature	-40	125	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: 20-Lead Plastic QFN 3.5mmx4.5mm

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	I/O(1)	PIN FUNCTION
EN	1	I	Enable input and under voltage lockout programming pin. If the EN voltage is below 0.4 V, the controller is in the shutdown mode with all functions disabled. If the EN voltage is greater than 0.4 V and less than 1.2 V, the regulator is in standby mode with the VCC regulator operating, the SS pin grounded, and no switching at the HGD and LGD outputs. If the EN voltage is above 1.2V, the SS/TRK voltage can ramp and pulse-width modulated gate-drive signals are delivered to the HGD and LGD pins. The user can use EN pin program input under voltage lockout UVLO threshold. A 10μA current source is enabled when EN exceeds 1.2 V and flows through the external UVLO programing resistor divider to provide hysteresis. Hysteresis can be adjusted by varying the resistance of the external divider.
RT	2	I	Oscillator frequency adjust pin. The internal oscillator frequency is programmed with a single resistor between RT and the AGND. Programmed oscillator frequency is 100KHz to 1.2MHz. An RT pin resistor is required even when using the SYNCIN pin to synchronize to an external clock.

SS/TRK	3	I	Soft-start and voltage-tracking pin. An internal 10μA current source charges an external capacitor to set the ramp rate of the error amplifier reference during start-up. When the SS/TRK pin voltage is less than 0.8 V, the SS/TRK voltage is noninverting input of the error amp. When the SS/TRK voltage exceeds 0.8 V, the noninverting of amplifier is controlled by the internal 0.8-V reference. SS/TRK is discharged to ground during standby and fault conditions. After start-up, the SS/TRK voltage is clamped at 115 mV above the FB pin voltage. If FB falls due to a load fault, SS/TRK is discharged to a level 115 mV above FB to provide a controlled recovery when the fault is removed. Voltage tracking can be implemented by connecting a low impedance reference between 0 V and 0.8 V to the SS/TRK pin. The 10μA SS/TRK charging current flows into the reference and produces a voltage error if the impedance is not sufficiently low. Connect a minimum capacitance 2.2nF from SS/TRK to AGND.
COMP	4	O	Low impedance output of the internal error amplifier. Connect the loop compensation network between the COMP pin and the FB pin.
FB	5	I	Feedback connection to the inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage regulation level.
AGND	6	P	Analog ground.
SYNCOUT	7	O	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the high-side FET gate drive. Connect SYNCOUT of the master SCT82630 to the SYNCIN pin of a second SCT82630 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turn-on transitions. Note that the SYNCOUT pin does not provide 180° interleaving when the controller is operating from an external clock that is different from the free-running frequency set by the RT resistor.
SYNCIN	8	I	Dual function pin for providing an optional clock input and for enabling diode emulation by the low-side MOSFET. Connecting a clock signal to the SYNCIN pin synchronizes switching to the external clock. Diode emulation by the low-side MOSFET is disabled when the controller is synchronized to an external clock, and negative inductor current can flow in the low-side MOSFET with light loads. A continuous logic low state at the SYNCIN pin enables diode emulation to prevent reverse current flow in the inductor. Diode emulation results in discontinuous mode operation (DCM) at light loads, which improves efficiency. A logic high state at the SYNCIN pin disables diode emulation producing forced-PWM (FPWM) operation. During soft-start when SYNCIN is high or a clock signal is present, the SCT82630 operates in diode emulation mode until the output is in regulation, then gradually increases the SW zero-cross threshold, resulting in a gradual transition from DCM to FPWM.
EXTVCC	9	I	External VCC Input. When EXTVCC exceeds 4.7V, an internal switch connects this pin to internal VCC and shuts down the internal regulator so that the controller and gate drive power is drawn from EXTVCC. EXTVCC should not exceed 14V.
PGOOD	10	O	Power Good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered at 0.8 V.
ILIM	11	I	Current limit and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for RDS(on) sensing or to a current sense resistor connected to the source of the low-side FET.
PGND	12	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low-side MOSFET or the ground side of a shunt resistor.
LGD	13	P	Low-side MOSFET gate drive output. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.

VCC	14	O	Output of the 7.5V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close as possible to the controller. Controller bias can be supplied from an external supply that is greater than the internal VCC regulation voltage. Use caution when applying external bias to ensure that the applied voltage is not greater than the minimum VIN voltage and does not exceed the VCC pin maximum operating rating, see Recommended Operating Condition.
EP	15	-	Pin internally connected to exposed pad of the package. Electrically isolated.
NC	16	-	No electrical connection.
BST	17	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor. The bootstrap capacitor supplies current to the high-side FET gate and must be placed as close as possible to controller. If an external bootstrap diode is used to reduce the time required to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.
HGD	18	P	High-side MOSFET gate drive output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
SW	19	P	Switching node of the buck controller. Connect to the bootstrap capacitor, the source terminal of the high side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths.
VIN	20	P	Supply voltage input for the VCC LDO regulator.
EP	-	-	Exposed pad of the package. Electrically isolated. Solder to the system ground plane to reduce thermal resistance.

(1) P=Power, G=Ground, I=Input, O=Output

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	5.5	65	V
VCC	External VCC bias rail	8	13	V
EXTVCC	External EXTVCC bias rail	4.7	13	V
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	+1	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	37	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	28	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	2.1	
$R_{\theta JB}$	Junction to board thermal resistance(1)	12	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT82630 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT82630. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 48 V, V_{EN} = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		5.5		65	V
I_{Q_SHDN}	Shutdown input current	EN=0, Vcc<1V		10		μA
I_{Q_STBY}	Standby input current	EN=1V,		1.4		mA
I_{Q_OP}	Operating input current, not switching	EN=1.5V, $V_{SS/TRK}$=1V		1.5		mA
V_{CC}	VCC regulation voltage	$V_{SS/TRK}$=0V, 9V≤V_{IN}≤100V, 0mA<I_{VCC}≤20mA	7.1	7.5	7.8	V
V_{CC_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		4.5 200		V mV
V_{CC_LDO}	VIN to VCC dropout voltage	V_{IN}=6V, $V_{SS/TRK}$=0V, I_{VCC}=20 mA		0.08		V
I_{SC_LDO}	VCC short circuit current	$V_{SS/TRK}$=0V, V_{CC} =0V	40	50	70	mA
V_{EXTVCC}	EXTVCC switchover voltage	V_{IN} rising		4.7		V
	Hysteresis			100		mV
Error Amplifier						
V_{REF}	FB reference voltage	FB connected to COMP	0.792	0.8	0.808	V
I_{FB_BIAS}	FB input bias current	V_{FB}=0.8V	-0.1		0.1	uA
AVOL	DC gain			94		dB
GBW	Unity gain bandwidth			6.5		MHz
I_{COMP_SRC}	EA maximum source current	V_{FB}=V_{REF}-100mV, V_{COMP}=1V	1000			μA
I_{COMP_SNK}	EA maximum sink current	V_{FB}=V_{REF}+100mV, V_{COMP}=1V	1000			μA
V_{COMP_H}	COMP output high voltage	V_{FB}=0V, COMP sourcing 1mA		4.5		V
V_{COMP_L}	COMP output low voltage	COMP sinking 1mA		0.25		V
Enable						
V_{EN_SHDN}	Shutdown to standby EN threshold	V_{EN} rising		0.41		V
	Hysteresis			30		mV
V_{EN}	Standby to operating EN threshold	V_{EN} rising	1.164	1.2	1.236	V
I_{EN_HYS}	Standby to operating hysteresis	V_{EN}=1.5V	9	10	11	μA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Soft-start and Voltage Tracking						
I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK}$=0V	8.5	10	12	uA
R_{SS}	SS/TRK discharging FET resistance	V_{EN}=1V, $V_{SS/TRK}$=0.1V		12		Ω
V_{SS-FB}	SS/TRK to FB offset			62		mV
V_{CC_CLAMP}	SS/TRK clamp voltage	$V_{SS/TRK}$ – V_{FB}, V_{FB}=0.8V		120		mV
Power Good Indicator						
PG_{UTH}	PGOOD high to low - FB upper threshold	% of V_{REF}, V_{FB} rising	106	109	110	%
PG_{U_HYS}	PGOOD upper threshold hysteresis	% of V_{REF}		3		%
PG_{LTH}	PGOOD high to low - FB lower threshold	% of V_{REF}, V_{FB} falling	90	92	94	%
PG_{L_HYS}	PGOOD upper threshold hysteresis	% of V_{REF}		2		%
t_{PG_rising}	PGOOD rising filter	FB to PGOOD rising edge		25		us
$t_{PG\_falling}$	PGOOD falling filter	FB to PGOOD falling edge		25		us
V_{PG_OL}	PGOOD low state output voltage	V_{FB}=0.9V, I_{PGOOD}=2mA			150	mV
I_{PG_OH}	PGOOD high state leakage current	V_{FB}=0.8V, V_{PGOOD}=13V			100	nA
Switching Frequency and External Clock Synchronization						
F_{SW1}	Switching frequency 1	R_{RT}=100 kΩ (1%)		100		kHz
F_{SW2}	Switching frequency 2	R_{RT}=24.9 kΩ (1%)		400		kHz
F_{SW3}	Switching frequency 3	R_{RT}=12.5 kΩ (1%)		780		kHz
F_{RANGE_CLK}	SYNCIN external clock frequency range using	% of nominal frequency set by RT	-20		50	%
$V_{SYNCI-IH}$	Minimum SYNCIN input logic high		1.8			V
$V_{SYNCI-IL}$	Maximum SYNCIN input logic low				0.8	V
R_{SYNCIN}	SYNCIN input resistance	V_{SYNCIN}=3V		20		kΩ
t_{SYNCPW}	SYNCIN minimum pulse width	Minimum high state or low state duration	50			ns
$V_{SYNCO-OH}$	SYNCOUT high state output voltage	$I_{SYNCOUT}$=-1mA (sourcing)	3			V
$V_{SYNCO-OL}$	SYNCOUT low state output voltage	$I_{SYNCOUT}$= 1mA (sinking)			0.4	V
$t_{SYNCOUT}$	Delay from HGD rising to SYNCOUT leading edge	V_{SYNCIN}= 0V, F_{SW}=400KHz, RT=24.9 kΩ		1030		ns
t_{SYNCIN}	Delay from SYNCIN leading edge to HGD rising	50% to 50%		220		ns
F_{JITTER}	Frequency spread spectrum in percentage of Fsw			±6		%
PWM Control						
$t_{ON(MIN)}$	Minimum control on-time	V_{BST}-V_{SW}=7V, HGD 50% to 50%		40		ns
$t_{OFF(MIN)}$	Minimum control off-time	V_{BST}-V_{SW}=7V, HGD 50% to 50%		150		ns
$D_{100K(MAX)}$	Maximum duty cycle	F_{SW}=100kHz, 5V<V_{IN}<100V		98		%
$D_{400K(MAX)}$	Maximum duty cycle	F_{SW}=400kHz, 5V<V_{IN}<100V		92		%
$V_{RAMP(MIN)}$	Ramp valley voltage (COMP at 0% duty cycle)			300		mV
K_{FF}	PWM feedforward gain (V_{IN}/V_{RAMP})	5V<V_{IN}<100V		12		V/V
Bootstrap Diode and Undervoltage Threshold						
$V_{BST-FWD}$	Diode forward voltage	VCC to BST, BST sourcing 20mA		0.8		V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$=0V, V_{SW}=48V, V_{BST}=54V		70		uA
V_{BST-UV}	BST to SW undervoltage detection	V_{BST}-V_{SW} falling		3.4		V
	Hysteresis			420		mV
Over Current Protection and Valley Current Limiting						
I_{RS}	ILIM source current, R_{SENSE} mode	Low voltage detected at ILIM	90	100	110	uA
I_{RDSON}	ILIM source current, $R_{DS(ON)}$ mode	SW voltage detected at ILIM, T_J=25°C	180	200	220	uA
$I_{RDSONTC}$	ILIM current tempco	R_{DS-ON} mode		4500		ppm/°C
I_{RSTC}	ILIM current tempco	R_{SENSE} mode		0		ppm/°C
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		-8	-2	3.5	mV
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated		128		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release		16384		cycles
Short Circuit Protection – Duty Cycle Clamp						
$V_{CLAMP-OS}$	Clamp offset voltage – no current limiting	Clamp to COMP steady state offset voltage		0.2+V_{IN}/75+1		V
$V_{CLAMP-MIN}$	Minimum clamp voltage	Clamp voltage with continuous current limiting		0.3+V_{IN}/150		V
DIODE Emulation						
V_{ZCD-SS}	Zero crossing detect ZCD soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after the first HGD pulse		0		mV
$V_{ZCD-DIS}$	Zero crossing detect ZCD disable threshold (CCM)	ZCD threshold measured at SW pin 1000 clock cycles after the first HGD pulse		200		mV
V_{DEM-TH}	Diode emulation zero crossing threshold	Measured at SW with V_{SW} rising	-15	-5	5	mV
Gate Driver						
R_{HGD-UP}	HGD high state resistance, HGD to BST	V_{BST}–V_{SW} =7V, I_{HGD}=-100mA		1.3		Ω
$R_{HGD-DOWN}$	HGD low state resistance, HGD to SW	V_{BST}–V_{SW} =7V, I_{HGD}= 100mA		0.6		Ω
R_{LGD-UP}	LGD high state resistance, LGD to VCC	V_{BST}–V_{SW} =7V, I_{LGD}=-100mA		1.3		Ω
$R_{LGD-DOWN}$	LGD low state resistance, LGD to SW	V_{BST}–V_{SW} =7V, I_{LGD}= 100mA		0.6		Ω
t_{HGD-TR} t_{LGD-TR}	HGD, LGD rise times	V_{BST}–V_{SW} =7V, C_{LOAD}=1nF, 20% to 80%		7		ns
t_{HGD-TF} t_{LGD-TF}	HGD, LGD fall times	V_{BST}–V_{SW} =7V, C_{LOAD}=1nF, 80% to 20%		4		ns
t_{HGD-DT}	HGD turn on dead time	V_{BST}–V_{SW} =7V, LGD off to HGD on. 50% to 50%		25		ns
t_{LGD-DT}	LGD turn on dead time	V_{BST}–V_{SW} =7V, HGD off to LGD on. 50% to 50%		22		ns
Thermal Shutdown						
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		175 20		°C °C

TYPICAL CHARACTERISTICS

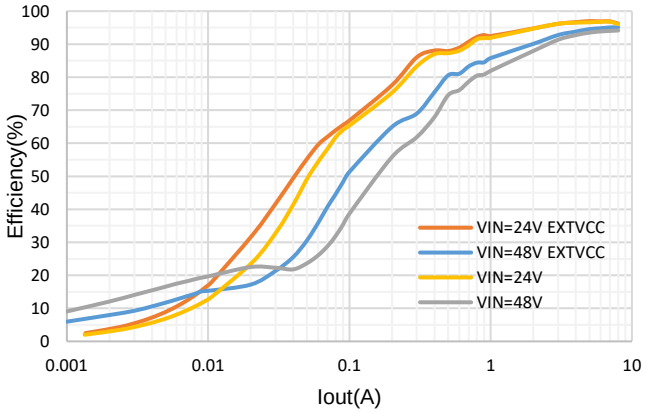


Figure 1. Efficiency vs Load Current, Vout=12V, DCM

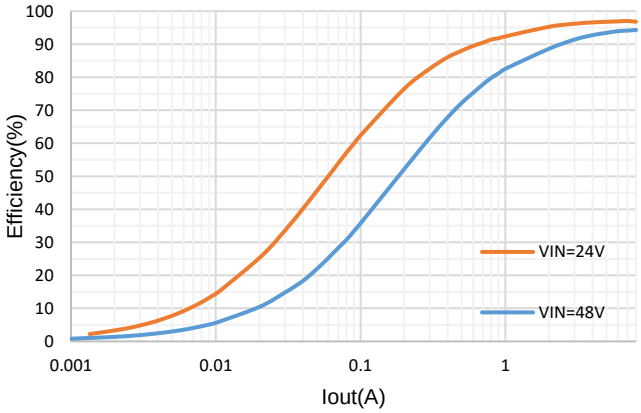


Figure 2. Efficiency vs Load Current, Vout=12V, FCCM

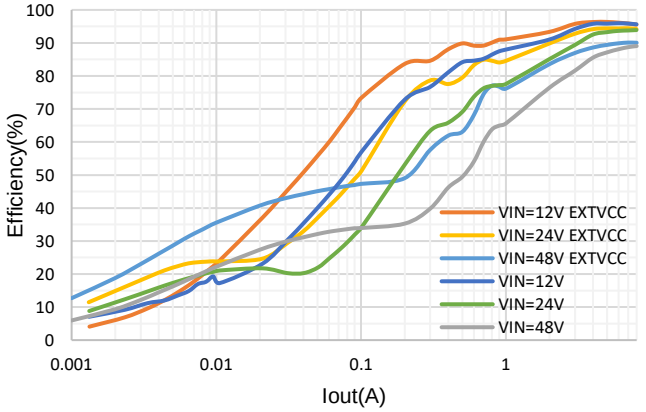


Figure 3. Efficiency vs Load Current, Vout=5V, DCM

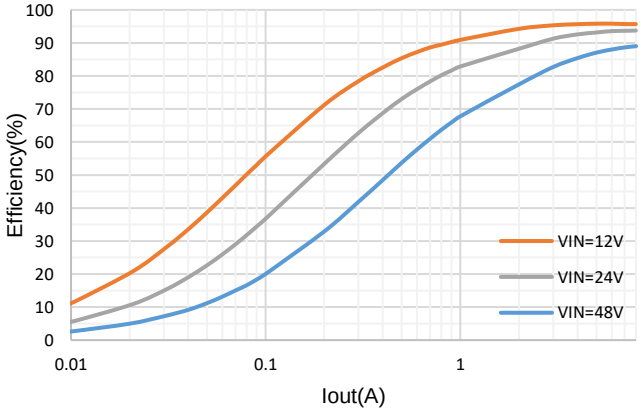


Figure 4. Efficiency vs Load Current, Vout=5V, FCCM

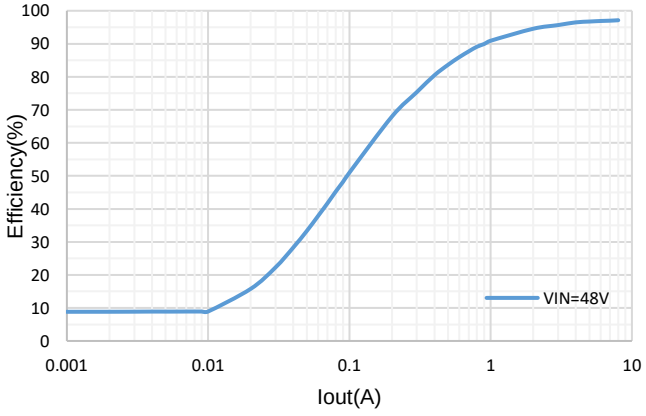


Figure 5. Efficiency vs Load Current, Vout=24V, DCM

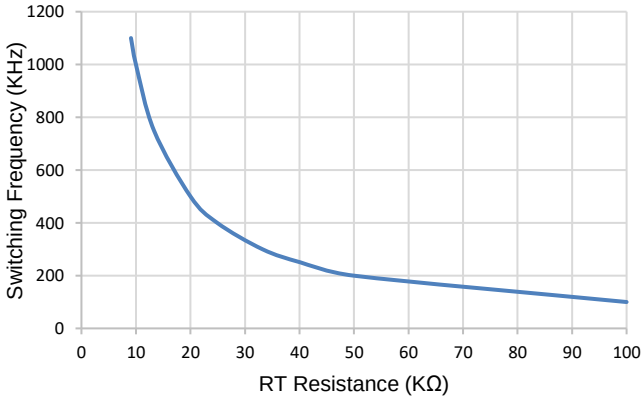


Figure 6. Oscillator Frequency vs RT Resistance

TYPICAL CHARACTERISTICS

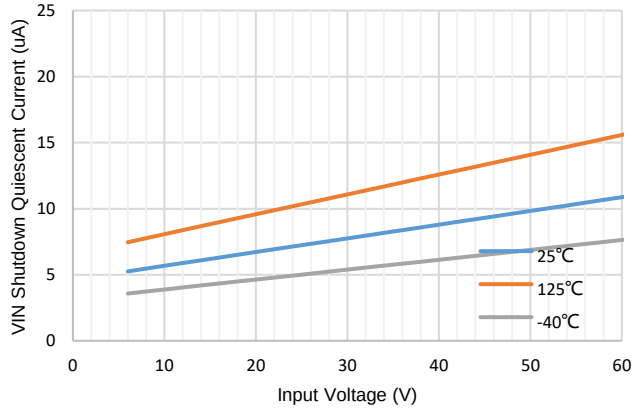


Figure 7. $I_{SHUTDOWN}$ vs Input Voltage

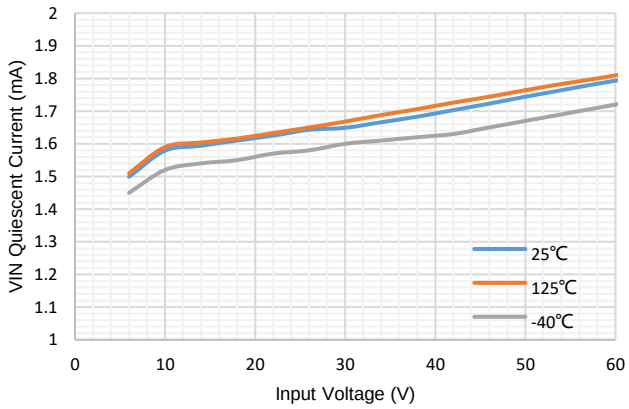


Figure 8. I_Q vs Input Voltage

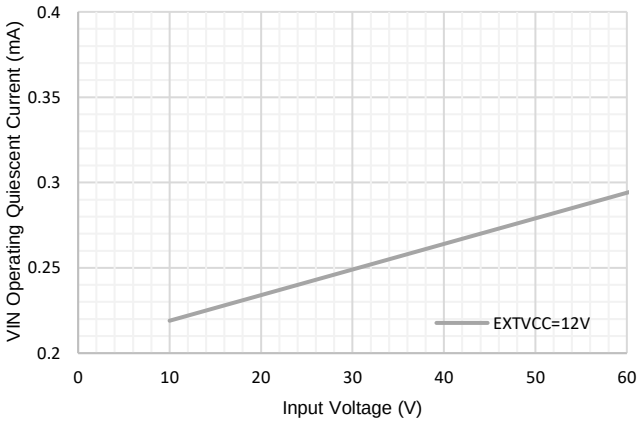


Figure 9. VIN Quiescent Current with External VCC Applied

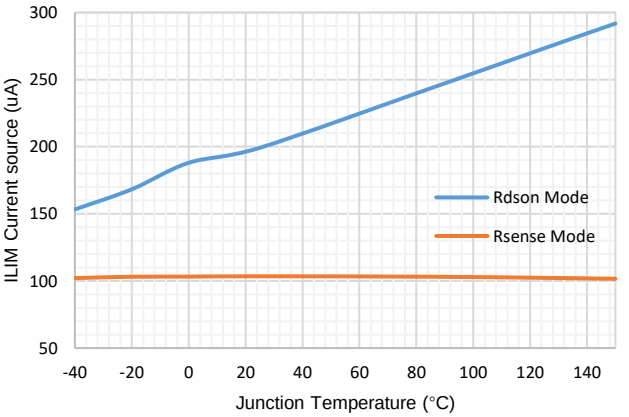


Figure 10. ILIM Current Source vs TJ

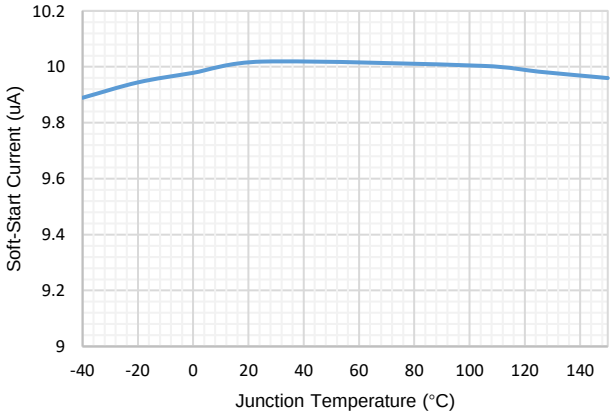


Figure 11. SS/TRK Current Source vs TJ

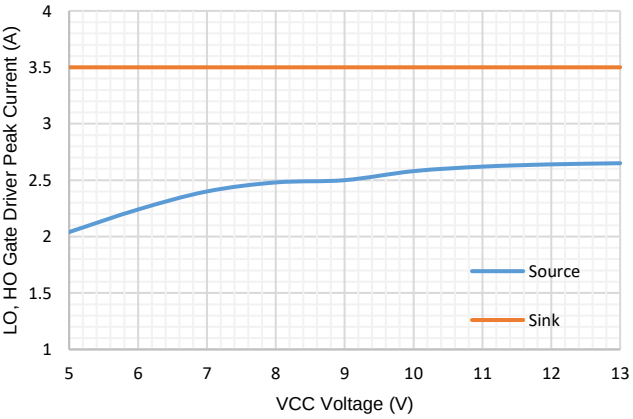


Figure 12. Gate Driver Peak Current vs VCC Voltage

TYPICAL CHARACTERISTICS

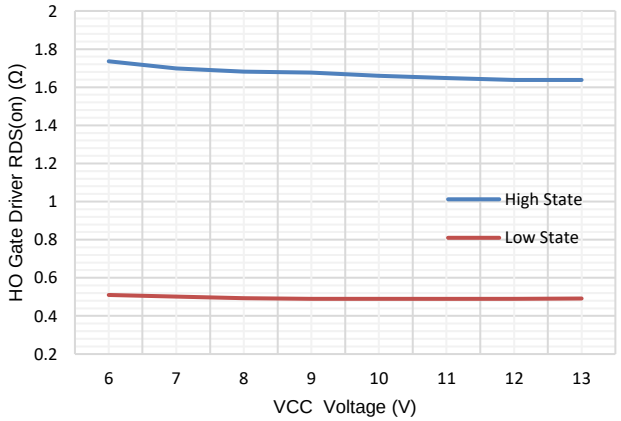


Figure 13. HO Driver Resistance vs VCC Voltage

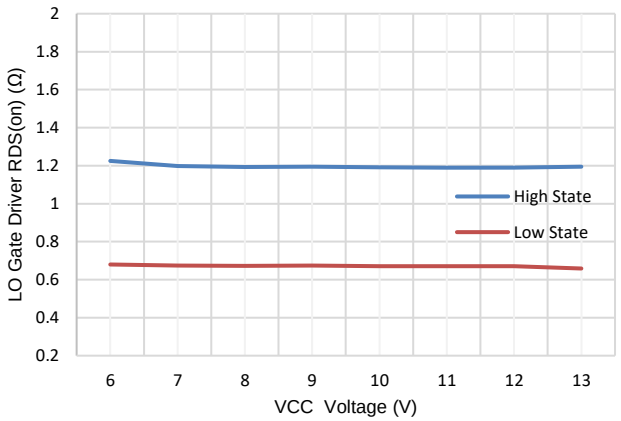


Figure 14. LO Driver Resistance vs VCC Voltage

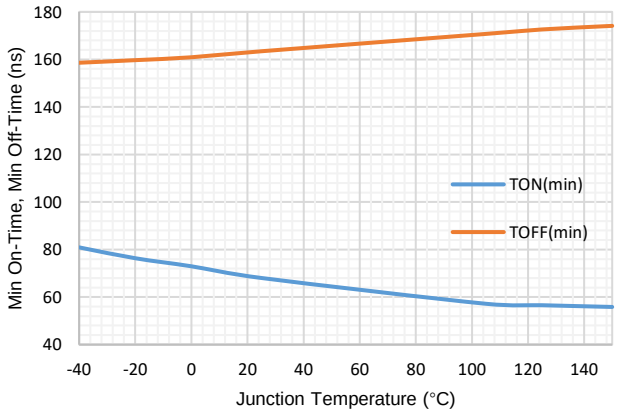


Figure 15. $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ vs TJ

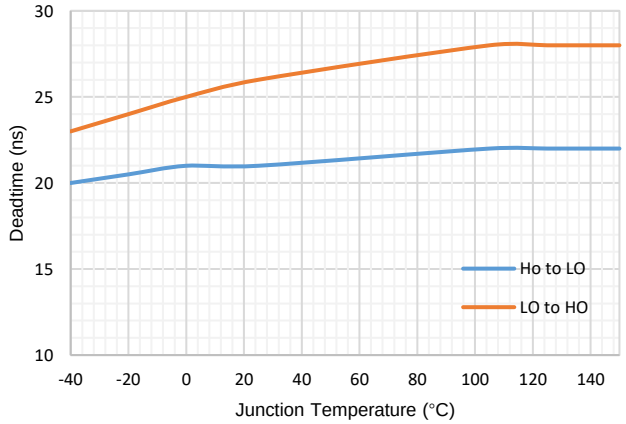


Figure 16. Deadtime vs TJ

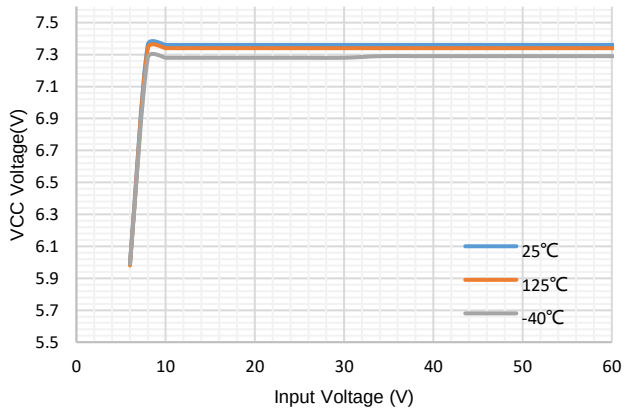


Figure 17. VCC Voltage vs Input Voltage

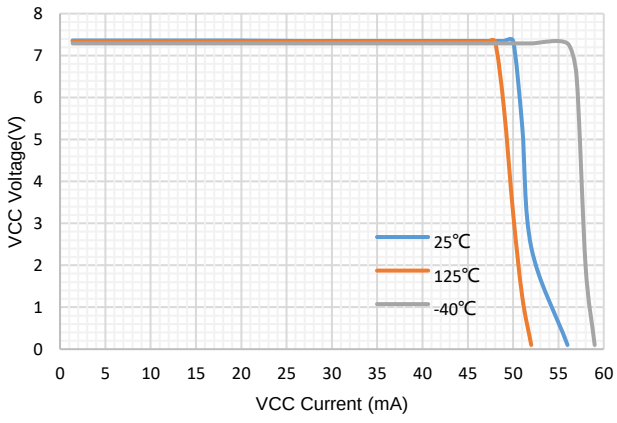


Figure 18. VCC vs ICC Characteristic

FUNCTIONAL BLOCK DIAGRAM

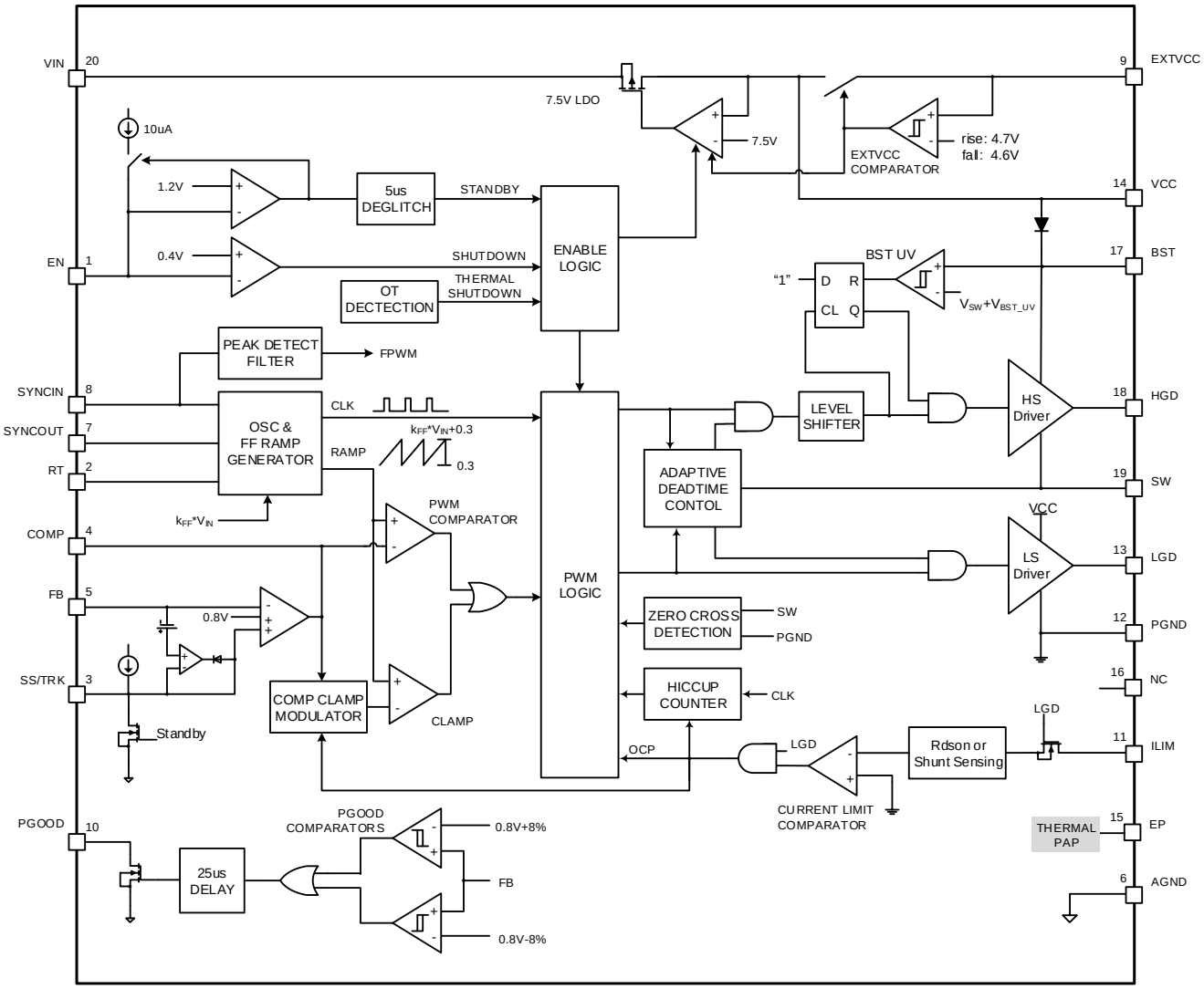


Figure 19. Functional Block Diagram

OPERATION

Overview

The SCT82630 is a synchronous buck controller, adopting voltage mode with input feedforward, to implement a high efficiency step-down DCDC power supply for excellent line transient response over a 5.5V-65V wide VIN range. The output voltage range is from 0.8 V to 65 V. Voltage-mode control supports wide duty cycle range for high input/output voltage conversion ratio and low dropout applications as well. It continues to operate during input voltage drops as low as 6 V, at nearly 100% duty cycle if needed, making it an excellent choice for high performance industrial control, robotic, Datacom, and networking communication infrastructure.

The device drives external high-side and low-side NMOS power switches with robust 7.5V gate drivers suitable for standard threshold MOSFETs.

The SCT82630 support Forced-PWM (FPWM) and Diode Emulation Mode. FPWM operation eliminates switching frequency variation to minimize EMI, while user selectable diode emulation lowers current consumption at light-load condition. The operating frequency is programmable from 100 kHz to 1.2MHz and can be synchronized to an external clock source to eliminate beat frequencies in noise-sensitive applications. The device features clock synchronization with clock input and clock output. A 180° out-of-phase clock output relative to the internal oscillator at SYNCOUT configures cascaded or multichannel power supplies to reduce input capacitor ripple current and EMI filter size.

The SCT82630 features Frequency Spread Spectrum FSS with ±6% jittering span of the setting switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

An external voltage or the output of the buck converter itself source can power internal VCC or EXTVCC helping to increase overall efficiency and decrease internal self-heating from power dissipated in the internal VCC LDO even with 5V output voltage.

Cycle-by-cycle current limiting and over current protection can be implemented with either sensing the low-side FET RDS(on) or a current sense resistor. The SCT82630 features additional features for flexible and robust design including a configurable soft start, an open-drain power-good monitor for fault reporting and output monitoring, monotonic start-up into pre-biased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line under voltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The SCT82630 controller is available in a 4.5-mm × 3.5-mm thermally enhanced, 20-pin QFN package

Input Voltage Range

The SCT82630 operational input voltage range is from 5.5V to 65V. The device is intended for step-down conversions from 12-V, 24-V, 48-V unregulated, semi-regulated, and fully regulated supply rails. An internal LDO regulator provides a 7.5V VCC bias rail for the gate drive and control circuits assuming the input voltage is higher than 7.5 V plus the necessary regulator dropout specification.

Output Voltage Regulation Point and Accuracy

The feedback reference voltage at the FB pin is typical 0.8 V with a feedback system accuracy over the full junction temperature range of ±1%. Junction temperature range for the device is –40°C to +125°C. the SCT82630 is generally capable of providing output voltages in the range of 0.8 V to a maximum of 65V or slightly less than VIN depending on switching frequency and load current levels. The output voltage regulation level during normal operation is set by the feedback resistor network, RFB1 and RFB2, connected to the output and FB pin.

High Voltage Internal VCC Bias Supply Regulator and EXTVCC Auxiliary Supply

Power for the high side and low side MOSFET drivers and most other internal control circuitry is derived from the VCC pin. An internal high-voltage VCC regulator directly to input voltage pin up to 65V. The output of internal VCC regulator is set up 7.5V. When the input voltage is below the VCC set point level, the VCC output tracks V_{IN} with a small voltage drop. Connect a ceramic decoupling capacitor between 1μF and 5μF from VCC to AGND for stability.

The VCC regulator output has a current limit of 40 mA (minimum). At power up, when the VCC voltage exceeds its rising UVLO threshold of 4.5 V, the output is enabled if EN is above 1.2V, and the soft-start sequence begins. The output remains active until the VCC voltage falls below its falling UVLO threshold of typical 4.3 V or if EN goes to a standby or shutdown state.

There are two ways powering the VCC pin with the external source helping to increase overall efficiency and decrease internal self-heating through power dissipated in the LDO. Connecting the output voltage or an auxiliary bias supply rail (up to 13V) to VCC using a diode. Or powering the EXTVCC pin with an external power source or from output voltage directly which is very convenient for customer especially when output voltage is setup at 5V as shown in Figure 20. If the EXTVCC pin is tied to an external source larger than 4.7V, then the internal VCC LDO is shut down and an internal switch shorts the EXTVCC pin to the VCC pin. This external power source could be the output of the buck switching converter itself if the output is programmed to higher than 4.7V.

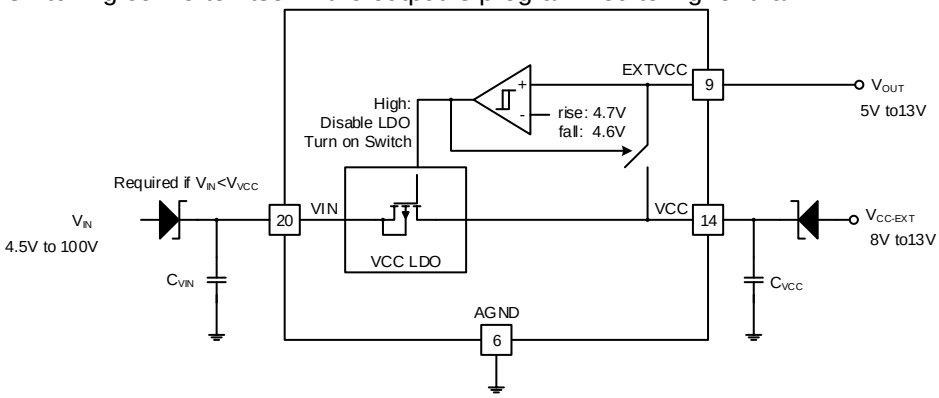


Figure 20. VCC Bias Supply Connecting EXTVCC Auxiliary Supply

Enable and programmable UVLO

The SCT82630 can be shut down using the EN pin. Pulling this pin below 1.2V prevents the controller from switching, and less than 0.41V disables most of the internal bias circuitry, including the VCC regulator. The shutdown IQ is about 7.2μA typical.

The EN input supports adjustable input under voltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN connects to a comparator-based input referenced to a 1.2V bandgap voltage. An external logic signal can be used to drive the N input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the SCT82630 is to connect EN directly to VIN. This allows self-power-up of the regulator when VCC is within its valid operating range. However, many applications benefit from using a resistor divider RUVLO1 and RUVlO2 as shown in Figure 21 to establish a precision UVLO level. Use Equation 1 and Equation 2 to calculate the UVLO resistors given the required input power-up and power-down voltages.

$$R_{UVLO1} = \frac{V_{IN(ON)} - V_{IN(OFF)}}{I_{HYS}} \quad (1)$$

$$R_{UVLO2} = R_{UVLO1} \cdot \frac{V_{EN}}{V_{IN(ON)} - V_{EN}} \quad (2)$$

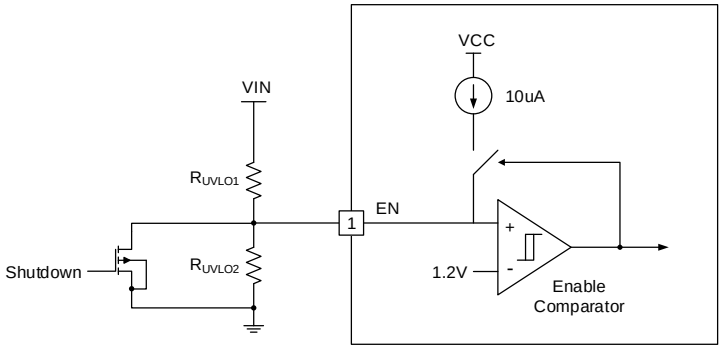


Figure 21. Programmable Input Voltage VIN UVLO Thresholds

Soft Start and Voltage Tracking

The SS/TRK pin voltage controls start-up of output voltage. After the EN pin exceeds its rising threshold of 1.2 V, the SCT82630 begins regulating the output to the level dictated by the feedback resistor network and SS/TRK voltage. A 10μA current source charges the soft-start capacitor connecting SS/TRK pin. Soft start avoids inrush current as a result of high output capacitance to avoid an overcurrent condition. The inrush stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by Equation 3.

$$t_{ss} = \frac{C_{SS} * V_{REF}}{I_{SS}} \quad (3)$$

Where

- C_{SS} is the soft-start capacitance
- V_{REF} is the 0.8V reference voltage
- I_{SS} is the 10μA current sourced from the SS/TRK pin

Calculate C_{SS} using Equation 4.

$$Css\ [nF] = 12.5 \cdot t_{SS}\ [mS] \quad (4)$$

The SS/TRK pin is internally clamped to VFB + 115 mV to allow a soft-start recovery from an overload event. The clamp circuit requires a soft-start capacitance greater than 2nF for stability and has a current limit of approximately 2mA.

The SS/TRK pin also serves as a tracking pin when master-slave power supply tracking is required. Coincident, ratiometric, and offset tracking modes are achieved by simply dividing down the output voltage of the master with a resistor network. For coincident tracking, make the divider ratio from the external supply the same as the divider ratio for the differential feedback voltage. ratiometric tracking could be achieved by using a different ratio than the differential feedback (Figure 22). Note that the small soft-start capacitor charging current is always flowing, producing a small offset error. To minimize this error, select the tracking resistive divider values to be small enough to make this offset error negligible.

As the master voltage rises, the slave voltage rises identically (aside from the 80mV offset from SS/TRK to FB when VFB is below 0.8 V). Eventually, the slave voltage reaches its regulation voltage, at which point the internal reference takes over the regulation while the SS/TRK input continues to 115 mV above FB, and no longer controls the output voltage. In all cases, to ensure that the output voltage accuracy is not compromised by the SS/TRK voltage being too close to the 0.8V reference voltage, the final value of the SS/TRK voltage of the slave should be at least 100mV above FB.

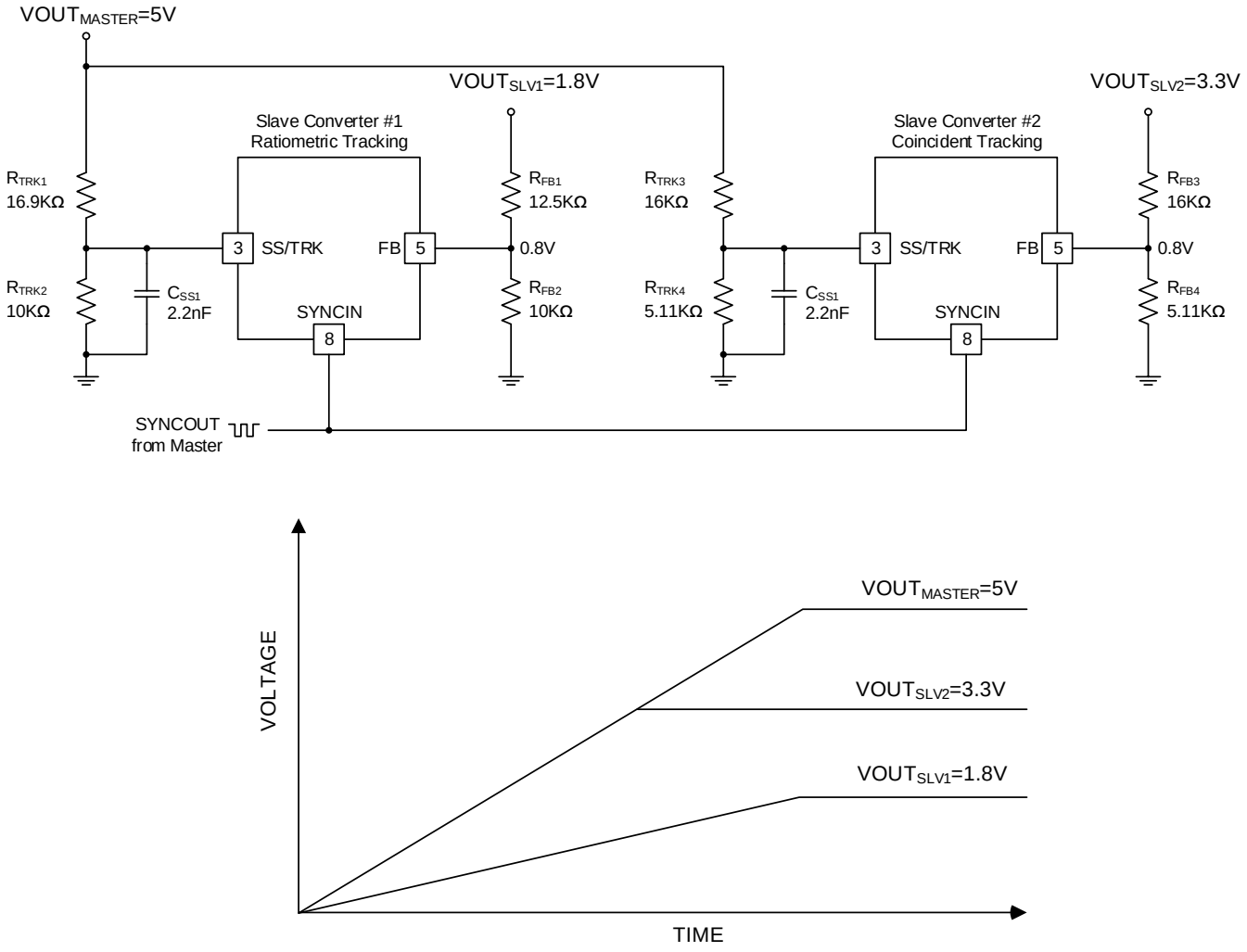


Figure 22. Tracking Implementation with Master, Ratiometric and Coincident Slave Rails

It is the responsibility of the system designer to determine if an external soft-start capacitor is required to keep the device from entering current limit during a start-up event. Likewise, the system designer must also be aware of how fast the input supply ramps if the tracking feature is enabled.

Power Good Monitor PGOOD

The SCT82630 provides a PGOOD indicator pin to indicate when the output voltage is within a regulation window.

When the FB voltage exceeds 94% of the internal reference VREF, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pull-up. If the FB voltage falls below 92% of VREF, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation.

Similarly, when the FB voltage exceeds 108% of VREF, the internal PGOOD switch turns on, pulling PGOOD low. If the FB voltage subsequently falls below 105% of VREF, the PGOOD switch is turned off and PGOOD is pulled high. PGOOD has a built-in deglitch delay of 25 μs.

Use the PGOOD signal as shown in Figure 23 for start-up sequencing of downstream converters, fault protection, and output monitoring. PGOOD is an open-drain output that requires a pull-up resistor to a DC power supply not greater than 13 V. The typical range of pull-up resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pull-up rail.

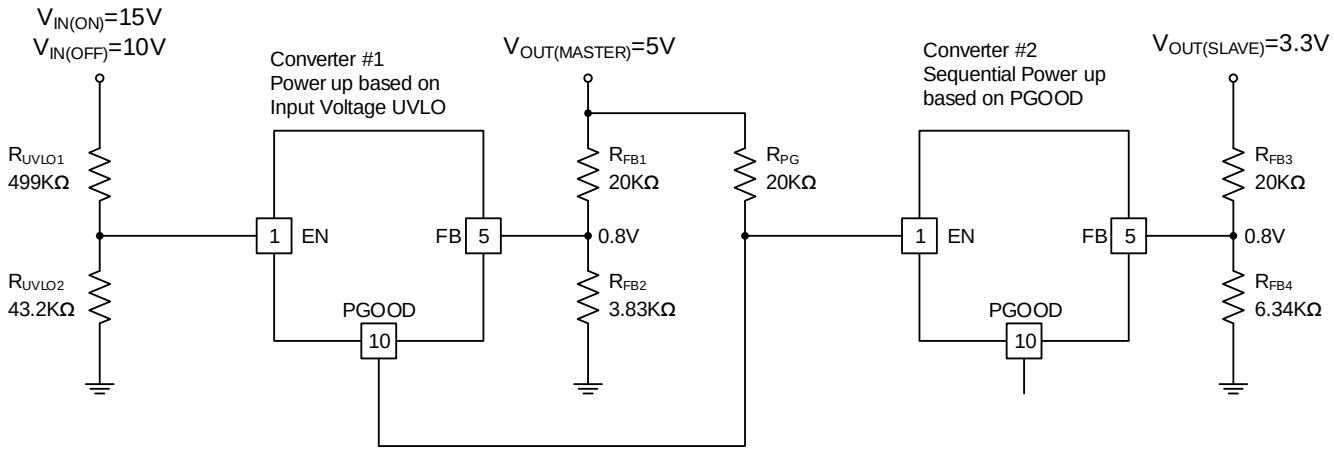


Figure 23. Master-Slave Sequencing Power up Using PGOOD and EN

Switching Frequency and Clock Synchronization

To adjust frequency for optimizing external components for various applications, the system designer can connect a resistor from the RT pin to AGND or synchronize the SCT82630 to an external clock signal through the SYNCIN pin.

A free-running switching frequency can be programmed from 100KHz to 1.2MHz by using a resistor from the RT pin to AGND. The frequency set resistance R_{RT} is calculated by Equation 5. Standard-value resistors for common switching frequencies are given in Table 1.

$$R_{RT}[k\Omega] = \frac{10^4}{F_{SW}[kHz]} \quad (5)$$

Table 1. Frequency Set Resistor R_T

Switching Frequency (kHz)	Frequency Set Resistance (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10
1100	9.09

For applications with stringent frequency or interference requirements, an external clock source connected to the SYNCIN pin can be used to synchronize the high-side power device turn-on to the rising edge of the clock. The rising edge of SW voltage is phase delayed relative to SYNCIN by approximately 100ns. The SCT82630 operates in forced continuous mode when it is synchronized to the external clock. Requirements for the external clock SYNC signal are:

- Clock frequency range: 100 kHz to 1 MHz
- Clock frequency: –20% to +50% of the free-running frequency set by R_{RT}
- Clock maximum voltage amplitude: 13 V
- Clock minimum pulse width: 50 ns

Frequency Spread Spectrum

To reduce EMI, the SCT82630 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the programmed switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency programmed by resistor placed at RT pin and an external clock synchronization application.

Voltage Mode Control

The SCT82630 incorporates a voltage-mode control loop implementation. The amplitude of PWM triangle wave is larger and the pulse width has better anti-noise margin. The duty cycle adjustment is unrestricted with good response to the change of output load. Input voltage feedforward eliminates the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies loop compensation design because the loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, KFF, is 12, equivalent to the input voltage divided by the ramp amplitude, VIN/VRAMP.

Gate Drivers

The SCT82630 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{CC} = 7.5 V, the low-side driver has a low impedance pulldown path of 0.6Ω to minimize the effect of dv/dt induced turn-on, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.3Ω and 0.6Ω pull-up and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, C_{BST}. When the low-side MOSFET conducts, the SW voltage is approximately at 0V and C_{BST} is charged from VCC through the integrated boot diode. Connect a 0.1μF or larger ceramic capacitor close to the BST and SW pins.

Furthermore, there is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

Current Sensing and Overcurrent Protection

The SCT82630 implements two lossless current sense schemes in Figure 24, using the on-state resistance of the low-side MOSFET or alternative implementation with current shunt resistor RS, limiting the inductor current during an overload or output short-circuit condition. The controller senses the inductor current during the PWM off-time when LGD is high.

The ILIM pin sources a reference current that flows in an external resistor, designated RILIM, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND.

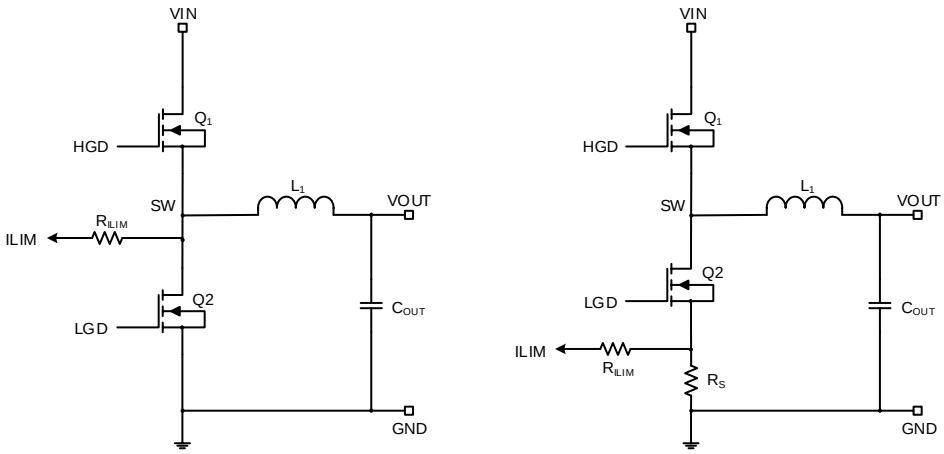


Figure 24. Current Sensing Schemes

Two optional connections sensing inductor current:

- $R_{DS(on)}$ sensing mode: R_{ILIM} is tied to SW to use the RDS(on) of the low-side MOSFET as a sensing element.
- R_{SENSE} shut mode: R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET.

The SCT82630 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly. The ILIM current with RDS-ON sensing is 200 μA at 27°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the RDS(on) temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100μA in RSENSE mode. This controls the valley of the inductor current during a steady state.

Depending on the chosen mode, select the resistance of RILIM using Equation 6 or Equation 7.

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L/2}{I_{RDSON}} \cdot R_{DS(ON)Q2} \quad R_{DS(ON)}\ sensing\ mode \tag{6}$$

$$R_{ILIM} = \frac{I_{OUT} - \Delta I_L/2}{I_{RS}} \cdot R_S \quad R_S\ shut\ sensing\ mode \tag{7}$$

where

- ΔI_L is the peak-to-peak inductor ripple current
- $R_{DS(on)Q2}$ is the on-state resistance of the low-side MOSFET
- I_{RDSON} is the ILIM pin current in R_{DS-ON} mode
- R_S is the resistance of the current-sensing shunt element, and
- I_{RS} is the ILIM pin current in R_{SENSE} mode.

Given the large voltage swings of ILIM in RDS(on) sensing mode, a capacitor designated CILIM connected from ILIM to PGND is essential to the operation of the valley current limit circuit. Choose this capacitance such that the time constant RILIM·CILIM is approximately 6 ns.

Note that current sensing with a shunt component is typically implemented at lower output current levels to provide accurate overcurrent protection. Burdened by the unavoidable efficiency penalty, PCB layout, and additional cost implications, this configuration is not usually implemented in high-current applications except where OCP set point accuracy and stability over the operating temperature range are critical specifications.

Device Functional Modes

Shutdown Mode

The EN pin provides ON / OFF control for the SCT82630. When the EN voltage is below 0.38V typical, the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 7.2 μA typical at VIN = 48 V. The SCT82630 also includes under voltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN voltage exceeds 0.41 V typical and is below the precision enable threshold 1.2 V typically, the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

Active Mode

The SCT82630 is in active mode when the VCC voltage is above its rising UVLO threshold of 5 V and the EN voltage is above the precision EN threshold of 1.2 V. The simplest way to enable the SCT82630 is to tie EN to VIN. This allows self-start-up of the SCT82630 when the input voltage exceeds the VCC threshold plus the LDO dropout voltage from VIN to VCC.

Diode Emulation Mode

The SCT82630 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at no-load and light-load conditions, the disadvantage being slower light-load transient response. The diode emulation feature is configured with the SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect the SYNCIN pin to AGND or leave SYNCIN floating. If forced PWM (FPWM) continuous conduction mode (CCM) operation is desired, tie SYNCIN to VCC either directly or using a pullup resistor. Note that diode emulation mode is automatically engaged to prevent reverse current flow during a pre-bias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

Thermal Shutdown

The SCT82630 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs. When entering thermal shutdown, the device:

- Turns off the high-side and low-side MOSFETs.
- Pulls SS/TRK and PGOOD low.
- Turns off the VCC regulator.
- Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of

20°C (typical).

This is a non-latching protection, and the device will cycle into and out of thermal shutdown if the fault persists.

Control loop compensation

The SCT82630 integrates the voltage mode control loop implementation and feeds the input voltage forward to eliminate the input voltage dependence of the PWM modulator gain. The voltage mode buck control loop is show as below:

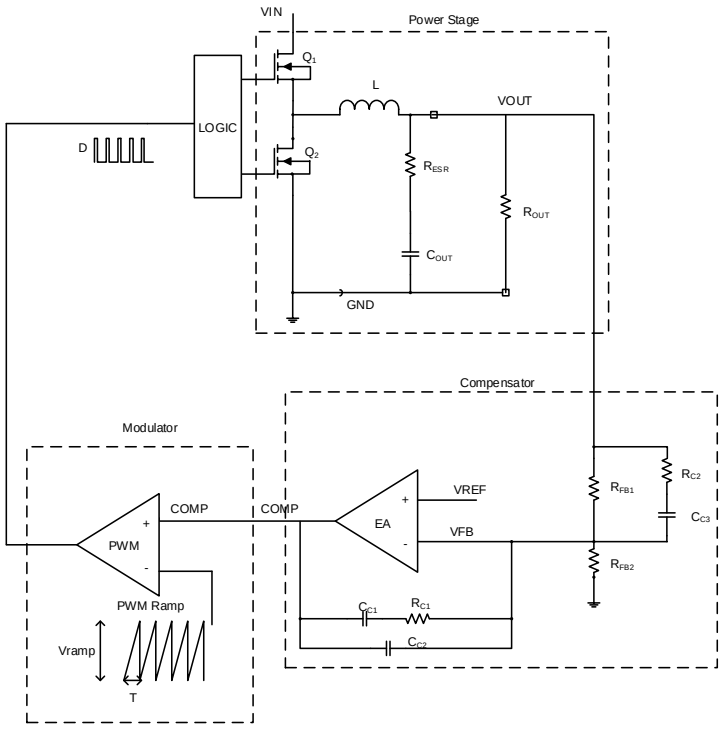


Figure 25. Buck circuit voltage loop control diagram

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, RFB2 , has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN} /V_{RAMP} . The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the SCT82630 (KFF=V_{IN} /V_{RAMP} =12 V/V).

Complete expressions for small-signal frequency analysis are presented in Table 2. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

Table 2. Buck Regulator Small-Signal Analysis

TRANSFER FUNCTION	EXPRESSION
Open-loop transfer function	$T_V(s)=\frac{V_{comp}(s)}{V_o(s)}\cdot\frac{V_o(s)}{d(s)}\cdot\frac{d(s)}{V_{comp}(s)}=G_C(s)\cdot G_{vd}(s)\cdot F_m$

Duty-cycle-to-output transfer function	$G_{vd}(s)=\frac{V_o(s)}{d(s)}=V_{IN}\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^{\ 2}}}$
Compensator transfer function	$G_C(s)=\frac{V_{comp}(s)}{V_o(s)}=\frac{1}{R_{FB1}C_{C1}s}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_m=\frac{d(s)}{V_{comp}(s)}=\frac{1}{V_{ramp}}$

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2} , has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature. The poles and zeros(no include original pole) inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 3.

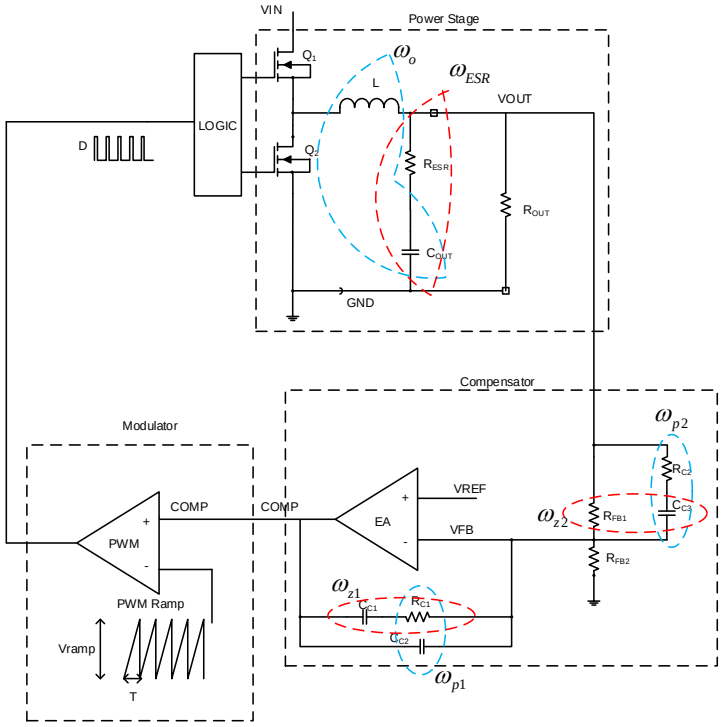


Figure 26. Control loop with poles and zeros

Table 3. Buck Regulator Poles and Zeros

POWER STAGE POLES	POWER STAGE ZEROS	COMPENSATOR POLES	COMPENSATOR ZEROS
$\omega_o = \frac{1}{\sqrt{L \cdot C_{OUT}}}$	$\omega_{ESR} = \frac{1}{R_{ESR} \cdot C_{OUT}}$	$\omega_{p1} = \frac{1}{R_{C1} \cdot C_{C2}}$	$\omega_{z1} = \frac{1}{R_{C1} \cdot C_{C1}}$
		$\omega_{p2} = \frac{1}{R_{C2} \cdot C_{C3}}$	$\omega_{z2} = \frac{1}{(R_{FB1} + R_{C2}) \cdot C_{C3}}$

Figure 27 shows the open-loop response gain and phase. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage, and compensator. The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal, and recording the ensuing frequency response using a network analyzer setup.

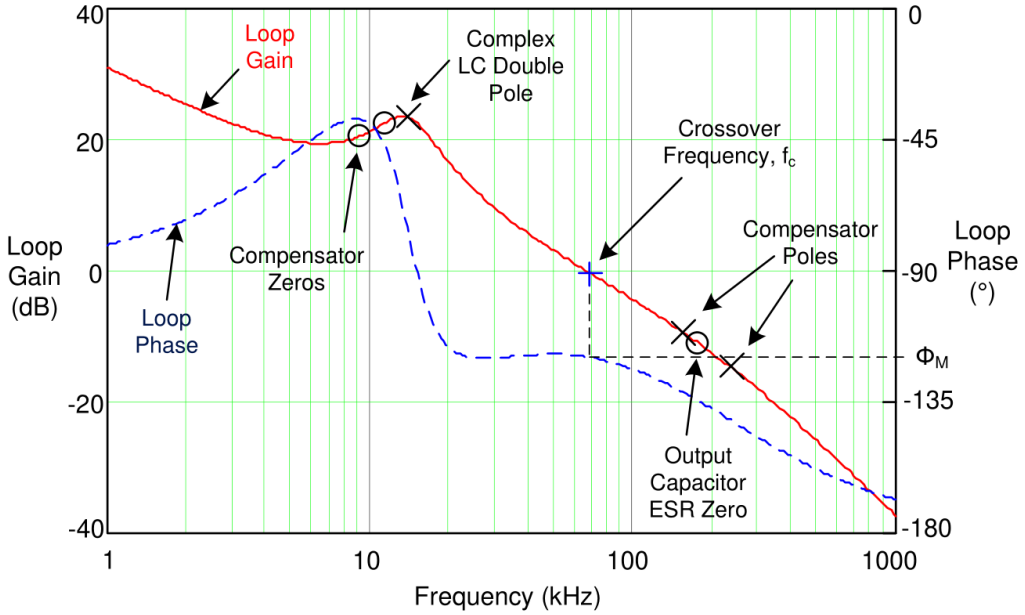


Figure 27. Typical Buck Regulator Loop Gain and Phase with Voltage-Mode Control

If the pole located at ω_{p1} cancels the zero located at ω_{ESR} and the pole at ω_{p2} is located well above crossover, the expression for the loop gain, $T_{v(s)}$ in Table 2, can be manipulated to yield the simplified expression given in Equation8 as below.

$$T_V(s) = \frac{V_{IN}}{V_{ramp}} \cdot \frac{1}{s \cdot R_{FB1} \cdot C_{C1}} \cdot \frac{1}{K} \quad (8)$$

where

- K is a constant, with a value range of 0.5 to 1

Essentially, a multi-order system is reduced to a single-order approximation by judicious choice of compensator components. A simple solution for the crossover frequency (denoted as f_c in Figure 27) with Type-III voltage- mode compensation is derived as shown in Equation 9.

$$\omega_c = 2\pi \cdot f_C = \frac{1}{R_{FB1} \cdot C_{C1}} \cdot \frac{V_{IN}}{V_{ramp}} \cdot \frac{1}{K} \quad (9)$$

The loop crossover frequency is usually selected between 1/10 to 1/5 of switching frequency. Inserting an appropriate crossover frequency into Equation 9 gives a target for the mid-band gain of the compensator, f_c. Given an initial value for R_{FB1}, R_{FB2} is then selected based on the desired output voltage. Values for R_{C1}, R_{C2}, C_{C1}, C_{C2}, and C_{C3} are calculated from the design expressions listed in Table 4, with the premise that the compensator poles and zeros are set as follows: $\omega_{z1} = K \cdot \omega_o$, $\omega_{z2} = \omega_o$, $\omega_{p1} = \omega_{SW/2}$, and $\omega_{p2} = \omega_{ESR}$

Table 4. Compensation Component Selection

RESISTORS	CAPACITORS
$R_{FB2} = \frac{R_{FB1}}{(V_{OUT} / V_{REF}) - 1}$	$C_{C1} = K_{FF} / (2\pi f_c \cdot R_{FB1} \cdot K)$
$R_{C1} = \frac{1}{K \cdot \omega_o \cdot C_{C1}}$	$C_{C2} = \frac{1}{\omega_{p1} \cdot R_{C1}}$
$R_{C2} = \frac{\omega_0}{\omega_{ESR} - \omega_0} \cdot R_{FB1}$	$C_{C3} = \frac{1}{\omega_{ESR} \cdot R_{C2}}$

Referring to the bode plot in Figure 27, the phase margin, indicated as φM , is the difference between the loop phase and –180° at crossover. A target of 50° to 70° for this parameter is considered ideal. Additional phase boost is dialed in by locating the compensator zeros at a frequency lower than the LC double pole. This helps mitigate the phase dip associated with the LC filter, particularly at light loads when the Q-factor is higher and the phase dip becomes especially prominent. The ramification of low phase in the frequency domain is an under-damped transient response in the time domain.

The power supply designer now has all the necessary expressions to optimally position the loop crossover frequency while maintaining adequate phase margin over the required line, load and temperature operating ranges.

APPLICATION INFORMATION

Typical Application

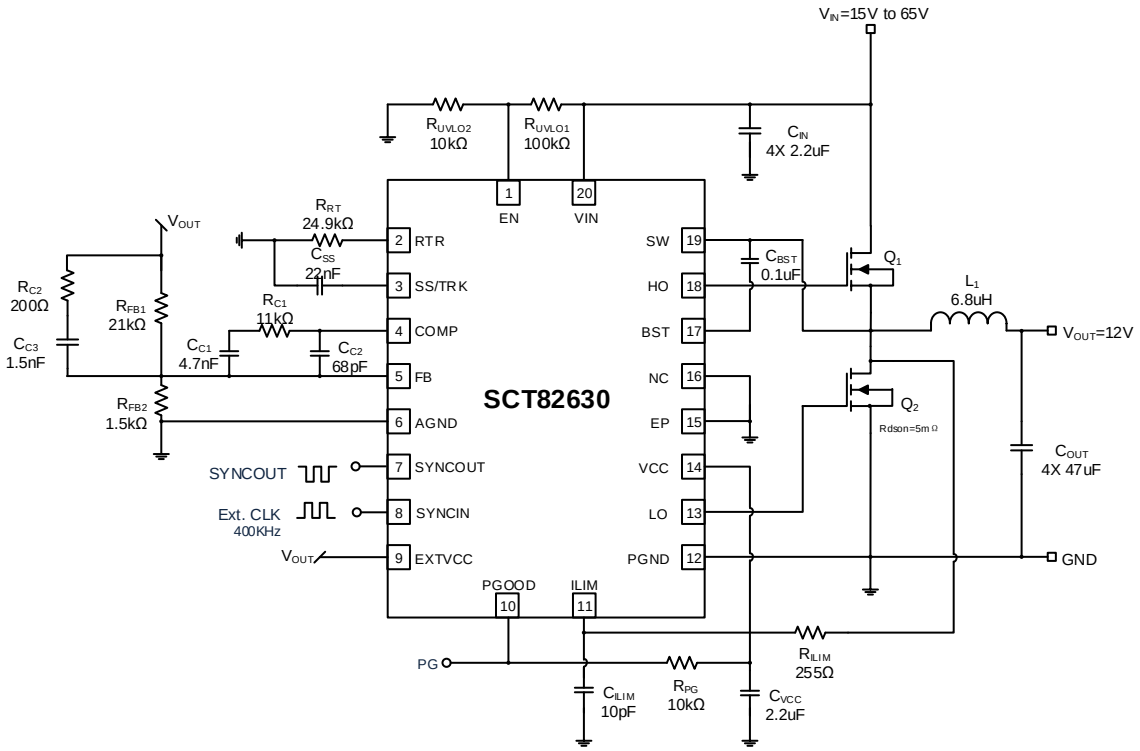


Figure 28. Application Schematic, 24V to 12V, 8A Buck Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 15V to 65V
Output Voltage	12V
Maximum Output Current	8A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 1.25A to 3.75A load step	ΔVout = 200mV
Start Input Voltage (rising VIN)	13.8V
Stop Input Voltage (falling VIN)	12.4V

Application Waveforms

Vin=24V, Vout=12V, unless otherwise noted

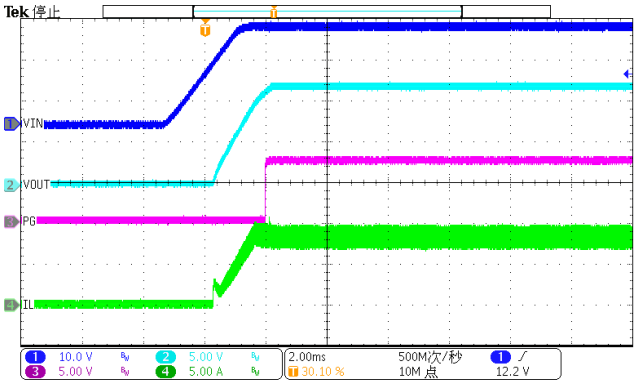


Figure 29. Power up(Iload=8A)

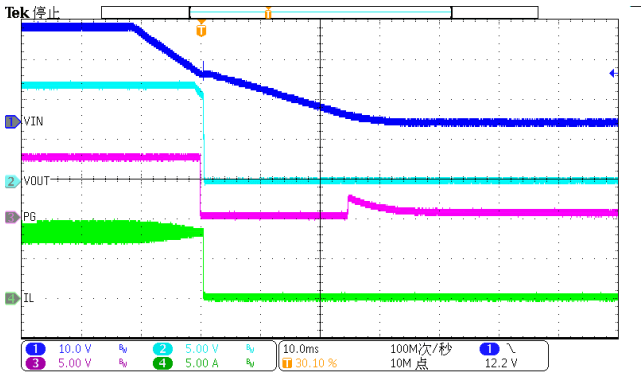


Figure 30. Power down(Iload=8A)

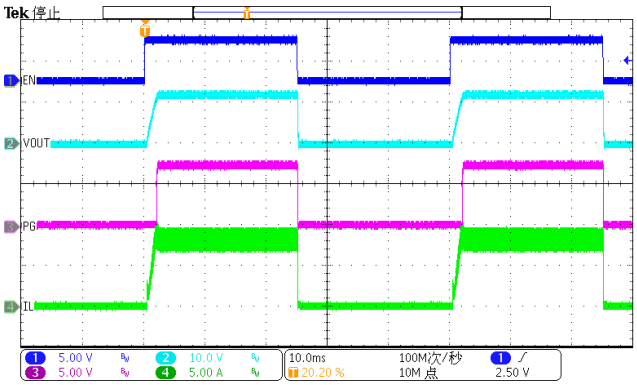


Figure 31. Enable (Iload=8A)

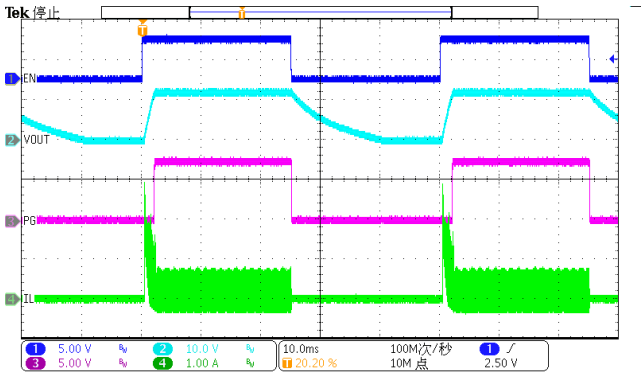


Figure 32. Enable (Iload=0.1A)

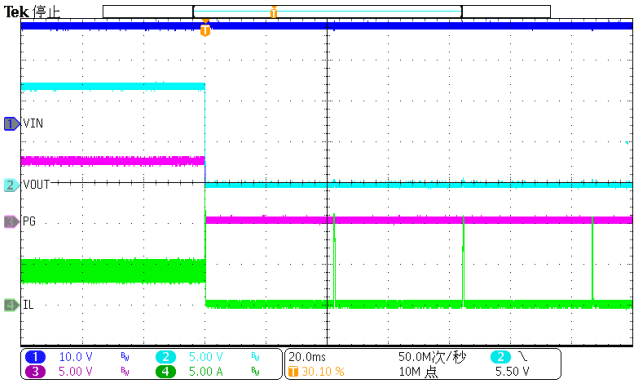


Figure 33. Normal to Hard Short

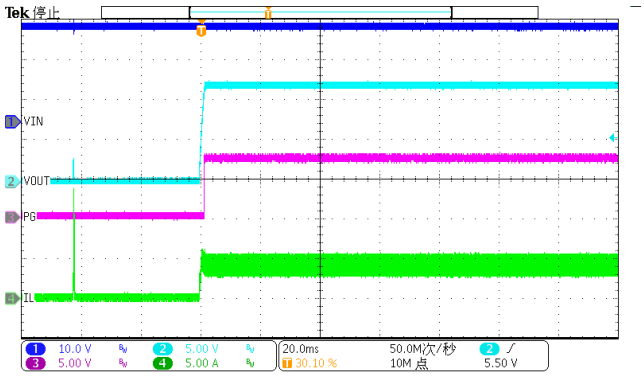


Figure 34. Hard Short Recovery

Application Waveforms(continued)

Vin=24V, Vout=12V, unless otherwise noted

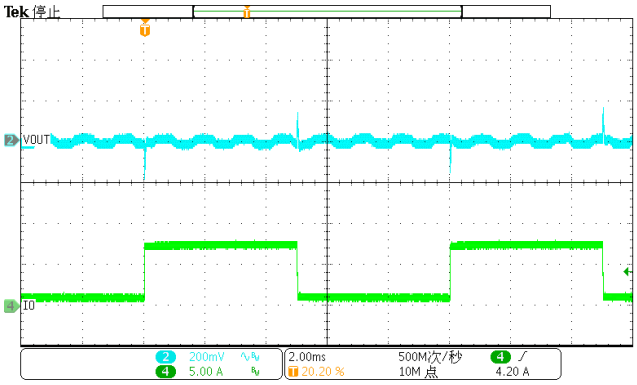


Figure 35. Load Transient (0.8A-7.2A, 1.6A/us)

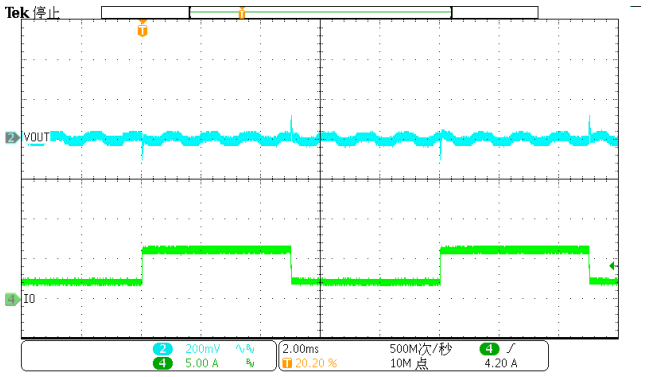


Figure 36. Load Transient (2A-6A, 1.6A/us)

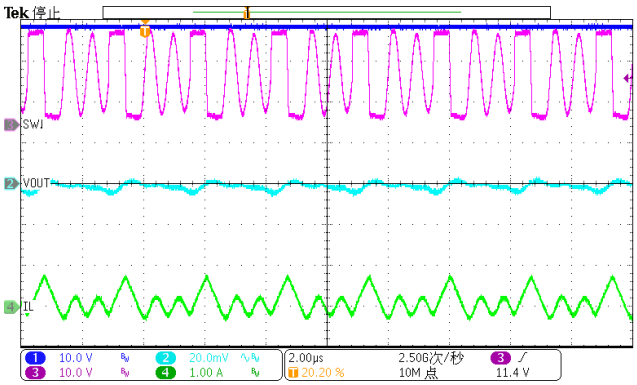


Figure 37. Output Ripple, DCM (Iload=100mA)

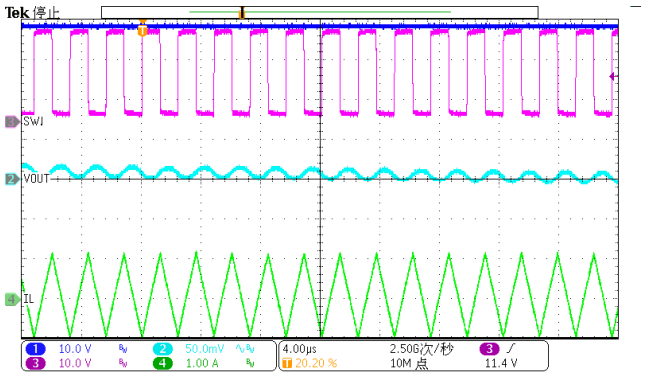


Figure 38. Output Ripple, FCCM (Iload=100mA)

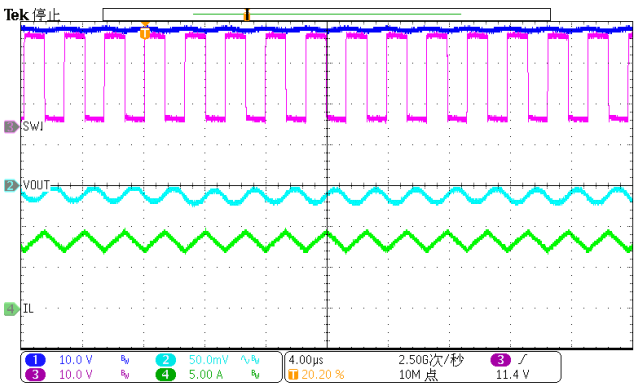


Figure 39. Output Ripple (Iload=8A)

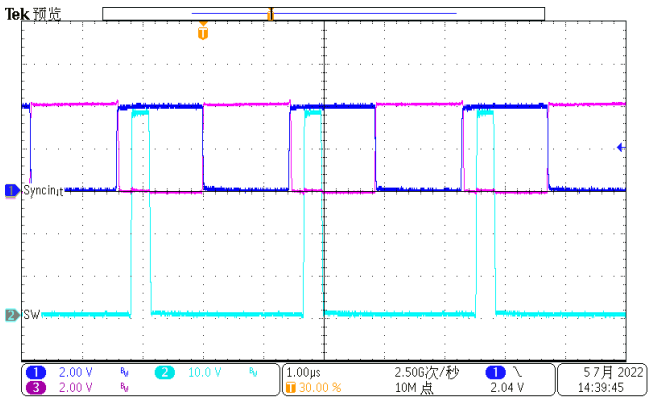


Figure 40. SYNCIN and SYNCOUT

Typical Application

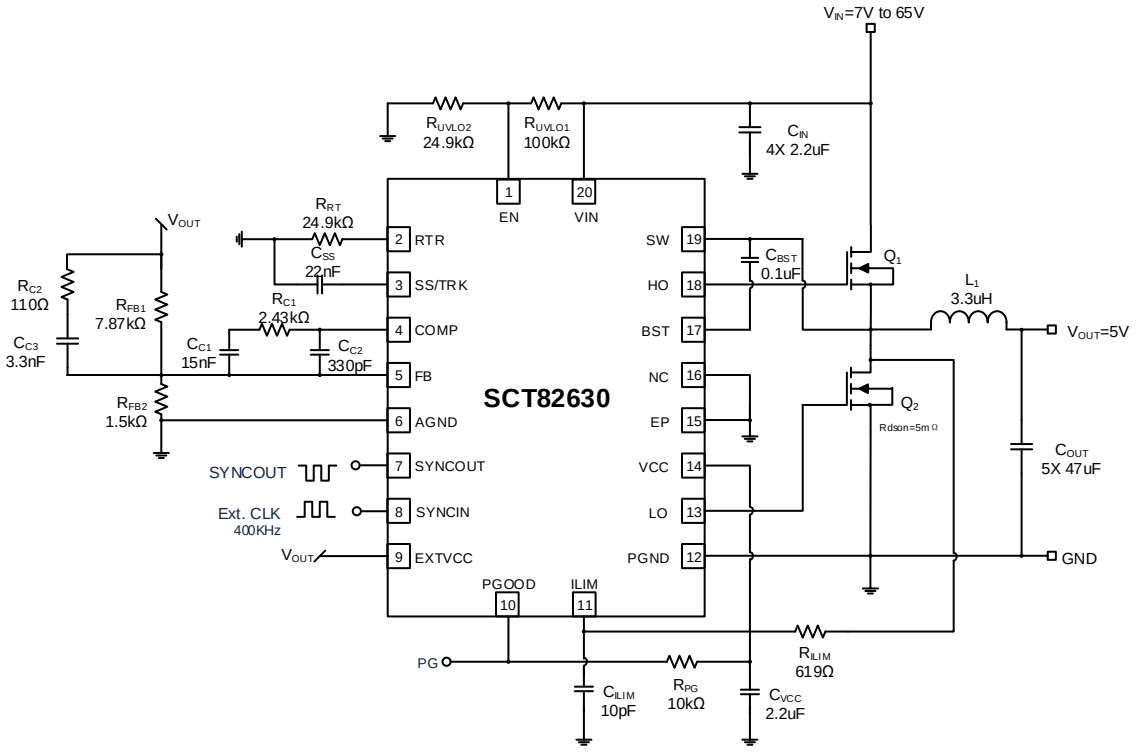


Figure 41. Application Schematic, 24V to 5V, 20A Buck Regulator at 400kHz

Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 7V to 65V
Output Voltage	5V
Maximum Output Current	20A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	16mV
Transient Response 5A to 15A load step	ΔVout = 420mV
Start Input Voltage (rising VIN)	6.3V
Stop Input Voltage (falling VIN)	5.1V

Application Waveforms

Vin=24V, Vout=5V, unless otherwise noted

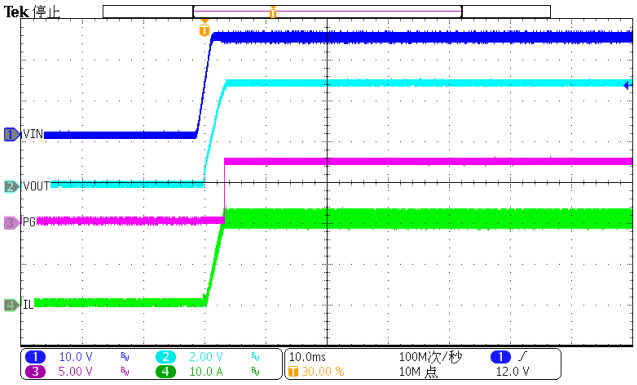


Figure 42. Power up(Iload=20A)

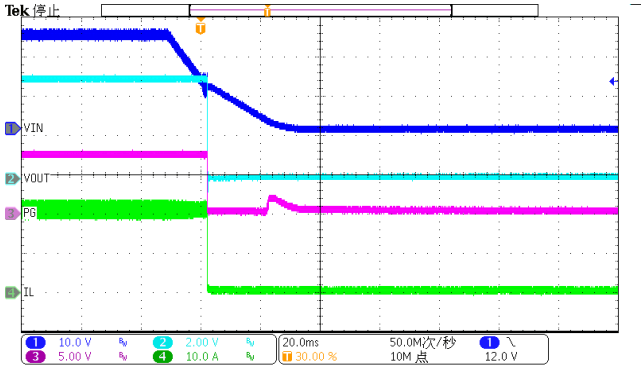


Figure 43. Power down(Iload=20A)

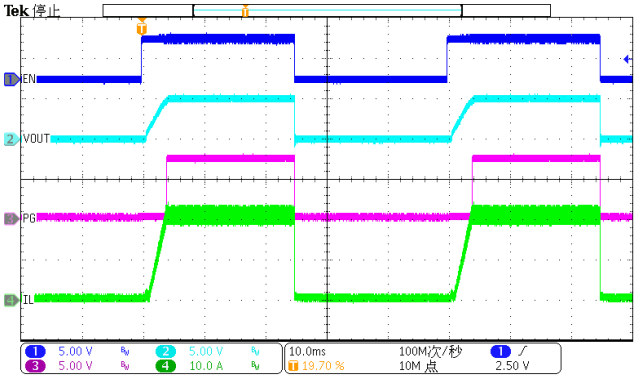


Figure 44.Enable (Iload=20A)

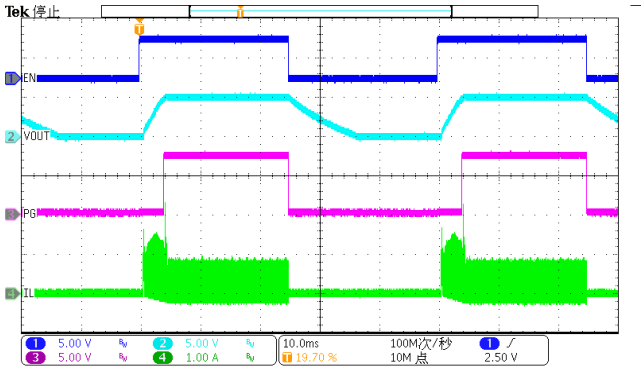


Figure 45. Enable (Iload=0.1A)

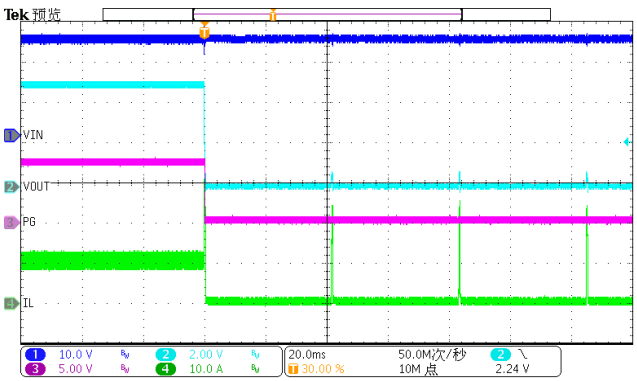


Figure 46. Normal to Hard Short

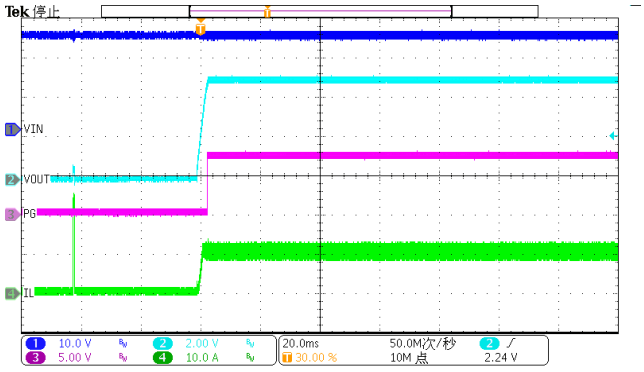


Figure 47. Hard Short Recovery

Application Waveforms(continued)

Vin=24V, Vout=5V, unless otherwise noted

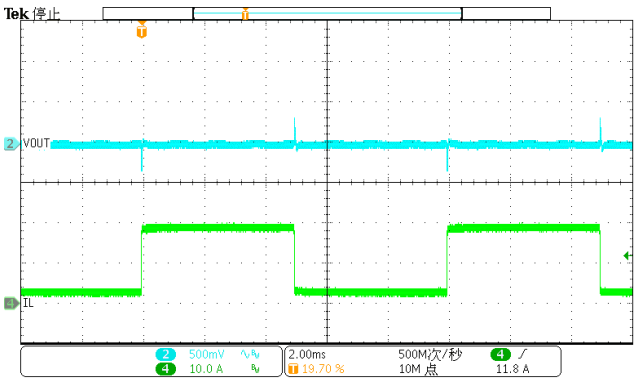


Figure 48. Load Transient (2A-18A, 1.6A/us)

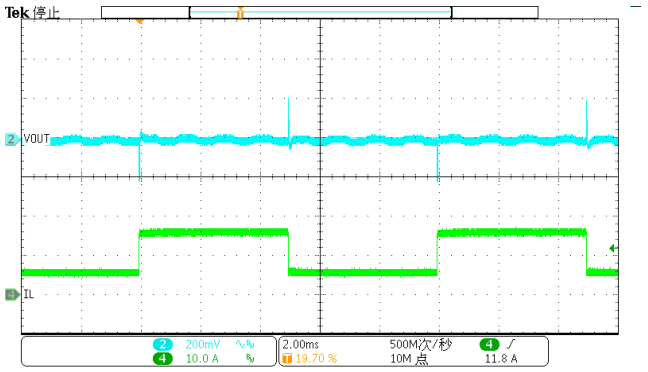


Figure 49. Load Transient (5A-15A, 1.6A/us)

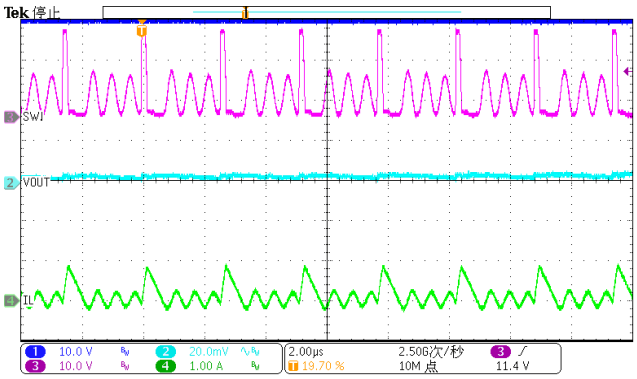


Figure 50. Output Ripple, DCM (Iload=100mA)

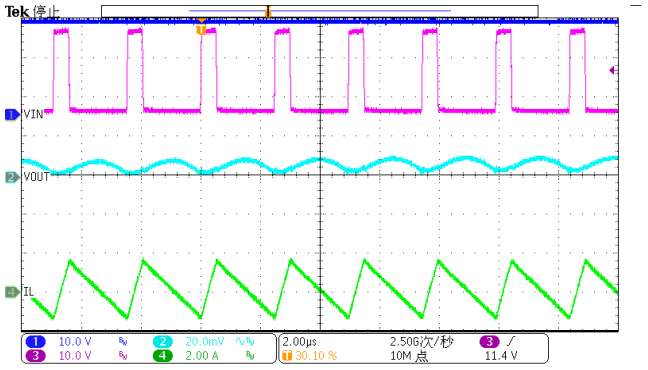


Figure 51. Output Ripple, FCCM (Iload=100mA)

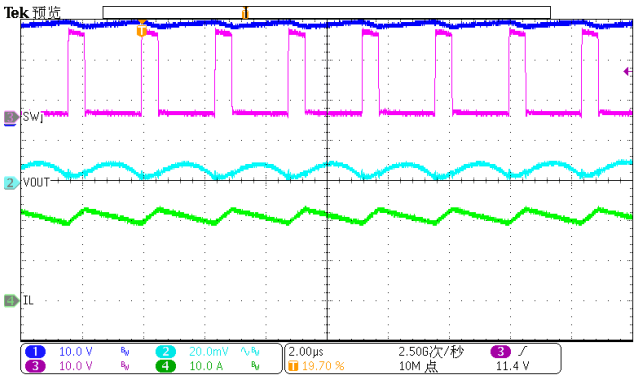


Figure 52. Output Ripple (Iload=20A)

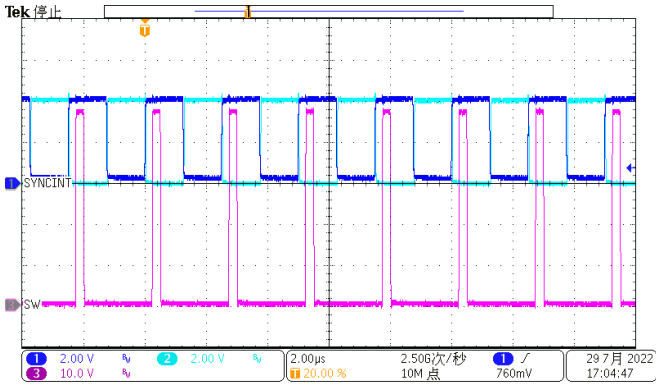


Figure 53. SYNCIN and SYNCOUT

Table 5: Compensation Values for Typical Output Voltage/Capacitor Combinations at fsw=400KHz

Vout	L1	COUT	R_{FB1}	R_{FB2}	R_{c1}	C_{c1}	C_{c2}	R_{c2}	C_{c3}
5V	3.3uH	5*47uF	7.87K	1.5K	2.43K	15nF	330pF	110	3.3nF
12V	6.8uH	4*47uF	21K	1.5K	11K	4.7nF	68pF	200	1.5nF
24V	6.8uH	4*47uF	43.2K	1.5K	23.2K	2.2nF	33pF	422	680pF

Layout Guideline

For PCB power loop design, as shown in Figure. 54, the distance between Q1 and Q2 shall be minimized, and the input capacitance 100nF shall be as close as possible to the drain of Q1 and the power ground. The inductance shall be close to the switching node to minimize the current loop. The small area of the buck regulator hot loop is denoted by the white arrow in Figure 54. This is critical to minimize EMI as well as switch-node voltage overshoot and ringing.

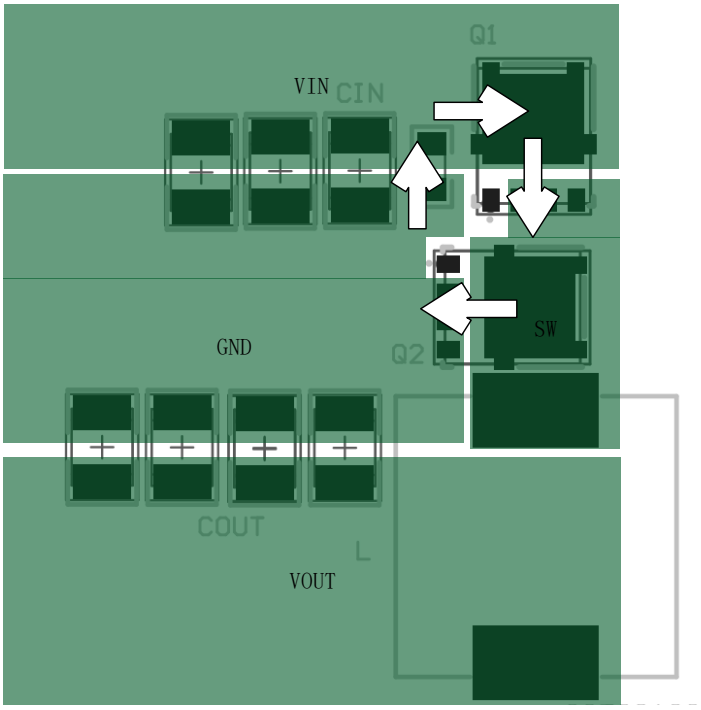


Figure 54. Power stage PCB Layout

Figure 55 shows an example PCB layout based on the SCT82630 design. In order to prevent the PGND from interfering with the controller AGND, It is recommended to use a single point connection between the two ground.

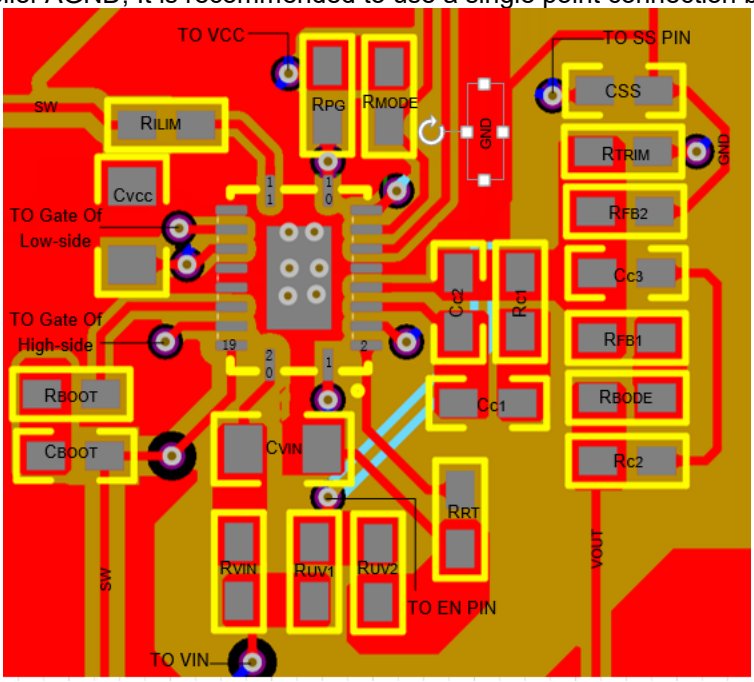
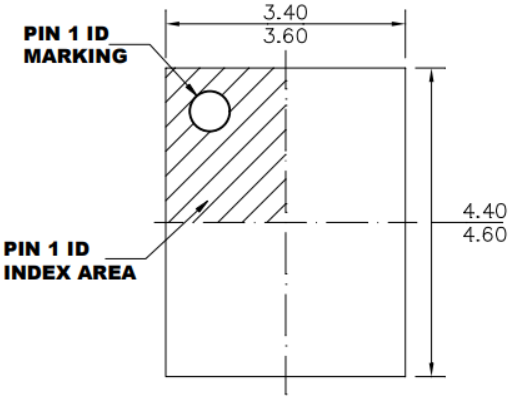
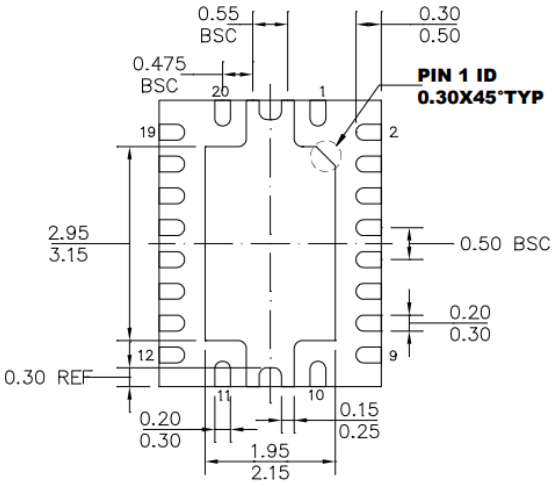


Figure 55. Controller PCB Layout

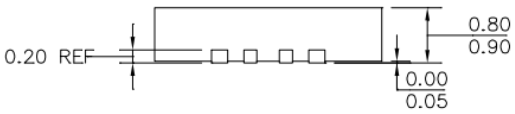
PACKAGE INFORMATION



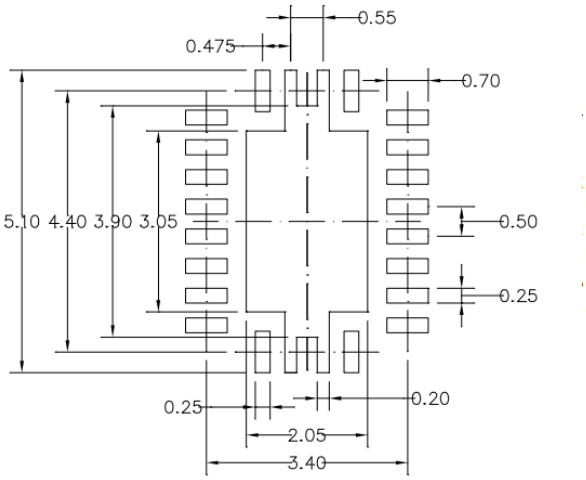
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

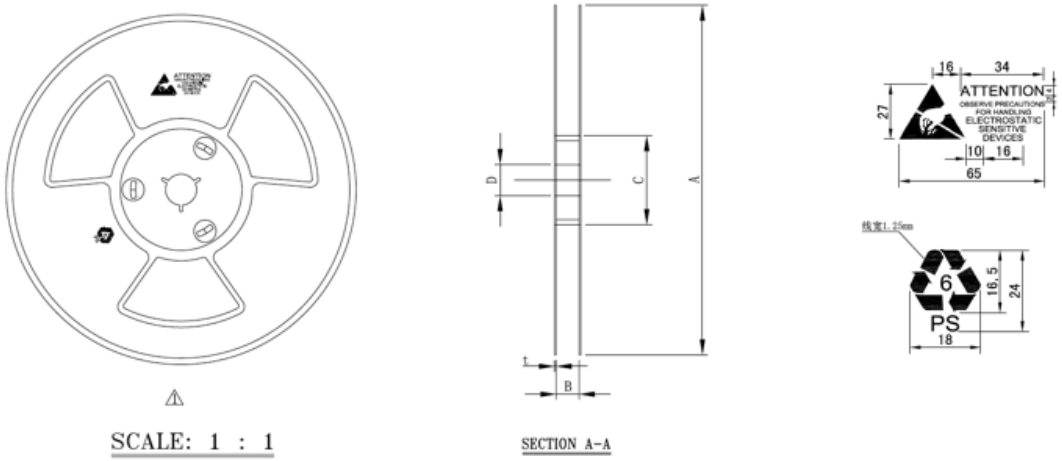
QFN-20L (3.5*4.5) Package Outline Dimensions

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3. LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4. JEDEC REFERENCE IS MO-220.
5. DRAWING IS NOT TO SCALE.

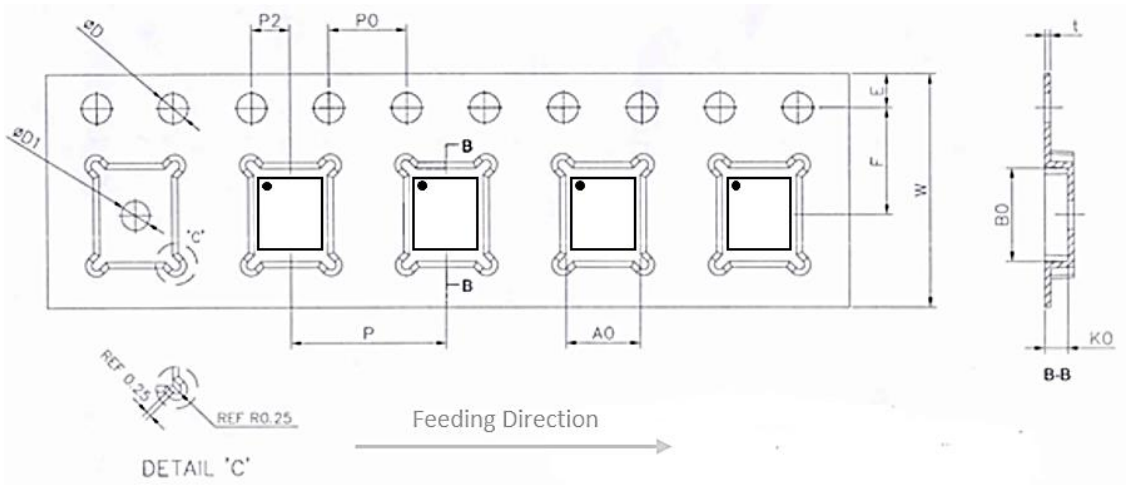
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT82630DHKR	QFN 3.5mmx4.5mm	20	3000



REEL DIMENSIONS

Reel Width	A	B	C	D	t
12	Ø329±1	12.8±1	Ø100±1	Ø13.3±0.3	2.0±0.3



TAPE DIMENSIONS

W (mm)	A0 (mm)	B0 (mm)	K0 (mm)	t (mm)	P (mm)
12±0.30	3.80±0.10	4.80±0.10	1.18±0.10	0.30±0.05	8±0.10

E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	10P0 (mm)
1.75±0.10	5.50±0.10	2.00±0.10	1.55±0.10	1.50MIN	4.00±0.10	40.0±0.20

